EN63A0QI
12A Synchronous Highly Integrated DC-DC Power SoC

Description

The EN63A0QI is a Power System on a Chip (PowerSoC) DC to DC converter in a 76 pin QFN module. It offers highly efficient performance along with a rich and proven feature set that facilitate ease of use in systems that are sensitive to beat tones. The switching frequency can be synchronized to an external clock or other EN63A0QIs. Other features include precision Enable threshold, pre-bias monotonic start-up, and parallel operation.

The EN63A0QI is specifically designed to meet the precise voltage and fast transient requirements of present and future high-performance, low-power processor, DSP, FPGA, memory boards and system level applications in distributed power architecture. The device's advanced circuit techniques, ultra high switching frequency, and proprietary integrated inductor technology deliver high-quality, ultra compact, non-isolated DC-DC conversion.

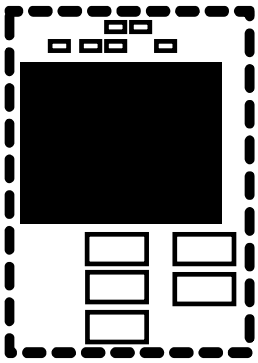


Figure 1: BOM layout of EN63A0QI solution for maximum performance. Total Area ≈ 227 mm^2

The Enpirion integrated inductor solution significantly helps to reduce noise. The complete power converter solution enhances productivity by offering greatly simplified board design, layout and manufacturing requirements. All Enpirion products are RoHS compliant and lead-free manufacturing environment compatible.

Ordering Information

Part Number	Temp Rating (°C)	Package
EN63A0QI	-40 to +85	76-pin QFN T&R
EN63A0QI-E	QFN Evaluation Board	

Features

- High efficiency, up to 96%.
- Excellent ripple and EMI performance.
- Up to 12A continuous operating current.
- 1.2 MHz operating frequency with ability to synchronize to an external clock source or serve as the primary source.
- External programmable Frequency between 0.9MHz and 1.5MHz for application tuning.
- 2% Output Voltage Accuracy over line, load, temp
- EN63A0QI is a member of a family of devices between 1A to 12A load capacity with small total PCB footprints from 156mm^2 and 227mm^2.
- Precision Enable threshold for sequencing.
- Monotonic start-up with pre-bias.
- Programmable soft-start time. Soft Shutdown.
- Master/slave configuration for parallel operation.
- Thermal shutdown, over current, short circuit, and under-voltage protection.
- RoHS compliant, MSL level 3, 260C reflow.

Applications

- Point of load regulation for low-power processors, multi-core processors, communication processor, DSPs, FPGAs, and ASICs
- Low voltage, distributed power architectures with 0.8, 1.0, 1.2, 2.5V, 3.3V, 5V or 6V rails
- Blade servers, RAID storage cards, LAN/SAN adapter cards, wireless base stations, industrial automation, test and measurement, embedded computing, communications, and multi-function printers
- High efficiency 12V intermediate bus architectures
- Beat frequency sensitive applications
- Ripple/Noise Sensitive Applications

Schematic

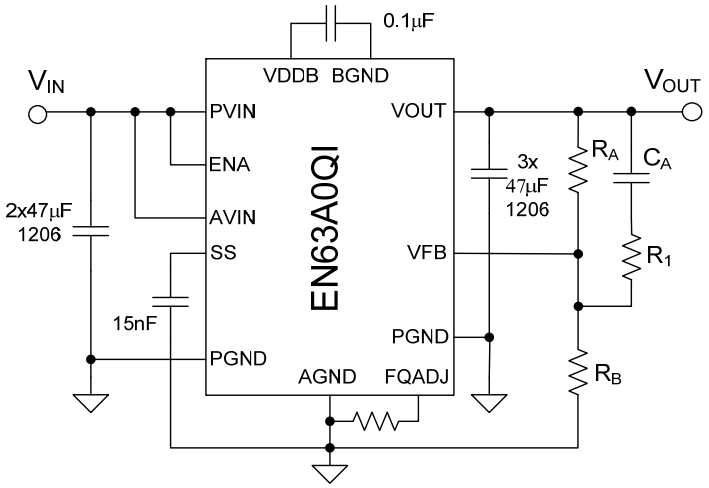


Figure 2: Simple Application Schematic for maximum performance. Unless otherwise specified, all passive components can be 0402 or smaller.

Pin Assignments (Top View)

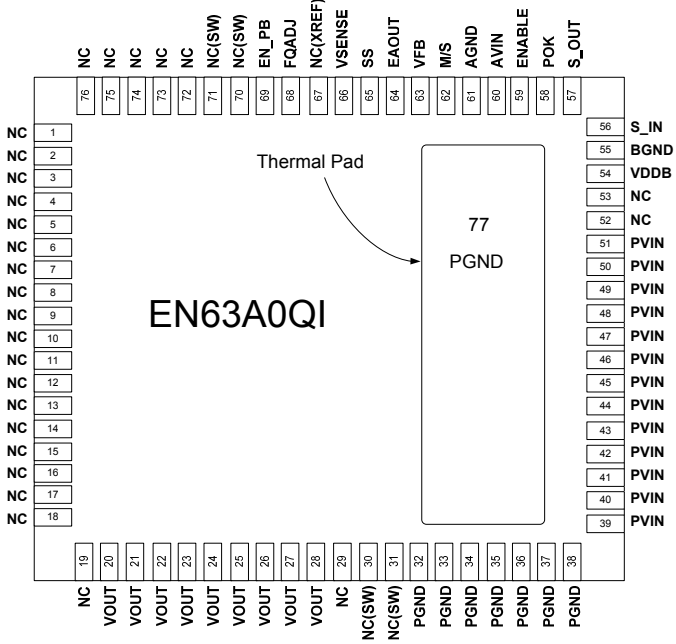


Figure 3: Pin Out Diagram (Top View)

NOTE: All pins must be soldered to PCB.

Pin Description

PIN	NAME	FUNCTION
1-19, 29, 52-53, 72-76	NC	NO CONNECT: These pins must be soldered to PCB but not be electrically connected to each other or to any external signal, voltage, or ground. These pins may be connected internally. Failure to follow this guideline may result in device damage.
20-28	VOUT	Regulated converter output. Connect to the load, and place output filter capacitor(s) between these pins and PGND pins 28-31.
30-31, 70-71	NC(SW)	NO CONNECT: These pins are internally connected to the common switching node of the internal MOSFETs. They must be soldered to PCB but not be electrically connected to any external signal, ground, or voltage. Failure to follow this guideline may result in device damage.
32-38	PGND	Input/Output power ground. Connect these pins to the ground electrode of the input and output filter capacitors. See VOUT and PVIN descriptions for more details.
39-51	PVIN	Input power supply. Connect to input power supply, place input filter capacitor(s) between these pins and PGND pins 32-34.
54	VDDB	Internal regulated voltage used for the internal control circuitry. Decouple with a 0.1uF capacitor to BGND for improved efficiency.
55	BGND	See pin 54 description.
56	S_IN	Digital Input. Depending on the M/S pin, this pin accepts either an input clock to phase lock the internal switching frequency or a S_OUT signal from another EN63A0QI. Leave this pin floating if it is not used.
57	S_OUT	Digital Output. Depending on the M/S pin, either a clock signal synchronous with the internal switching frequency or the PWM signal is output on this pin. Leave this pin floating if it is not used.
58	POK	POK is a logic high when VOUT is within -10% to +20% of the programmed output voltage. This pin has an internal pull-up resistor to AVIN with a nominal value of 94K ohms. This pin can sink a maximum 4mA.
59	ENABLE	This is the Device Enable pin. Floating this pin or a high level enables the device while a low level disables the device. A voltage ramp from another power converter may be applied for precision Enable.
60	AVIN	Analog input voltage for the controller circuits. Connect this pin to the input power supply (PVIN) through a 1 ohm resistor. Can also be connected to an auxiliary supply within a voltage range that is sequencing.

PIN	NAME	FUNCTION
61	AGND	This is the quiet ground for the controller.
62	M/S	This is a Ternary Input put. Floating the pin disables parallel operation. A low level configures the device as Master and a High level configures the device as a slave.
63	VFB	This is the External Feedback input pin. A resistor divider connects from the output to AGND. The mid-point of the resistor divider is connected to VFB. (A feed-forward capacitor is required across the upper resistor.) The output voltage regulates so as to make the VFB node voltage = 0.600volt.
64	EAOUT	Optional Error Amplifier output. Allows for customization of the control loop.
65	SS	A soft-start capacitor is connected between this pin and AGND. The value of the capacitor controls the soft-start interval.
66	VSENSE	This pin senses the output voltage when the device is in Back-feed (or Pre-bias) mode.
67	NC (XREF)	NO CONNECT: Precision External voltage reference input. Feature is available in a separate part number. Application of external reference overrides the device's internal reference. Contact Enpirion for more information.
68	FQADJ	This pin must have a resistor to AGND, which sets the free running frequency of the internal oscillator.
69	EN_PB	This is the Enable Pre-Bias Input. When this pin is pulled high, the Device will support monotonic start-up under a pre-biased load. This pin is pulled high internally. Pull this pin to GND if there is no need to support a pre-bias on the output.
77	PGND	Device thermal pad to be connected to the system GND plane for heat-sinking purposes. See Layout Recommendations section.

Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN	MAX	UNITS
Voltages on: PVIN, AVIN, VOUT		-0.3	7.0	V
Voltages on: EN, POK, M/S		-0.3	V_{IN}+0.3	V
Voltages on: VFB, EXTREF, EAOUT, SS, S_IN, S_OUT, FQADJ		-0.3	2.5	V
Storage Temperature Range	T_{STG}	-65	150	°C
Maximum Operating Junction Temperature	$T_{J\text{-}ABS\ Max}$		150	°C
Reflow Temp, 10 Sec, MSL3 JEDEC J-STD-020A			260	°C
ESD Rating (based on Human Body Model)			2000	V
ESD Rating (based on CDM)			500	V

Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Voltage Range	V_{IN}	2.5	6.6	V
Output Voltage Range	V_{OUT}	0.60	V_{IN} - 0.05*I_{LOAD}	V
Output Current	I_{OUT}		12[2]	A
Operating Ambient Temperature	T_A	- 40	+85	°C

Thermal Characteristics

PARAMETER	SYMBOL	TYP	UNITS
Thermal Resistance: Junction to Ambient (0 LFM) (**Note 1**)	θ_{JA}	16	°C/W
Thermal Resistance: Junction to Case (0 LFM)	θ_{JC}	1.0	°C/W
Thermal Shutdown	T_{SD}	150	°C
Thermal Shutdown Hysteresis	T_{SDH}	20	°C

Note 1: Based on a 2oz. copper board and proper thermal design in line with JEDEC EI/JESD 51 standards.

Note 2: See Table in "Resistor Programmable Frequency" section for allowable Vin, Vout, Switching Frequency.

Electrical Characteristics

NOTE: V_{IN}=6.6V over operating temperature range unless otherwise noted. Typical values are at T_A = 25°C.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Operating Input Voltage	V_{IN}	See Note 5.	2.5		6.6	V
VFB Pin Voltage	V_{VFB}	Internal voltage reference at: V_{IN} = 5V, T_A = 25°C, ILOAD = 0	0.594	0.600	0.606	V
VFB Pin Voltage	V_{VFB}	2.5V ≤ V_{IN} ≤ 6.6V 0A ≤ ILOAD ≤ 10A, T_A = -40 to 85°C	0.588	0.600	0.612	V
VFB Pin Input Leakage Current	I_{VFB}	VFB pin input leakage current	-0.2		0.2	µA
Shut-Down Supply Current	I_S	Power Supply current with Enable=0		2		mA
Under Voltage Lock-out – V_{IN} Rising	V_{UVLOR}	Voltage above which UVLO is not asserted		2.2		V
Under Voltage Lock-out – t_{VIN} Falling	V_{UVLOF}	Voltage below which UVLO is asserted		2.1		V
Output Drop Out Voltage Resistance (Note 1)	V_{DO} R_{DO}	V_{INMIN} - V_{OUT} at Full load Input to Output Resistance		300 50		mV mΩ
Maximum Continuous Output Current	$I_{OUT\_Max\_SRC}$	Maximum load current. See Note 1 and Note 5.	12			A
Maximum Continuous Output Sinking Current	$I_{OUT\_Max\_SNK}$	Maximum load current. See Note 1.	12			A
Over Current Trip Level	I_{OCP}	Sourcing current		18.5		A
Switching Frequency	F_{SW}	Operating frequency with FQADJ resistor = 4.42 kΩ at 5Vin	0.9	1.2	1.5	MHz
External SYNC Clock Frequency Lock Range	F_{PLL_LOCK}	SYNC clock input frequency range	0.9*F_{sw}	F_{sw}	1.1*F_{sw}	MHz
S_IN Clock Amplitude – Low	$V_{S\_IN\_LO}$	SYNC Clock Logic Level			0.8	V
S_IN Clock Amplitude – High	$V_{S\_IN\_HI}$	SYNC Clock Logic Level	1.8		2.5	V
S_IN Clock Duty Cycle (PLL)	DC_{S_INPLL}	M/S Pin Float or Low	20		80	%
S_IN Clock Duty Cycle (PWM)	DC_{S_INPWM}	M/S Pin High	10		90	%
Pre-Bias Level	V_{PB}	Allowable pre-bias as a fraction of programmed output voltage for monotonic start up. Minimum pre-bias voltage = 300mV.	20		75	%
Non-Monotonicity	V_{PB_NM}	Allowable non-monotonicity under pre-bias start up		100		mV
V_{OUT} Range for P_{OK} = High		Range of output voltage as a fraction of programmed value when P_{OK} is asserted	90		120	%

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
P_{OK} Deglitch Delay		Falling edge deglitch delay after output crossing 90% level. F_{SW}=1.0 MHz		62		us
V_{POK} Logic Low level		With 4mA current sink into P_{OK} pin			0.4	V
V_{POK} Logic high level				V_{IN}		V
POK Internal pull-up resistor				94		kΩ
Current Balance	ΔI_{OUT}	With 2-4 converters in parallel, the difference between nominal and actual current levels. ΔV_{IN}<50mV; R_{TRACE}< 10 mΩ, I_{load}= # converter * I_{MAX}		+/-10		%
V_{OUT} Rise Time Accuracy	ΔT_{RISE}	T_{RISE} = C_{SS}*65KΩ; 10nF ≤ C_{SS} ≤30nF; (See Notes 3, 4)	-25		+25	%
Enable Threshold	V_{ENABLE}	2.375V ≤ V_{IN} ≤ 6.6V	1.3			V
Disable Threshold	$V_{DISABLE}$	Max voltage to ensure the converter is disabled			0.8	V
Enable Pin Current	I_{EN}	VIN = 6.6V		50		µA
M/S Ternary Pin Logic Low	V_{T-LOW}	Tie pin to GND		0		V
M/S Ternary Pin Logic Hi	V_{T-HIGH}	Pull up to VIN through an external resistor REXT	TBD	see Input Current below		V
Ternary Pin Input Current	I_{TERN}	VIN = 5.0V, REXT = 24.9kΩ		100		µA
Binary Pin Logic Low Threshold	V_{B-LOW}	ENABLE, S_IN			0.8	V
Binary Pin Logic High Threshold	V_{B-HIGH}	ENABLE, S_IN	1.8			V
S_OUT Low Level	$V_{S\_OUT\_LOW}$				0.4	V
S_OUT High Level	$V_{S\_OUT\_HIGH}$		2.0			V

Note 1: Maximum output current may need to be de-rated, based on operating condition, to meet TJ and headroom requirements.

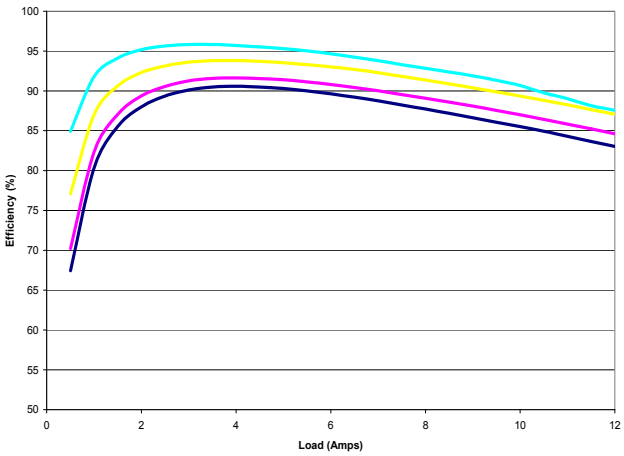
Note 2: POK threshold when VOUT is rising is nominally 92%. This threshold is 90% when VOUT is falling. After crossing the 90% level, there is a 256 clock cycle (~62us at 1 MHz) delay before POK is de-asserted. The 90% and 92% levels are nominal values. Expect these thresholds to vary by ±3%.

Note 3: Parameter not production tested but is guaranteed by design.

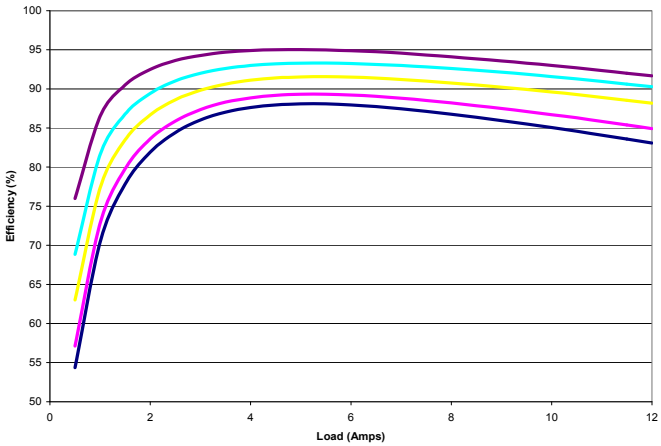
Note 4: Rise time begins when AVIN > V_{UVLO} and Enable=HIGH.

Note 5: See Table in "Resistor Programmable Frequency" section for allowable Vin, Vout.

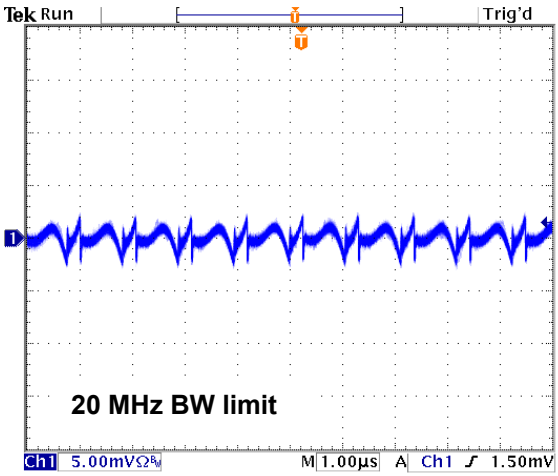
Typical Performance Characteristics



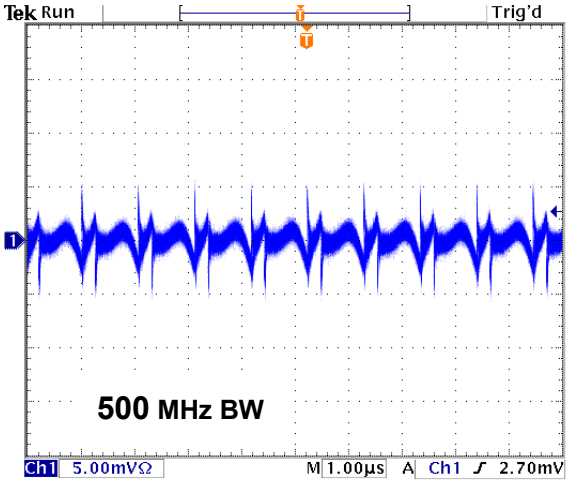
Efficiency V_{IN} = 3.3V, Vout = 2.5, 1.8, 1.2, 1.0 at Frequency = 1.00MHz



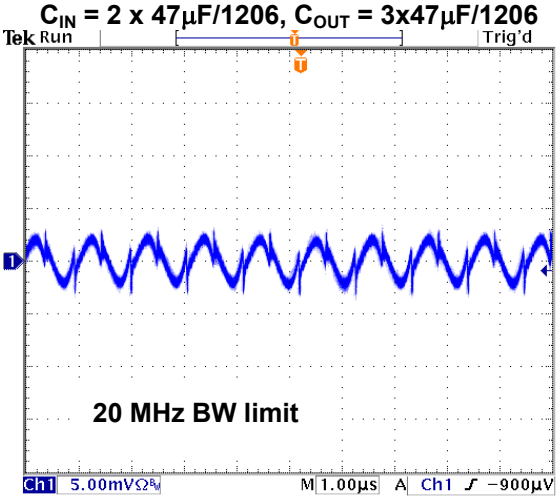
Efficiency V_{IN} = 5.0V, Vout = 3.3, 2.5, 1.8, 1.2, 1.0 at Frequency = 1.00MHz



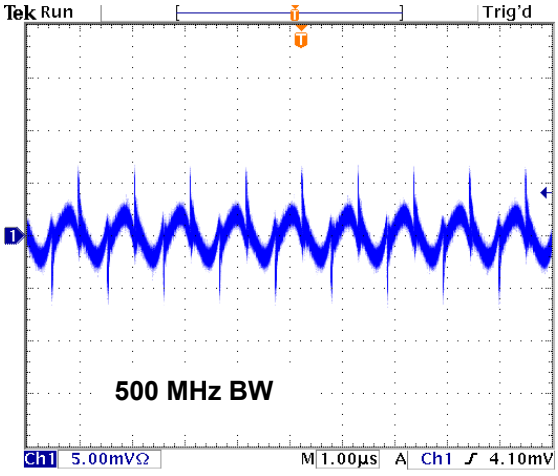
Output Ripple: V_{IN} = 5.0V, V_{OUT} = 1.0V, Iout = 12A
C_{IN} = 2 x 47µF/1206, C_{OUT} = 3x47µF/1206



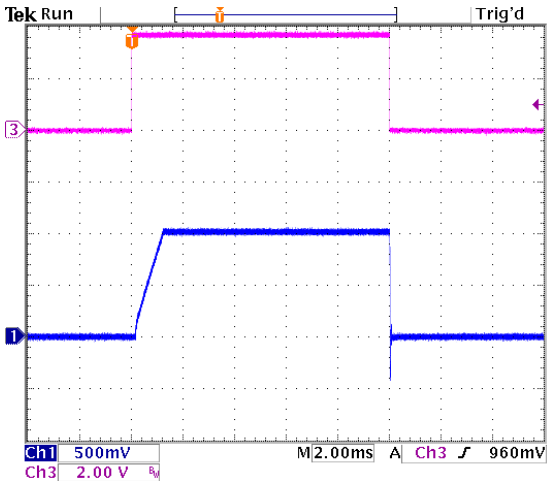
Output Ripple: V_{IN} = 5.0V, V_{OUT} = 1.0V, Iout = 12A
C_{IN} = 2 x47µF/1206, C_{OUT} = 3x47µF/1206



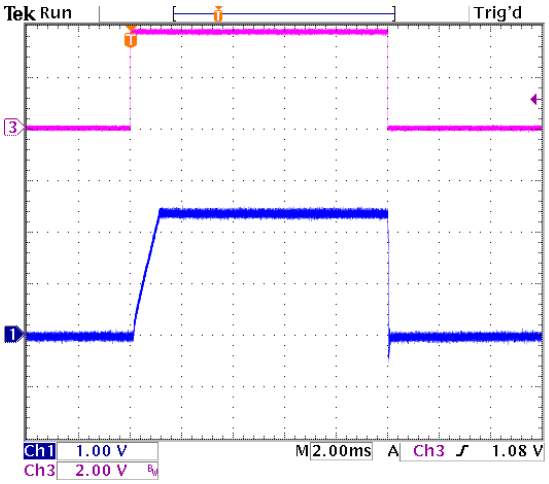
Output Ripple: V_{IN} = 5.0V, V_{OUT} = 2.4V, Iout = 12A
C_{IN} = 2 x 47µF/1206, C_{OUT} = 3x47µF/1206



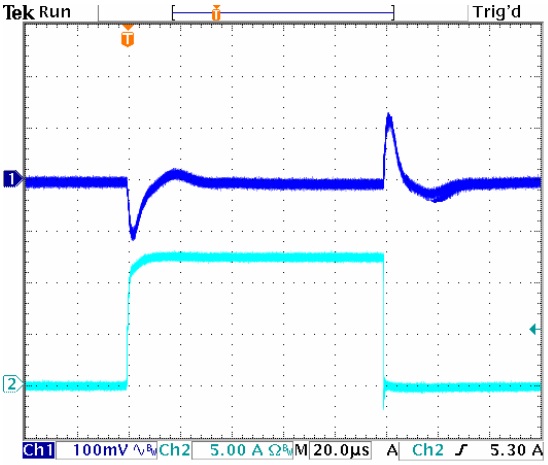
Output Ripple: V_{IN} = 5.0V, V_{OUT} = 2.4V, Iout = 12A
C_{IN} = 2 x 47µF/1206, C_{OUT} = 3x47µF/1206



Power Up/Down at 12A (0.08 Ω) Load: V_{IN}/V_{OUT} = 5.0V/1.0V,
15nF soft-start capacitor, Ch.3: ENABLE, Ch.1: V_{OUT}



Power Up/Down into 12A (0.194 Ω) load: V_{IN}/V_{OUT} = 5.0V/2.4V,
15nF soft-start capacitor, Ch.3: ENABLE, Ch.1: V_{OUT}



Load Transient: V_{IN} = 6.2V, V_{OUT} = 1.5V
Ch.1: V_{OUT}, Ch.2: I_{LOAD} 0↔12A (slew rate ≥ 10A/µS)
C_{IN} ≈ 2x47µF, C_{OUT} ≈ 3x47µF

Functional Block Diagram

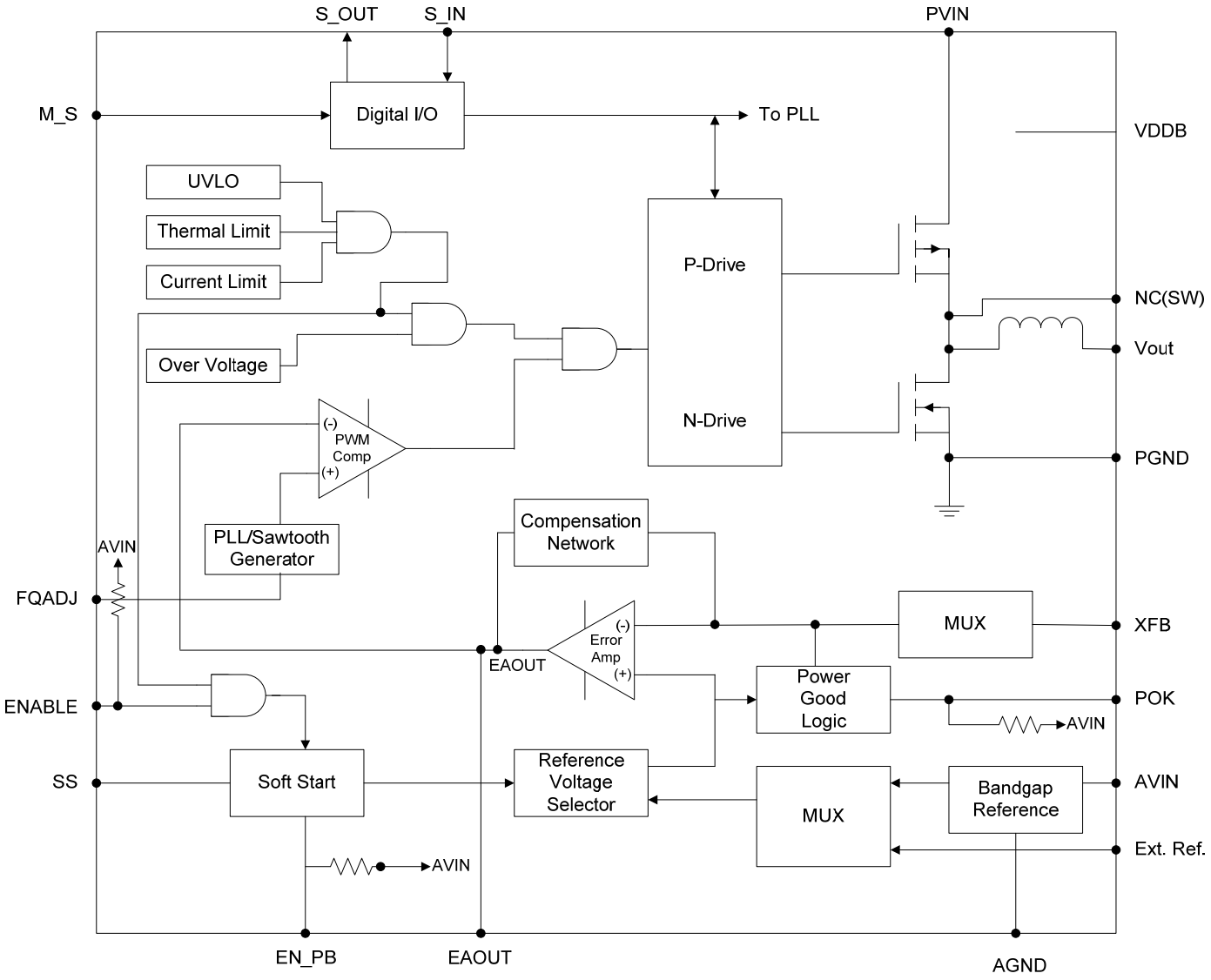


Figure 4: Functional Block Diagram

Functional DescriptionSynchronous Buck Converter

The EN63A0QI is a synchronous, programmable Buck power supply with integrated power MOSFET switches and integrated inductor. The switching supply uses voltage mode control and a low noise PWM topology. This provides superior impedance matching to ICs processed in sub 90nm process technologies. The nominal input voltage range is 2.50 - 6.6 volts. The output voltage is programmed using an external resistor divider network. The feedback control loop is a type IV design. Voltage-mode control and a low-noise PWM topology offers superior performance. The device is optimized for 8A with up to 12A continuous output current operation. Operating between 0.9MHz and 1.5MHz switching frequency enables the use of small-size input and output capacitors.

The power supply has the following protection features:

- Over-current protection with hiccup mode.
- Short Circuit protection.
- Thermal shutdown with hysteresis.
- Under-voltage lockout circuit to disable the converter output when the input voltage is less than approximately 2.2V

The power supply further supports the following features:

- Precision enable threshold
- Soft-start and Soft-shutdown
- Pre-Bias Start-up
- Resistor Programmable Switching Frequency
- Optional external Voltage Reference
- Switching frequency phase lockable to an external oscillator/another PoL device.
- Parallel operation
- Power OK

Precision Enable

The Enable threshold is a precision Analog voltage rather than a digital logic threshold. A precision voltage reference and a comparator circuit are kept powered up even when Enable is de-asserted. Precision threshold along with a proper choice of soft-start capacitor helps to accurately sequence multiple power supplies in a system as desired.

Soft-Start and Soft-Shutdown

The SS pin in conjunction with a small external capacitor between this pin and AGND provides a soft-start function to limit in-rush current during device power-up. When the part is initially powered up, the output voltage is gradually ramped to its final value. The gradual output ramp is achieved by increasing the reference voltage to the error amplifier. A constant current flowing into the soft-start capacitor provides the reference voltage ramp. When the voltage on the soft-start capacitor reaches 0.60V, the output has reached its programmed voltage. The current source will continue, however, to charge the SS capacitor beyond 0.60V to about 1.5V in normal operation. The output ramp rate can be controlled by the choice of soft-start capacitor value.

When the device is disabled, the soft-start capacitor is discharged before the controller is powered down. The EN63A0, however, relies on the output load current as the primary path to discharge the output

The Enable signal, internal to the device, is extended to allow soft-shutdown. In shutdown, the SS capacitor is discharged in a controlled manner. The output ramps down correspondingly and when the output voltage is essentially zero, the controller is turned off.

Pre-Bias Start-up

The EN63A0QI supports the device start up into a pre-biased load. A proprietary circuit ensures the output voltage ramps up from the pre-bias value to the programmed output voltage. Start-up is guaranteed for pre-bias voltages in the range of 20% to 75% of the programmed output voltage with a minimum pre-bias voltage of 300mV. The Pre-Bias feature is engaged by use of the EN_PB pin. For this feature to work properly, V_{IN} must be ramped up first with ENABLE low, and then the converter has to be turned on using the ENABLE pin. Please see Electrical Characteristics table for more details.

Resistor Programmable Frequency

The free running frequency of the oscillator may be altered by connecting a suitable value resistor from the pin FQADJ to AGND. Frequency can be tuned to optimize dynamic performance and efficiency. The tables below show the recommended R_{FQADJ} values for optimum efficiency for specific Vin/Vout combinations and 10A and 12A loads. Contact Enpirion Applications for more information.

Recommended R_{FQADJ} (KΩ) as a Function of V_{IN} & V_{OUT} for 10A Load

V_{IN} \ V_{OUT}	0.8V	1.2V	1.5V	1.8V	2.5V	3.3V
3.3V ±10%	3.57	3.57	4.42	4.42	3.57	NA
5.0V ±10%	3.57	3.57	3.57	4.42	4.42	3.57
6.0V ±10%	3.57	3.57	3.57	4.42	4.42	3.57

Recommended R_{FQADJ} (KΩ) as a Function of V_{IN} & V_{OUT} for 12A Load

V_{IN} \ V_{OUT}	0.8V	1.2V	1.5V	1.8V	2.5V	3.3V
3.3V ±10%	3.57	3.57	4.42	4.42	4.42	NA
5.0V ±10%	3.57	12.1	12.1	4.42	NR	NR
6.0V ±10%	20.0	20.0	20.0	NR	NR	NR

NOTE: NR means device not rated for this operating condition.

External Voltage Reference (Optional)

This feature is available in a separate part number. Contact Enpirion for more information.

When a voltage greater than 0.6V is present at the EXTREF pin the device will detect the presence of the voltage and automatically switch to this voltage as the reference for voltage regulation. Bypassing the internal reference can be used to further improve overall DC set point accuracy and temperature drift associated with the internal reference. EN63A0QI accepts a wide range of input references between 1.15 and 1.5V directly.

Phase-Lock Operation:

With M/S pin floating or at a logical '0,' the internal switching clock of the DC/DC converter can be phase-locked to a clock signal applied to S_IN. When a clock signal is present at S_IN, an activity detector recognizes the presence of the clock signal and the internal oscillator phase locks to the external clock. The external clock could be the system clock or the output of another EN63A0QI. A delayed version of the phase locked clock is output at S_OUT. The clock frequency should be within ±20% of the free running frequency for guaranteed phase-lock. Multiple EN63A0QI devices on a system board may be daisy chained to avoid beat frequency components. The device switching frequency can be adjusted with the resistor to FQADJ as well as by the external clock source for phase-lock.

Master / Slave (Parallel) Operation:

Two EN63A0QI devices may be connected in a Master/Slave configuration to handle larger load currents. The Master device's switching clock may be phase-locked to an external clock source or another EN63A0QI. The device is placed in Master mode by pulling the M/S pin low or in Slave mode by pulling M/S pin high. **When this pin is in Float state, parallel operation is not possible.** In master mode, the internal PWM signal is output on the S_OUT pin. This PWM signal from the Master is fed to the slave device at its S_IN input. The Slave device acts like an extension of the power FETs in the Master. The inductor in the slave prevents crow-bar currents from Master to slave due to timing delays.

POK Operation

The POK signals the output voltage is within the specified range. The POK signal is asserted high when the rising output voltage crosses 92% (nominal) of the programmed output voltage. POK is de-asserted low for 256 clock cycles (62us at 1MHz) after the falling output voltage crosses 90% (nominal) of the programmed voltage. POK remains asserted if the output voltage falls outside the range of 90% to 120% for a period of time less than the de-glitch time. POK is also de-asserted if the output voltage exceeds 120% of the programmed output. If the feedback loop is broken, POK will remain de-asserted (sensed output < 92% of programmed value!) but the actual output voltage will equal the input voltage. If however, there is a short across the PFET, and the feedback is in place, POK will be de-asserted as an over voltage condition. In this case, the power NFET is turned on resulting in a large input supply current. This in turn is expected to trip the upstream power supply powering the EN63A0QI. The POK pin can sink up to 4mA. No pull-up resistor required; when POK is asserted high the output will be pulled up to PVIN.

Over Voltage Protection

If the output voltage exceeds 120% of the programmed value (as sensed at VFB pin), the low-side power FET is turned on. If the over-voltage condition is due to an input-to-output or a high-side power FET short, the turn-on of the low-side power FET will cause a large current draw from the input supply. This will likely cause the input voltage to drop, thus protecting the load.

Over Current Protection

The current limit function is achieved by sensing the current flowing through a sense P-FET. When the sensed current exceeds the current limit, both power FETs are turned off for the rest of the switching cycle. If the over-current condition is removed, the over-current protection circuit will re-enable PWM operation. If the over-current condition persists, the circuit will continue to protect the load.

The OCP trip point is nominally set as specified in the Electrical Characteristics table. In the event the OCP circuit trips consistently in normal operation, the device enters a hiccup mode. The device is disabled for a short while and restarted with a normal soft-start. This cycle can continue indefinitely as long as the over current condition persists.

Thermal Overload Protection

Temperature sensing circuits in the controller will disable operation when the Junction temperature exceeds approximately 150ºC. Once the junction temperature drops by approx 20ºC, the converter will re-start with a normal soft-start.

Input Under-Voltage Lock-Out

When the input voltage is below a required voltage level (V_{UVHI}) for normal operation, the converter switching is inhibited. The lock-out threshold has hysteresis to prevent chatter. Thus when the device is operating normally, the input voltage has to fall below the lower threshold (V_{UVLO}) for the device to stop switching.

Application Information / Layout Recommendation

Soft-start Capacitor Selection

The output voltage ramp time is controlled by the choice of the soft-start capacitor value. The ramp time is defined as the time from when the Enable signal crosses the threshold and the input voltage crosses the upper UVLO threshold to the time when the output voltage reaches 95% of the programmed value. This time is given by the following equation:

$$T_{SS} = C_{ss} * 65k\Omega \text{ (seconds)}$$

Output Voltage Programming and loop Compensation

The EN63A0QI output voltage is programmed using a simple resistor divider network. A phase lead capacitor plus a resistor are required for stabilizing the loop. Figure 5 shows the required components and the equations to calculate their values.

The EN63A0QI output voltage is determined by the voltage presented at the VFB pin. This voltage is set by way of a resistor divider between VOUT and AGND with the midpoint going to VFB.

The EN63A0QI uses a type IV compensation network. Most of this network is integrated. However a phase lead capacitor and a resistor are required in parallel with upper resistor of the external feedback network (see Figure 5). Total compensation is optimized for use with 3X47µF output capacitance and will result in a wide loop bandwidth and excellent load transient performance for most applications. Additional capacitance may be placed beyond the voltage sensing point outside the control loop. Voltage mode operation provides high noise immunity at light load. Further, Voltage mode control provides superior impedance matching to ICs processed in sub 90nm technologies.

In some cases modifications to the compensation or output capacitance may be required to optimize device performance such as transient response, ripple, or hold-up time. The EN63A0QI provides the capability to modify the control loop response to allow for customization for such applications. For more information, contact Enpirion Applications Engineering support.

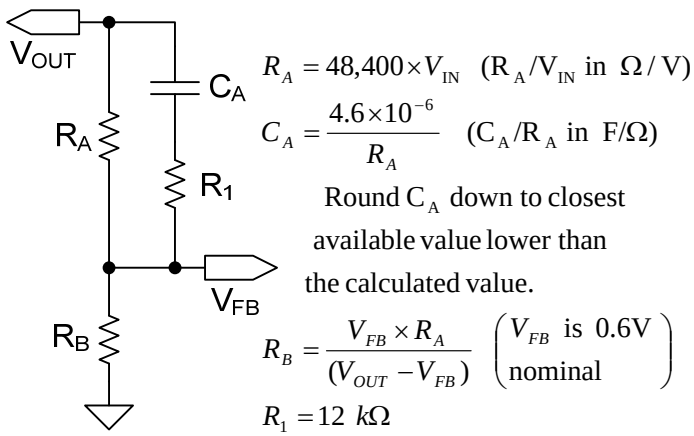


Figure 5: External feedback and compensation network

Enable Operation

With the device input power applied, the device automatically starts to operate with a normal soft-start, provided the input supply voltage is above the UVLO high threshold of ~2.2 volts. To start device operation under ENABLE control, the ENABLE pin has to be initially pulled low and subsequently pulled high when so desired.

Input Capacitor Selection

The EN63A0QI requires between 80–100µF of input capacitance. Low ESR ceramic capacitors are required with X5R or X7R dielectric formulation. Y5V or equivalent dielectric formulations must not be used as these lose capacitance with frequency, temperature and bias voltage.

In some applications, lower value ceramic capacitors maybe needed in parallel with the larger capacitors in order to provide high frequency decoupling.

Recommended Input Capacitors

Description	MFG	P/N
47uF, 10V, 20% X5R, 1206 (2 capacitors needed)	Taiyo Yuden	LMK316BJ476ML-T

Output Capacitor Selection

The EN63A0QI has been optimized for use with about 150µF of output filter capacitance. Additional capacitance may be placed beyond the voltage sensing point outside the control loop. Low ESR ceramic capacitors are required with X5R or X7R dielectric formulation. Y5V or equivalent dielectric formulations must not be used as these lose capacitance with frequency, temperature and bias voltage.

Recommended Output Capacitors

Description	MFG	P/N
47uF, 10V, 20% X5R, 1206 (3 capacitors needed)	Taiyo Yuden	LMK316BJ476ML-T
47uF, 6.3V, 20% X5R, 1206 (3 capacitors needed)	Murata	GRM31CR60J476ME19L
	Taiyo Yuden	JMK316BJ476ML-T
10uF, 6.3V, 10% X7R, 0805 (Optional 1 capacitor in parallel with 3x47uF)	Murata	GRM21BR70J106KE76L
	Taiyo Yuden	JMK212B7106KG-T

Output ripple voltage is primarily determined by the aggregate output capacitor impedance. Placing multiple capacitors in parallel reduces the impedance and hence will result in lower ripple voltage.

$$\frac{1}{Z_{Total}} = \frac{1}{Z_1} + \frac{1}{Z_2} + \ldots + \frac{1}{Z_n}$$

Typical Ripple Voltages

Output Capacitor Configuration	Typical Output Ripple (mVp-p) (as measured on device evaluation board)†
3 x 47 uF	~5mV

† 20 MHz bandwidth limit

Ternary Pin

M/S is a Ternary pin. This pin can assume 3 states – A low state, a high state and a float state. Device operation is controlled by the state of the pin. The pins may be pulled to ground or left floating without any special care. However when pulling high, we recommend tying this pin to VIN with a series resistor. The resistor value may be optimized to reduce the current drawn by the pin by following the equations in 6. The resistance may not be too high as in that case the pin may not recognize the high state.

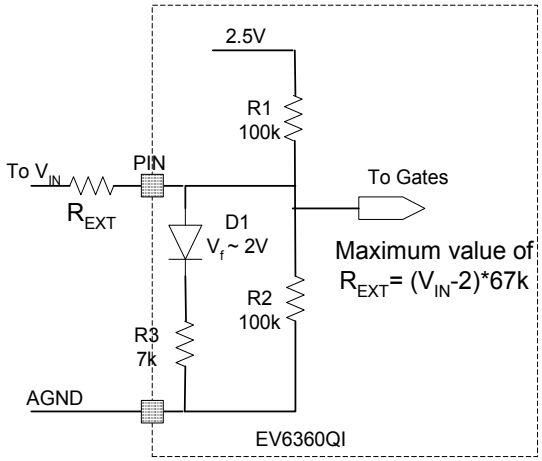


Figure 6: Selection of R_{EXT} to connect ternary pins to V_{IN}

M/S (Master/Slave) Pin States

M/S Pin	Function
Low	This is the Master mode. Switching phase locked to S_IN external clock. S_OUT outputs a delayed version of internal PWM signal
Float	Parallel operation is not feasible. Switching phase locked to S_IN external clock. S_OUT outputs a delayed version of switching clock
High	This is the Slave mode. The S_IN signal drives directly the power FETs. S_OUT outputs a delayed version of S_IN

Contact Enpirion Application support for parallel operation of multiple EN63A0QIs for higher output currents.

Layout Recommendation

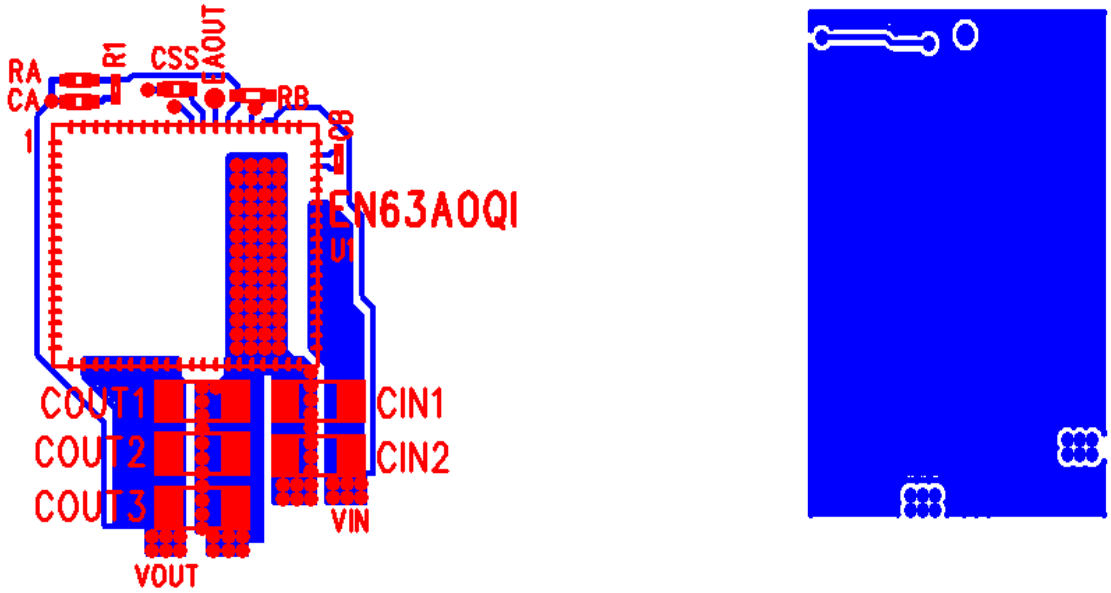


Figure 7: Critical Components and Layer 1 Copper for Minimum Footprint and Layer 2 Ground Plane

Figure 7 above shows critical components and layer 1 traces of the recommended EN63A0 layout for minimum footprint with ENABLE tied to V_{IN}. Please use this figure as a guide when considering the following recommendations. Alternate ENABLE configurations, and other small signal pins need to be connected and routed according to specific customer application. Please see the Gerber files on the Enpirion website www.enpirion.com for exact dimensions and other layers.

Recommendation 1: Input and output filter capacitors should be placed on the same side of the PCB, and as close to the EN63A0QI package as possible. They should be connected to the device with very short and wide traces. Do not use thermal reliefs or spokes when connecting the capacitor pads to the respective nodes. The +V and GND traces between the capacitors and the EN63A0QI should be as close to each other as possible so that the gap between the two nodes is minimized, even under the capacitors.

Recommendation 2: The system ground plane should be the first layer immediately below the surface layer. This ground plane should be continuous and un-interrupted below the converter and the input/output capacitors.

Recommendation 3: The thermal pad underneath the component must be connected to the system ground plane through as many vias as possible. The drill diameter of the vias should be 0.33mm, and the vias must have at least 1 oz. copper plating on the inside wall, making the finished hole size around 0.20-0.26mm. Do not use thermal reliefs or spokes to connect the vias to the ground plane. This connection provides the path for heat dissipation from the converter.

Recommendation 4: Multiple small vias (the same size as the thermal vias) should be used to connect ground terminal of the input capacitor and output capacitors to the system ground plane. It is preferred to put these vias under the capacitors along the edge of the GND copper closest to the +V copper. These vias connect the input/output filter capacitors to the GND plane, and help reduce parasitic inductances in the input and output current loops.

Recommendation 5: AVIN is the power supply for the small-signal control circuits. It should be connected to the input voltage at a quiet point. In Figure 7 this connection is made at the input capacitor.

Recommendation 6: The layer 1 metal under the device must not be more than shown in Figure 7. See the section regarding exposed metal on bottom of package. As with any switch-mode DC/DC converter, try not to run sensitive signal or control lines underneath the converter package on other layers.

Recommendation 7: The V_{OUT} sense point should be just after the last output filter capacitor. Keep the sense trace short in order to avoid noise coupling into the node.

Recommendation 8: Keep R_A, C_A, R_B, and R_1 close to the VFB pin (see Figures 5 and 7). The VFB pin is a high-impedance, sensitive node. Keep the trace to this pin as short as possible. Whenever possible, connect R_B directly to the AGND pin instead of going through the GND plane.

Design Considerations for Lead-Frame Based Modules

Exposed Metal on Bottom of Package

Lead-frames offer many advantages in thermal performance, in reduced electrical lead resistance, and in overall foot print. However, they do require some special considerations.

In the assembly process lead frame construction requires that, for mechanical support, some of the lead-frame cantilevers be exposed at the point where wire-bond or internal passives are attached. This results in several small pads being exposed on the bottom of the package, as shown in Figure 8.

Only the thermal pad and the perimeter pads are to be mechanically or electrically connected to the PC board. The PCB top layer under the EN63A0QI should be clear of any metal (copper pours, traces, or vias) except for the two thermal pads. The “grayed-out” area in Figure 8 represents the area that should be clear of any metal on the top layer of the PCB. Any layer 1 metal under the grayed-out area runs the risk of undesirable shorted connections even if it is covered by soldermask.

Figure 9 shows the package dimensions.

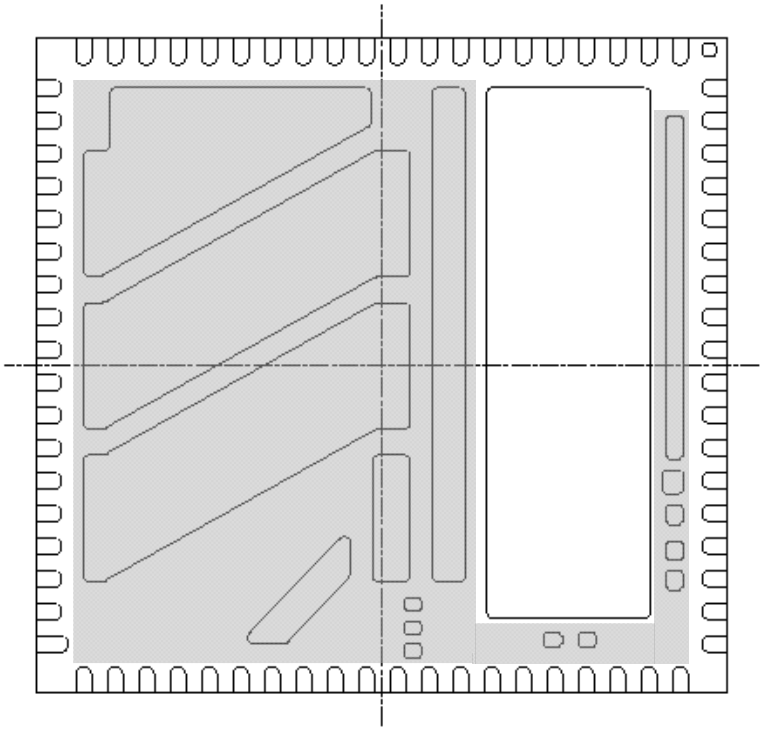


Figure 8: Lead-Frame exposed metal. Grey area highlights exposed metal that is not to be mechanically or electrically connected to the PCB.

Package and Mechanical

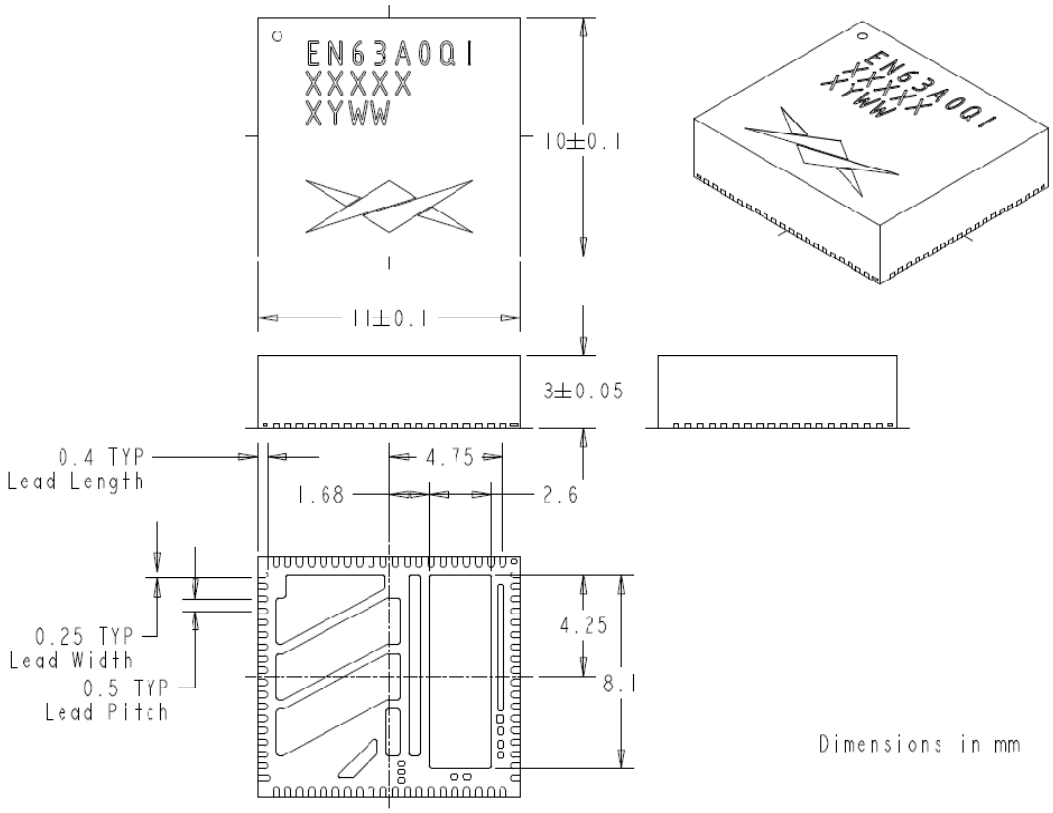


Figure 9: EN63A0QI Package Dimensions

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