Digitally Programmable Sensor Signal Amplifier

Data Sheet **AD8557**

FEATURES

Very low offset voltage: 12 µV maximum over temperature
Very low input offset voltage drift: 65 nV/°C maximum
High CMRR: 96 dB minimum
Digitally programmable gain and output offset voltage
Gain range from 28 to 1300
Qualified for automotive applications
Single-wire serial interface
Stable with any capacitive load
SOIC and LFCSP packages
2.7 V to 5.5 V operation

APPLICATIONS

Automotive sensors
Pressure and position sensors
Precision current sensing
Thermocouple amplifiers
Industrial weigh scales
Strain gages

FUNCTIONAL BLOCK DIAGRAM

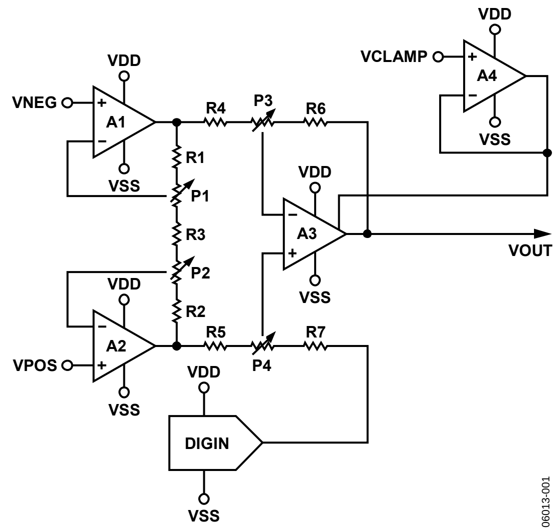

Figure 1.

GENERAL DESCRIPTION

The AD8557 is a zero drift, sensor signal amplifier with digitally programmable gain and output offset. Designed to easily and accurately convert variable pressure sensor and strain bridge outputs to a well-defined output voltage range, the AD8557 accurately amplifies many other differential or single-ended sensor outputs. The AD8557 uses the Analog Devices, Inc., proprietary low noise auto-zero and DigiTrim® technologies to create an accurate and flexible signal processing solution in a compact footprint.

Gain is digitally programmable in a wide range from 28 to 1300 through a serial data interface. Gain adjustment can be fully simulated in circuit and then permanently programmed with reliable polyfuse technology. Output offset voltage is also digitally programmable and is ratiometric to the supply voltage.

In addition to extremely low input offset voltage and input offset voltage drift and very high dc and ac CMRR, the AD8557 also includes a pull-up current source at the input pins and a pull-down current source at the VCLAMP pin. Output clamping set via an external reference voltage allows the AD8557 to drive lower voltage analog-to-digital converters (ADCs) safely and accurately.

When used in conjunction with an ADC referenced to the same supply, the system accuracy becomes immune to normal supply voltage variations. Output offset voltage can be adjusted with a resolution of better than 0.4% of the difference between VDD and VSS. A lockout trim after gain and offset adjustment further ensures field reliability.

The AD8557 is fully specified from −40°C to +125°C. Operating from single-supply voltages of 2.7 V to 5.5 V, the AD8557 is offered in an 8-lead SOIC, and a 4 mm × 4 mm, 16-lead LFCSP.

Rev. D **Document Feedback**

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Technical Support **www.analog.com**

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6/11—Rev. B to Rev. C
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5/07—Revision 0: Initial Version

SPECIFICATIONS

VDD = 5.0 V, VSS = 0.0 V, V_{CM} = 2.5 V, VOUT = 2.5 V, gain = 28, T_A = −40°C to +125°C, unless otherwise specified.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT STAGE						
Input Offset Voltage	V_{OS}			2	12	μV
Input Offset Voltage Drift	T_CV_{OS}			27	65	nV/°C
Input Bias Current	I_B		10	18	25	nA
Input Offset Current	I_{OS}			1	4	nA
Input Voltage Range			0.6		3.8	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0.9 V to 3.6 V, A_V = 28	75	85		dB
		V_{CM} = 0.9 V to 3.6 V, A_V = 1300	96	112		dB
Linearity		VOUT = 0.2 V to 3.4 V		20		ppm
		VOUT = 0.2 V to 4.8 V		1000		ppm
Differential Gain Accuracy		Second stage gain = 10 to 70			1.6	%
Differential Gain Accuracy		Second stage gain = 100 to 250			2.5	%
Differential Gain Temperature Coefficient		Second stage gain = 10 to 250		15	40	ppm/°C
DAC						
Accuracy		Offset codes = 8 to 248		0.7	0.8	%
Ratiometricity		Offset codes = 8 to 248		50		ppm
Output Offset		Offset codes = 8 to 248		5	35	mV
Temperature Coefficient				20	80	ppm FS/°C
VCLAMP						
Clamp Input Bias Current	ICLAMP	1.25 V to 5.0 V		200		nA
Clamp Input Voltage Range			1.25		5.0	V
OUTPUT STAGE						
Short-Circuit Current	I_{SC}	Source		−45	−25	mA
	I_{SC}	Sink	40	55		mA
Output Voltage, Low	V_{OL}	R_L = 10 kΩ to 5 V			30	mV
Output Voltage, High	V_{OH}	R_L = 10 kΩ to 0 V	4.94			V
POWER SUPPLY						
Supply Current	I_{SY}	VPOS = VNEG = 2.5 V, VDAC code = 128, VOUT = 2.5 V		1.8		mA
Power Supply Rejection Ratio	PSRR	VDD = 2.7 V to 5.5 V	105	125		dB
DYNAMIC PERFORMANCE						
Gain Bandwidth Product	GBP	First gain stage, T_A = 25°C		2		MHz
		Second gain stage, T_A = 25°C		8		MHz
Settling Time	t_s	To 0.1%, 4 V output step		8		μs
NOISE PERFORMANCE						
Input Referred Noise		f = 1 kHz, T_A = 25°C		32		nV/√Hz
Low Frequency Noise	e_n p-p	f = 0.1 Hz to 10 Hz, T_A = 25°C		0.5		μV p-p
Total Harmonic Distortion	THD	V_{IN} = 16.75 mV rms, f = 1 kHz, T_A = 25°C		−100		dB
DIGITAL INTERFACE						
Input Current				2		μA
DIGIN Pulse Width to Load 0	tw_0	T_A = 25°C	0.05		10	μs
DIGIN Pulse Width to Load 1	tw_1	T_A = 25°C	50			μs
Time Between Pulses at DIGIN	tw_s	T_A = 25°C	10			μs
DIGIN Low		T_A = 25°C			0.2 × VDD	V
DIGIN High		T_A = 25°C	0.8 × VDD			V
DIGOUT Logic 0		T_A = 25°C			0.2 × VDD	V
DIGOUT Logic 1		T_A = 25°C	0.8 × VDD			V

VDD = 2.7 V, VSS = 0.0 V, V_{CM} = 1.35 V, VOUT = 1.35 V, gain = 28, T_A = −40°C to +125°C, unless otherwise specified.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT STAGE						
Input Offset Voltage	V_{OS}			2	12	µV
Input Offset Voltage Drift	T_CV_{OS}				65	nV/°C
Input Bias Current	I_B		10	18	25	nA
Input Offset Current	I_{OS}			1	4	nA
Input Voltage Range			0.6		1.5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0.9 V to 1.5 V, A_V = 28	71	82		dB
		V_{CM} = 0.9 V to 1.5 V, A_V = 1300	96	112		dB
Linearity		VOUT = 0.2 V to 1.8 V		20		ppm
		VOUT = 0.2 V to 2.5 V		1000		ppm
Differential Gain Accuracy		Second stage gain = 10 to 250			1.6	%
Differential Gain Temperature Coefficient		Second stage gain = 10 to 250		15	40	ppm/°C
DAC						
Accuracy		Offset codes = 8 to 248		0.7	0.8	%
Ratiometricity		Offset codes = 8 to 248		50		ppm
Output Offset		Offset codes = 8 to 248		5	35	mV
Temperature Coefficient				20	80	ppm FS/°C
VCLAMP						
Input Bias Current	ICLAMP	1.25 V to 2.7 V		200		nA
Input Voltage Range			1.25		2.7	V
OUTPUT STAGE						
Short-Circuit Current	I_{SC}	Source		−12	−7	mA
		Sink	15	25		mA
Output Voltage, Low	V_{OL}	R_L = 10 kΩ to 2.7 V			30	mV
Output Voltage, High	V_{OH}	R_L = 10 kΩ to 0 V	2.64			V
POWER SUPPLY						
Supply Current	I_{SY}	VPOS = VNEG = 1.35 V, VDAC code = 128, VOUT = 1.35 V		1.8		mA
Power Supply Rejection Ratio	PSRR	VDD = 2.7 V to 5.5 V	105	125		dB
DYNAMIC PERFORMANCE						
Gain Bandwidth Product	GBP	First gain stage, T_A = 25°C		2		MHz
		Second gain stage, T_A = 25°C		8		MHz
Settling Time	t_s	To 0.1%, 2 V output step, T_A = 25°C		8		µs
NOISE PERFORMANCE						
Input Referred Noise		f = 1 kHz		32		nV/√Hz
Low Frequency Noise	e_n p-p	f = 0.1 Hz to 10 Hz		0.5		µV p-p
Total Harmonic Distortion	THD	V_{IN} = 16.75 mV rms, f = 1 kHz		−100		dB
DIGITAL INTERFACE						
Input Current				2		µA
DIGIN Pulse Width to Load 0	tw_0	T_A = 25°C	0.05		10	µs
DIGIN Pulse Width to Load 1	tw_1	T_A = 25°C	50			µs
Time Between Pulses at DIGIN	tw_s	T_A = 25°C	10			µs
DIGIN Low		T_A = 25°C			0.2 × VDD	V
DIGIN High		T_A = 25°C	0.8 × VDD			V
DIGOUT Logic 0		T_A = 25°C			0.2 × VDD	V
DIGOUT Logic 1		T_A = 25°C	0.8 × VDD			V

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	6 V
Input Voltage	VSS − 0.3 V to VDD + 0.3 V
Differential Input Voltage[1]	±6.0 V
Output Short-Circuit Duration to VSS or VDD	Indefinite
ESD (Human Body Model)	2000 V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +125°C
Junction Temperature Range	−65°C to +150°C
Lead Temperature	300°C

[1] Differential input voltage is limited to ±5.0 V or ± the supply voltage, whichever is less.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

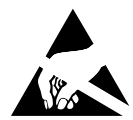
THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for LFCSP packages.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead SOIC (R)	158	43	°C/W
16-Lead LFCSP (CP)	44	31.5	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

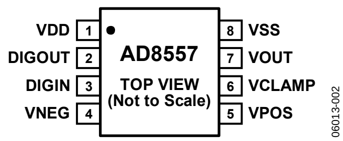


Figure 2. 8-Lead SOIC Pin Configuration

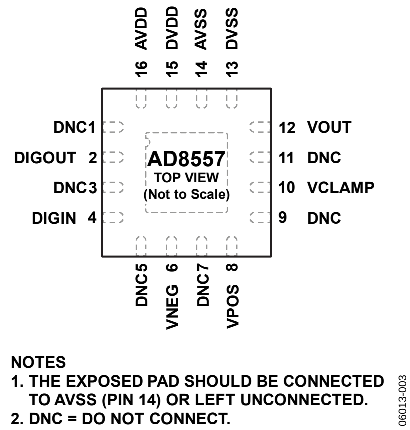


Figure 3. 16-Lead LFCSP Pin Configuration

Table 5. Pin Function Descriptions

Pin No.			
SOIC	**LFCSP**	**Mnemonic**	**Description**
1	Not applicable	VDD	Positive Supply Voltage.
2	2	DIGOUT	Digital Output. In read mode, this pin functions as a digital output.
3	4	DIGIN	Digital Input.
4	6	VNEG	Negative Amplifier Input (Inverting Input).
5	8	VPOS	Positive Amplifier Input (Noninverting Input).
6	10	VCLAMP	Set Clamp Voltage at Output.
7	12	VOUT	Amplifier Output.
8	Not applicable	VSS	Negative Supply Voltage.
Not applicable	13	DVSS	Negative Supply Voltage.
Not applicable	14	AVSS	Negative Supply Voltage.
Not applicable	15	DVDD	Positive Supply Voltage.
Not applicable	16	AVDD	Positive Supply Voltage.
Not applicable	1, 3, 5, 7, 9, 11	DNC	Do Not Connect. Do not connect to these pins.
Not applicable	0	EPAD	Exposed Pad. The exposed pad should be connected to AVSS (Pin 14) or left unconnected.

TYPICAL PERFORMANCE CHARACTERISTICS

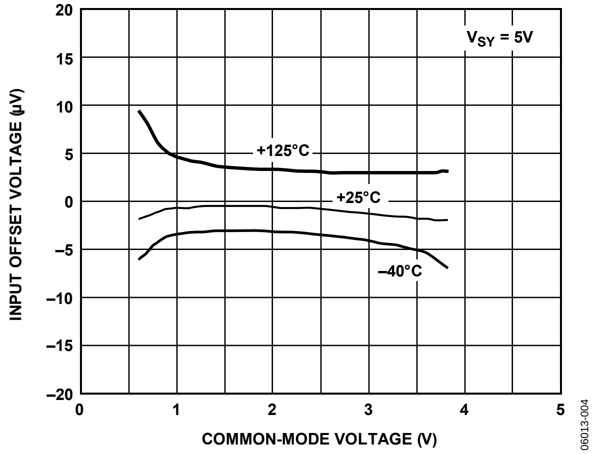


Figure 4. Input Offset Voltage vs. Common-Mode Voltage, V_{SY} = 5 V

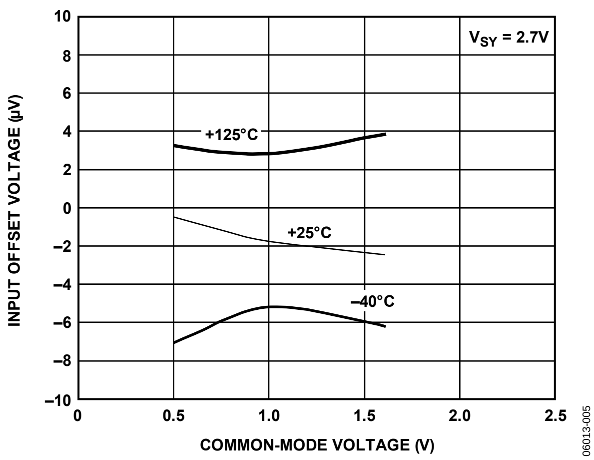


Figure 5. Input Offset Voltage vs. Common-Mode Voltage, V_{SY} = 2.7 V

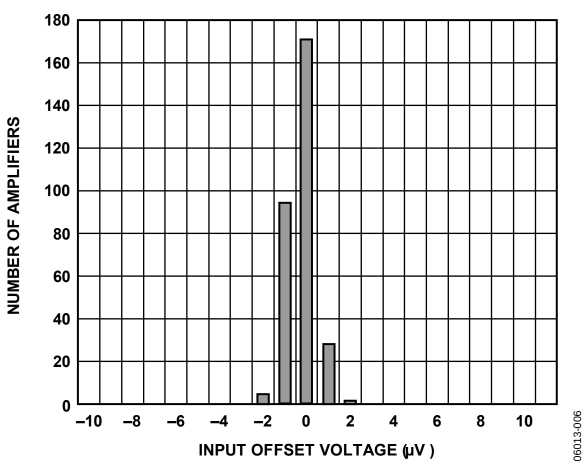


Figure 6. Input Offset Voltage Distribution, V_{SY} = 5 V

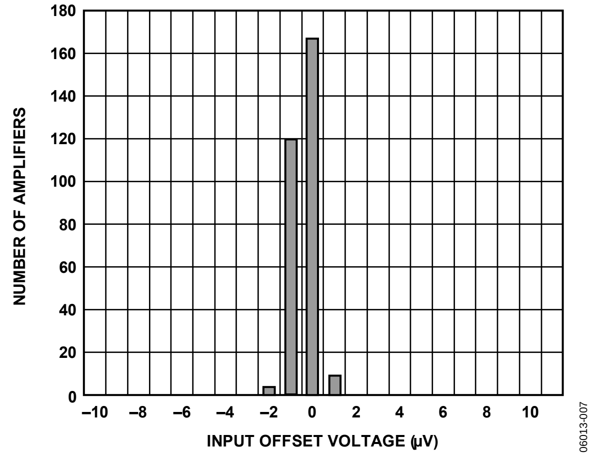


Figure 7. Input Offset Voltage Distribution, V_{SY} = 2.7 V

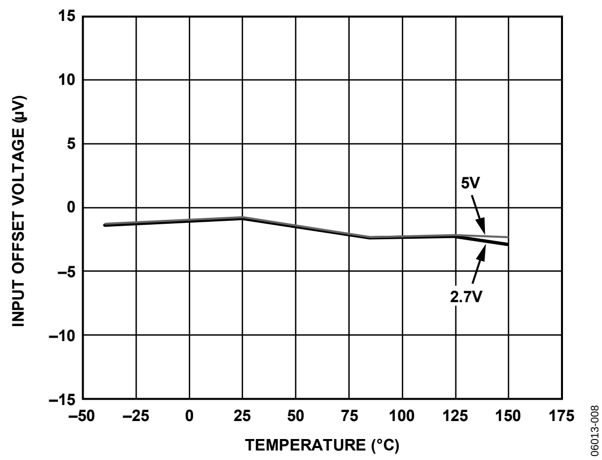


Figure 8. Input Offset Voltage vs. Temperature

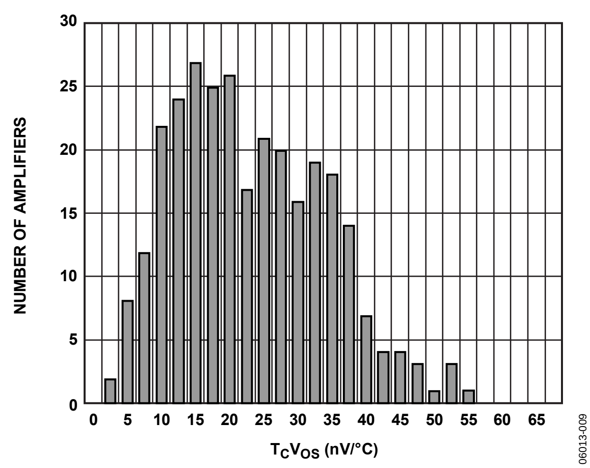


Figure 9. T_CV_{OS} at V_{SY} = 5 V, −40°C ≤ T_A ≤ +125°C

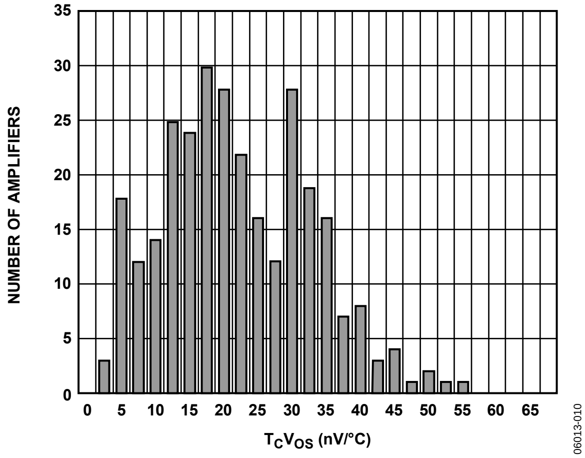


Figure 10. T_CV_{OS} at V_{SY} = 2.7 V, −40°C ≤ T_A ≤ +125°C

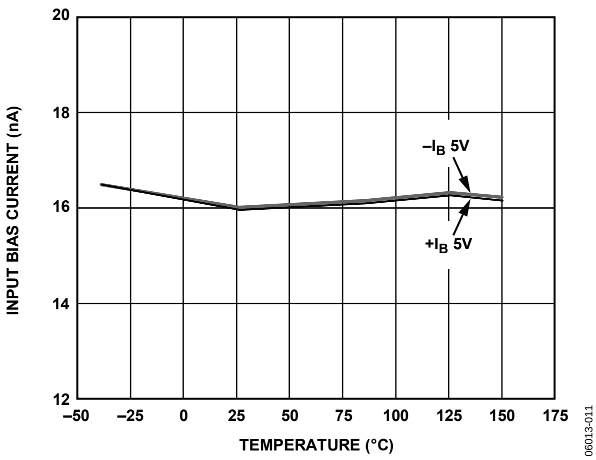


Figure 11. Input Bias Current at VPOS, VNEG vs. Temperature, V_{SY} = 5 V, 2.7 V

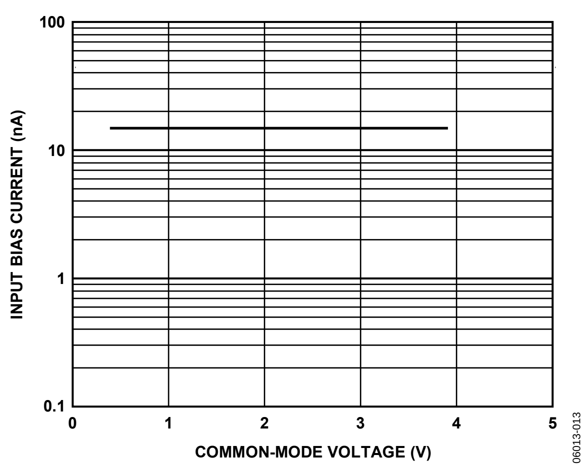


Figure 12. Input Bias Current at VPOS, VNEG vs. Common-Mode Voltage, T_A = 25°C

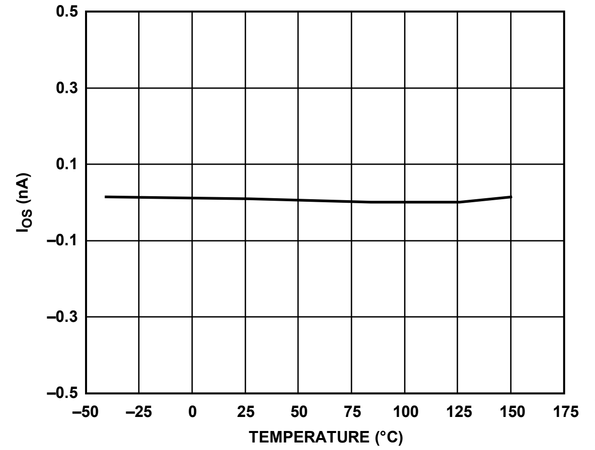


Figure 13. Input Offset Current vs. Temperature

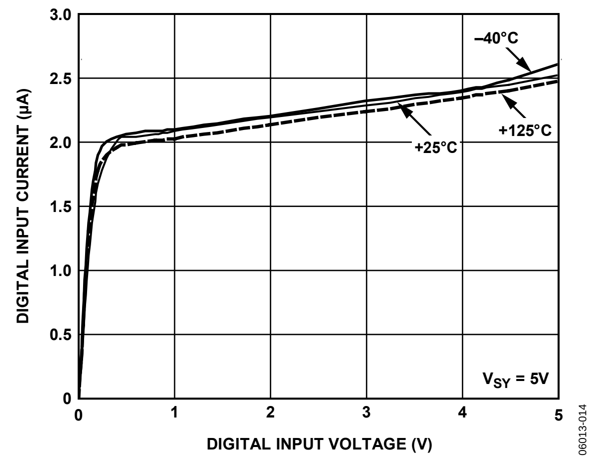


Figure 14. Digital Input Current vs. Digital Input Voltage (Pin 4)

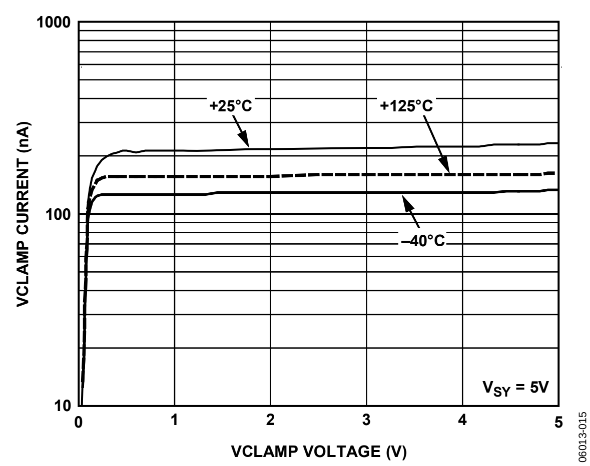


Figure 15. VCLAMP Current over Temperature at V_{SY} = 5 V vs. VCLAMP Voltage

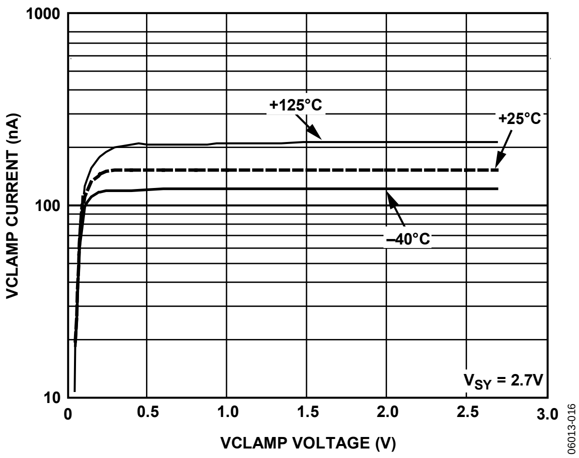


Figure 16. VCLAMP Current over Temperature at V_{SY} = 2.7 V vs. VCLAMP Voltage

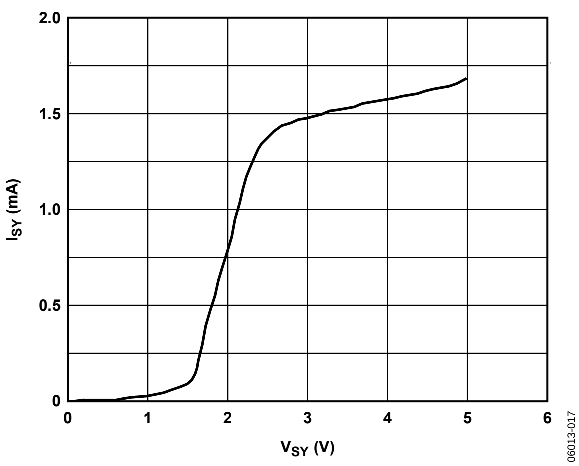


Figure 17. Supply Current (I_{SY}) vs. Supply Voltage

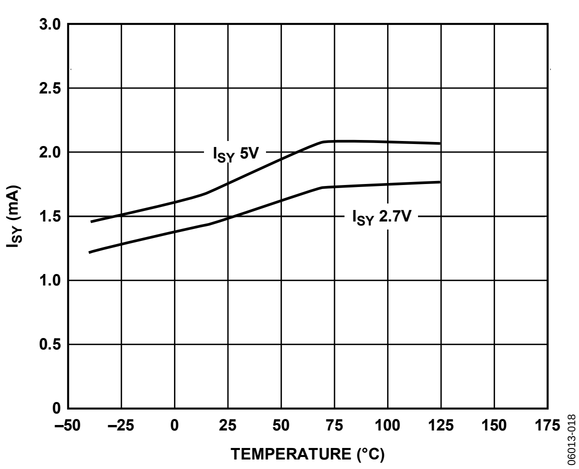


Figure 18. Supply Current (I_{SY}) vs. Temperature

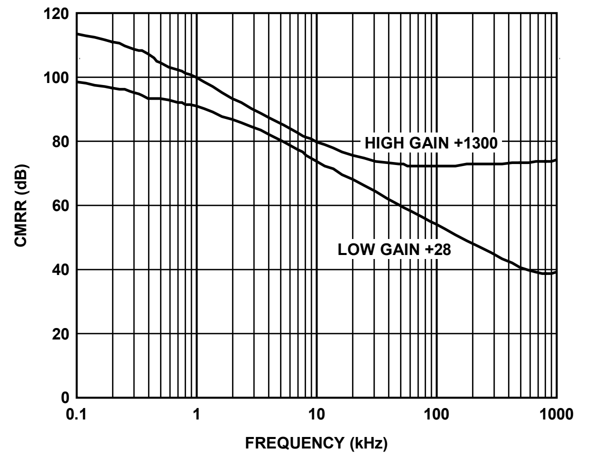


Figure 19. CMRR vs. Frequency, V_{SY} = 5 V

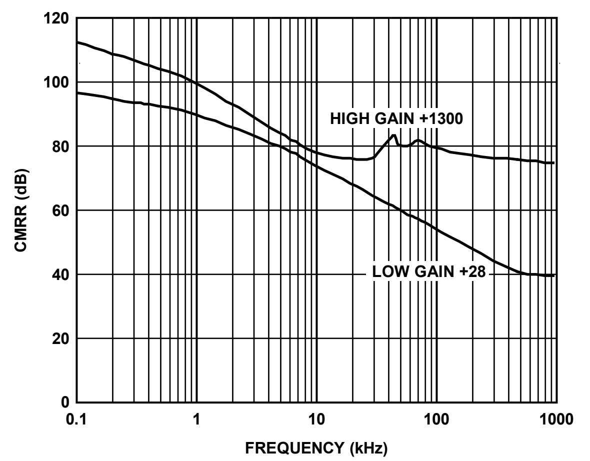


Figure 20. CMRR vs. Frequency, V_{SY} = 2.7 V

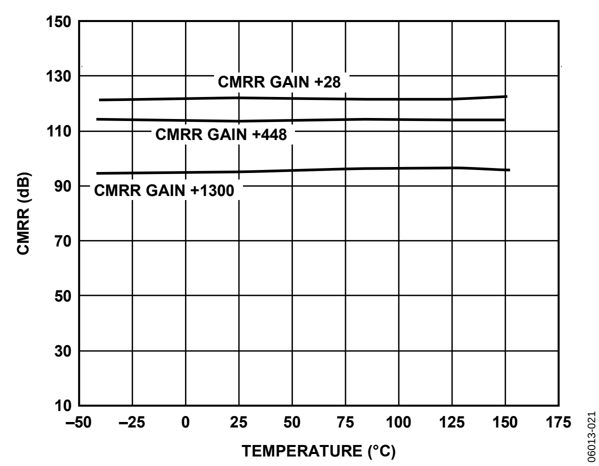


Figure 21. CMRR vs. Temperature at Different Gains, V_{SY} = 5 V

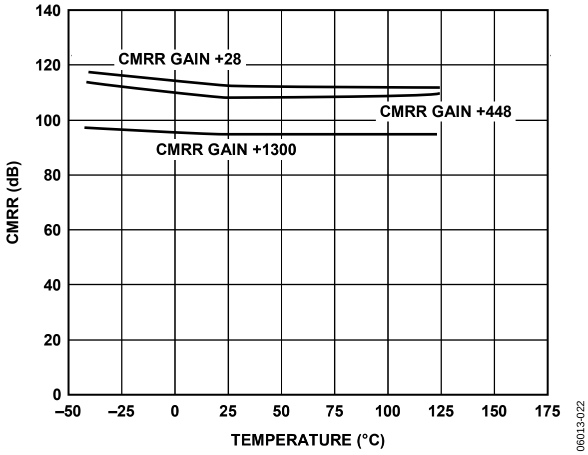


Figure 22. CMRR vs. Temperature at Different Gains, V_{SY} = 2.7 V

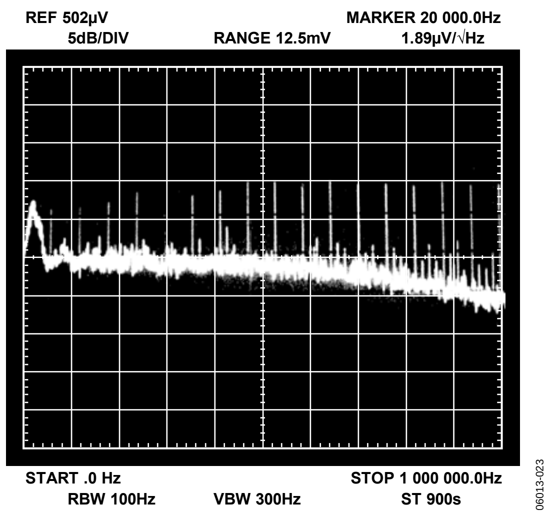


Figure 23. Input Voltage Noise Density vs. Frequency (0 Hz to 1000 kHz)

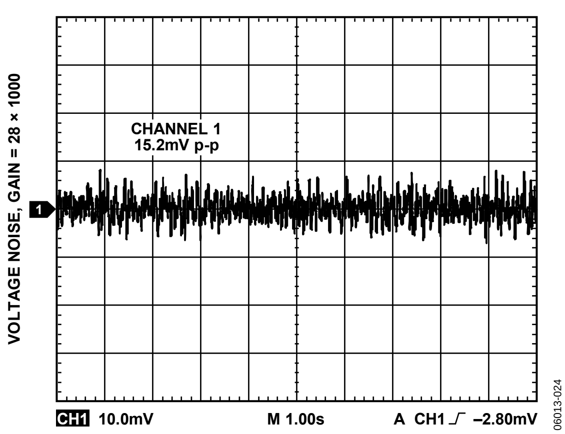


Figure 24. Low Frequency Input Voltage Noise, 0.1 Hz to 10 Hz, V_{SY} = 5 V

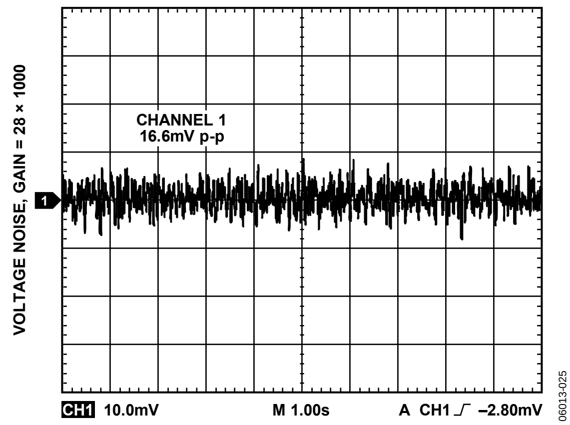


Figure 25. Low Frequency Input Voltage Noise 0.1 Hz to 10 Hz, V_{SY} = 2.7 V

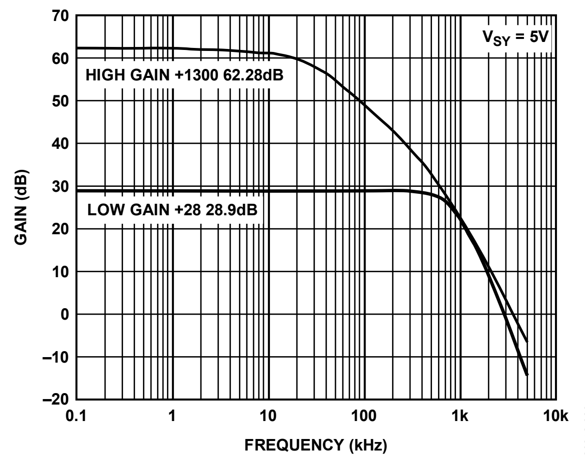


Figure 26. Closed-Loop Gain vs. Frequency Measured at Output Pin, V_{SY} = 5 V

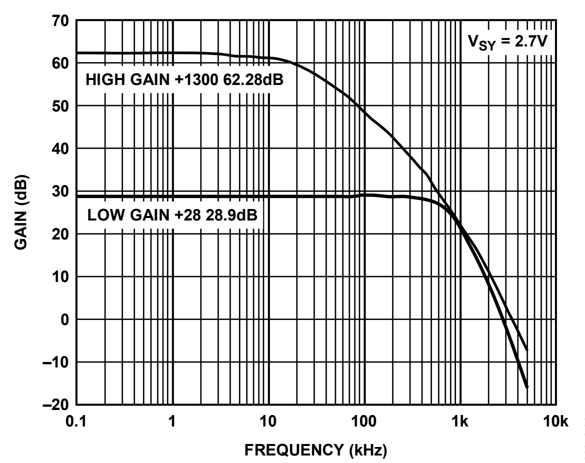


Figure 27. Closed-Loop Gain vs. Frequency Measured at Output Pin, V_{SY} = 2.7 V

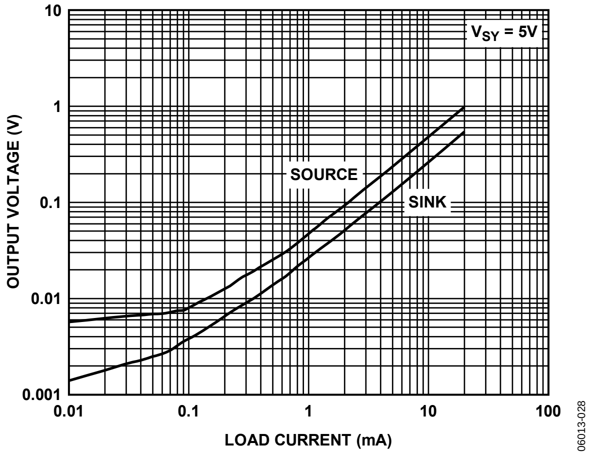


Figure 28. Output Voltage to Supply Rail vs. Load Current

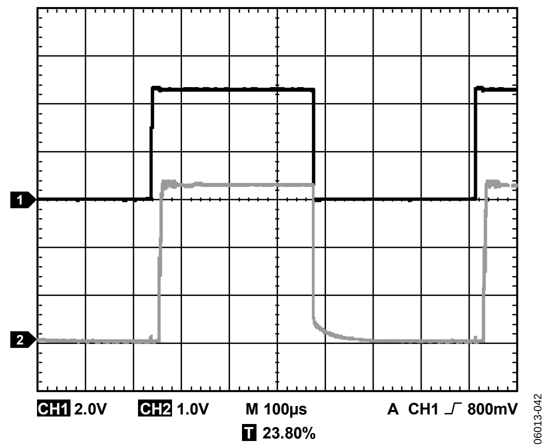


Figure 31. Power-On Response at 125°C

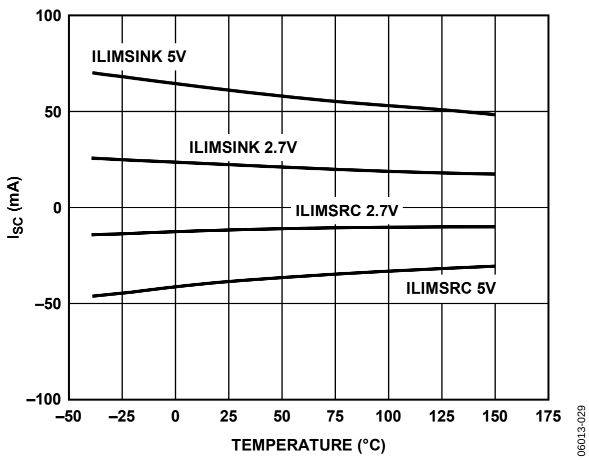


Figure 29. Output Short-Circuit vs. Temperature

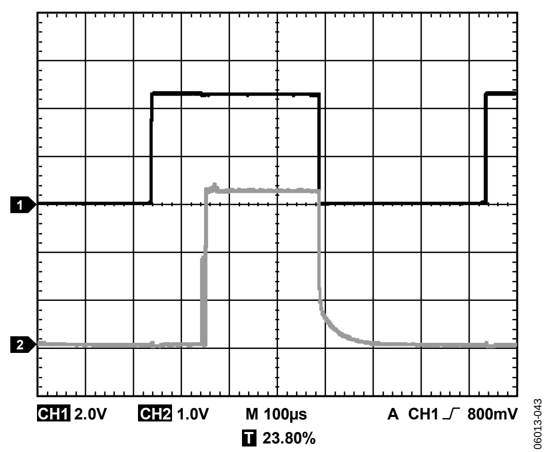


Figure 32. Power-On Response at −40°C

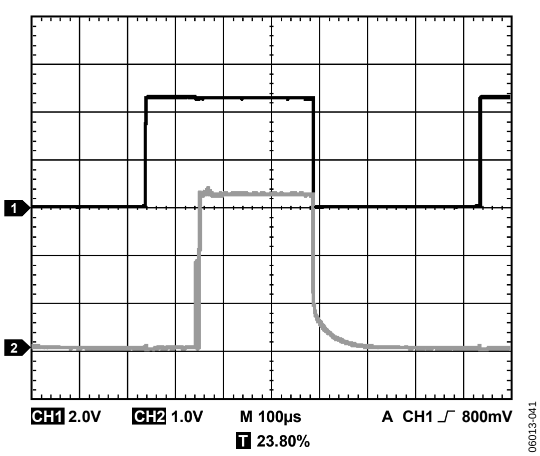


Figure 30. Power-On Response at 25°C

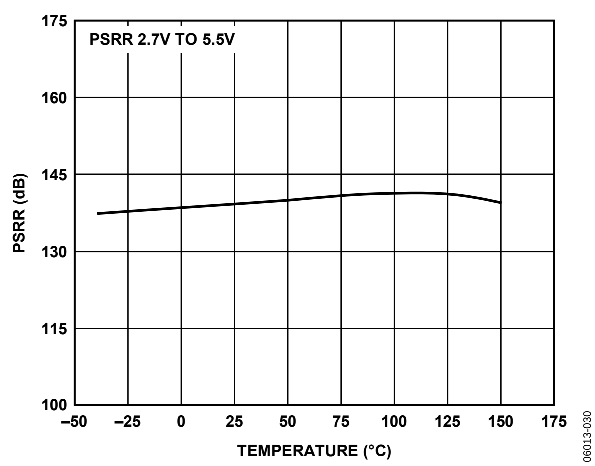


Figure 33. PSRR vs. Temperature

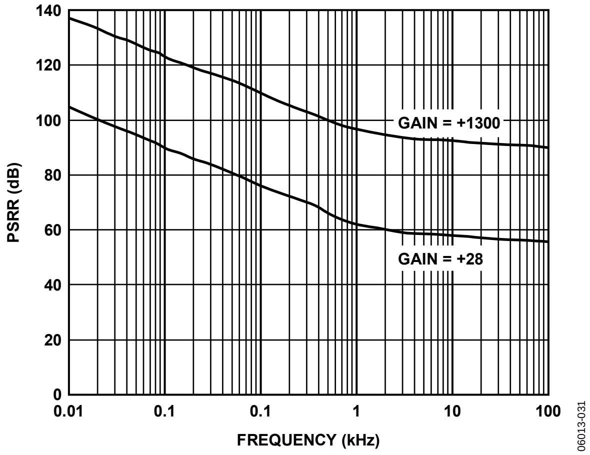


Figure 34. PSRR vs. Frequency

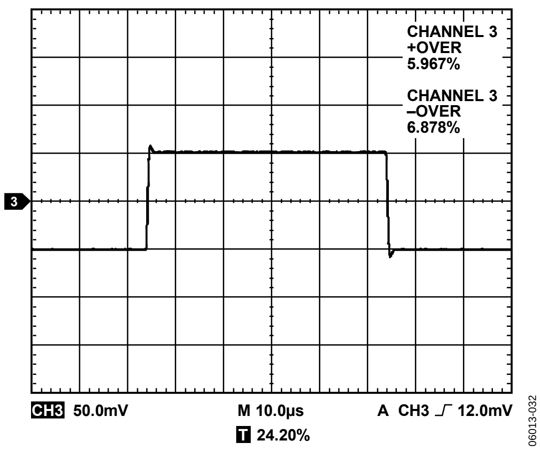


Figure 35. Small Signal Response, V_{SY} = 5 V, C_L = 100 pF

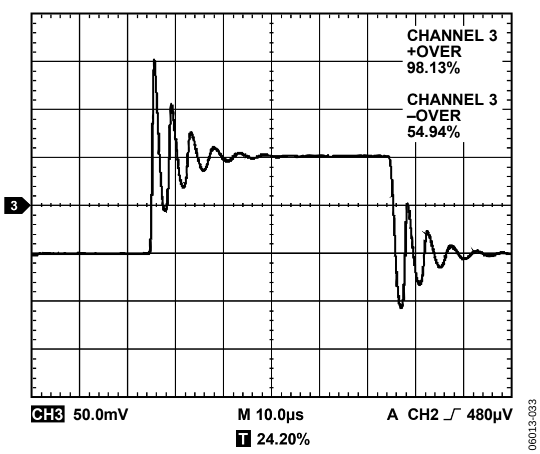


Figure 36. Small Signal Response, V_{SY} = 5 V, C_L = 15 nF

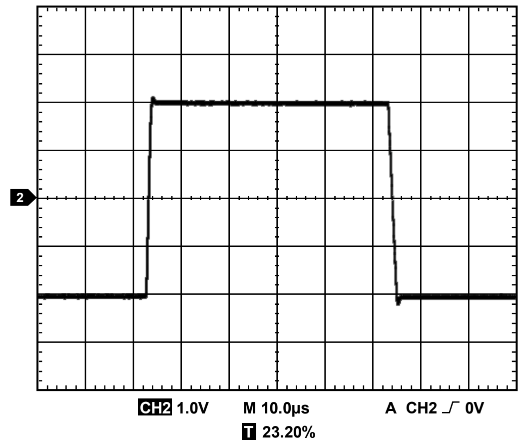


Figure 37. Large Signal Response, C_L = 0 pF

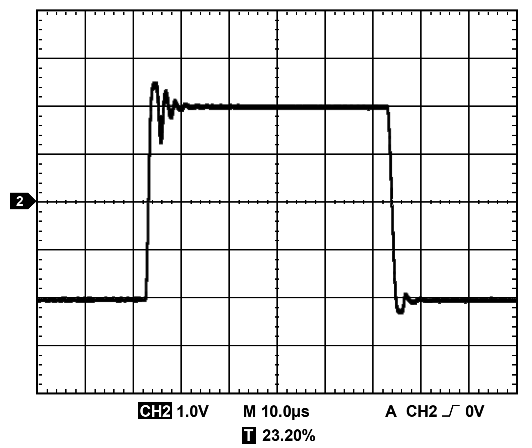


Figure 38. Large Signal Response, C_L = 5 nF

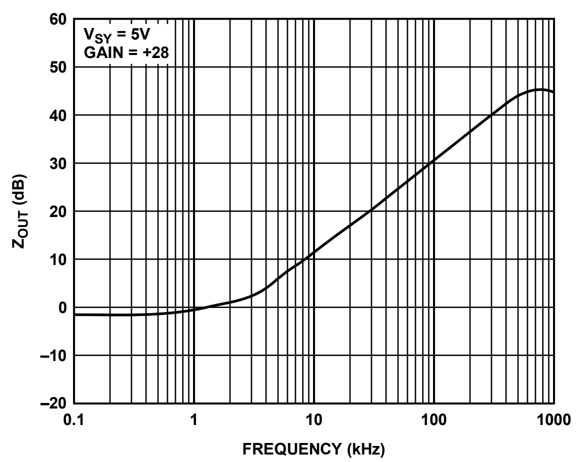


Figure 39. Output Impedance vs. Frequency

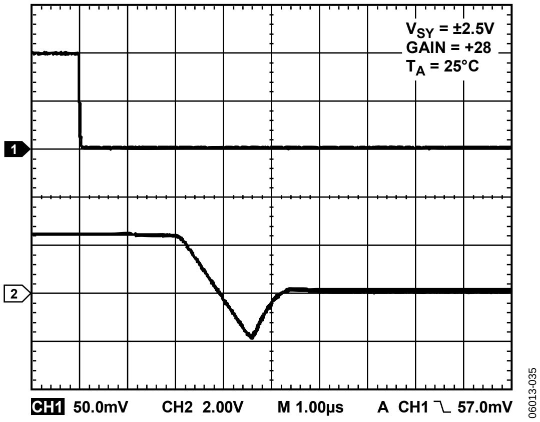


Figure 40. Positive Overload Recovery

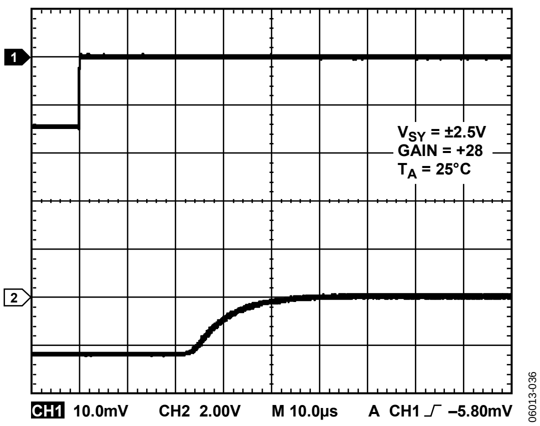


Figure 41. Negative Overload Recovery

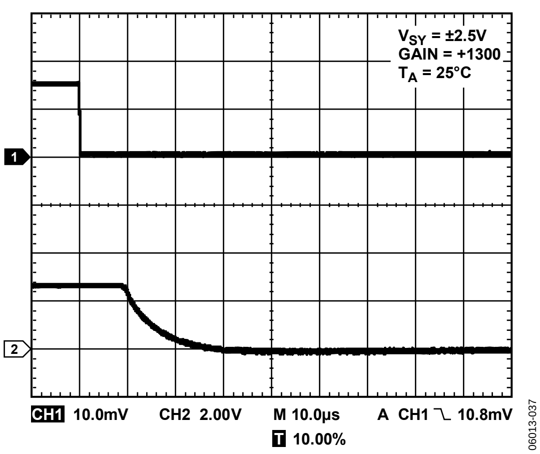


Figure 42. Negative Overload Recovery (Gain = 1300)

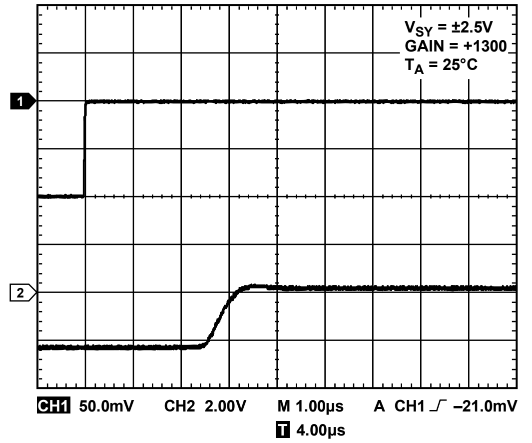


Figure 43. Positive Overload Recovery (Gain = 1300)

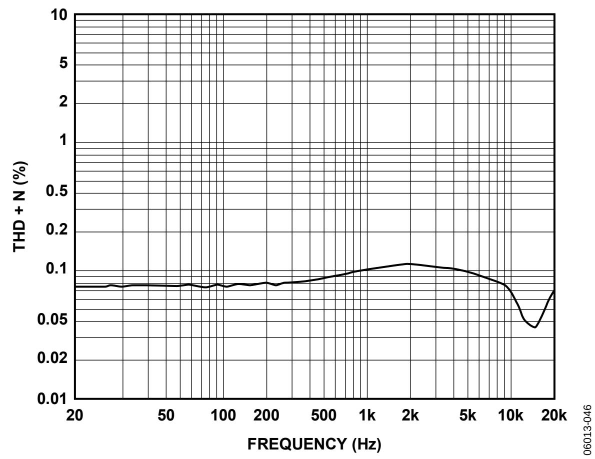


Figure 44. THD + N vs. Frequency

THEORY OF OPERATION

A1, A2, R1, R2, R3, P1, and P2 form the first gain stage of the differential amplifier. A1 and A2 are auto-zeroed op amps that minimize input offset errors. P1 and P2 are digital potentiometers, guaranteed to be monotonic. Programming P1 and P2 allows the first stage gain to be varied from 2.8 to 5.2 with 7-bit resolution (see Table 6 and Equation 1), giving a fine gain adjustment resolution of 0.49%. Because R1, R2, R3, P1, and P2 each have a similar temperature coefficient, the first stage gain temperature coefficient is lower than 100 ppm/°C.

$$GAIN1 \approx 2.8 \times \left(\frac{5.2}{2.8}\right)^{\left(\frac{Code}{127}\right)} \quad (1)$$

A3, R4, R5, R6, R7, P3, and P4 form the second gain stage of the differential amplifier. A3 is an auto-zeroed op amp that minimizes input offset errors and also includes an output buffer. P3 and P4 are digital potentiometers, which allow the second stage gain to be varied from 10 to 250 in eight steps (see Table 7). R4, R5, R6, R7, P3, and P4 each have a similar temperature coefficient, so the second stage gain temperature coefficient is lower than 100 ppm/°C. The output stage of A3 is supplied from a buffered version of VCLAMP instead of VDD, allowing the positive swing to be limited.

A4 implements a voltage buffer, which provides the positive supply to the output stage of A3. Its function is to limit VOUT to a maximum value, useful for driving analog-to-digital converters (ADC) operating on supply voltages lower than VDD. The input to A4, VCLAMP, has a very high input resistance. It should be connected to a known voltage and not be left floating. However, the high input impedance allows the clamp voltage to be set using a high impedance source, such as a potential divider. If the maximum value of VOUT does not need to be limited, VCLAMP should be connected to VDD.

An 8-bit digital-to-analog converter (DAC) is used to generate a variable offset for the amplifier output. This DAC is guaranteed to be monotonic. To preserve the ratiometric nature of the input signal, the DAC references are driven from VSS and VDD, and the DAC output can swing from VSS (Code 0) to VDD (Code 255). The 8-bit resolution is equivalent to 0.39% of the difference between VDD and VSS, for example, 19.5 mV with a 5 V supply. The DAC output voltage (VDAC) is given approximately by

$$VDAC \approx \left(\frac{Code + 0.5}{256}\right)(VDD - VSS) + VSS \quad (2)$$

where the temperature coefficient of *VDAC* is lower than 200 ppm/°C.

The amplifier output voltage (VOUT) is given by

$$VOUT = GAIN(VPOS - VNEG) + VDAC \quad (3)$$

where *GAIN* is the product of the first and second stage gains.

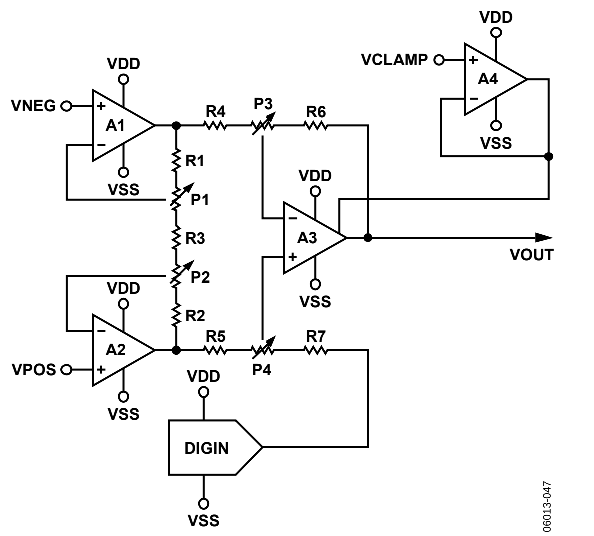


Figure 45. Functional Schematic

GAIN VALUES

Table 6. First Stage Gain vs. First Stage Gain Code

First Stage Gain Code	First Stage Gain	First Stage Gain Code	First Stage Gain	First Stage Gain Code	First Stage Gain	First Stage Gain Code	First Stage Gain
0	2.800	32	3.273	64	3.825	96	4.471
1	2.814	33	3.289	65	3.844	97	4.493
2	2.827	34	3.305	66	3.863	98	4.515
3	2.841	35	3.321	67	3.881	99	4.537
4	2.855	36	3.337	68	3.900	100	4.559
5	2.869	37	3.353	69	3.919	101	4.581
6	2.883	38	3.370	70	3.939	102	4.603
7	2.897	39	3.386	71	3.958	103	4.626
8	2.911	40	3.403	72	3.977	104	4.649
9	2.926	41	3.419	73	3.997	105	4.671
10	2.940	42	3.436	74	4.016	106	4.694
11	2.954	43	3.453	75	4.036	107	4.717
12	2.969	44	3.470	76	4.055	108	4.740
13	2.983	45	3.487	77	4.075	109	4.763
14	2.998	46	3.504	78	4.095	110	4.786
15	3.012	47	3.521	79	4.115	111	4.810
16	3.027	48	3.538	80	4.135	112	4.833
17	3.042	49	3.555	81	4.156	113	4.857
18	3.057	50	3.573	82	4.176	114	4.881
19	3.072	51	3.590	83	4.196	115	4.905
20	3.087	52	3.608	84	4.217	116	4.929
21	3.102	53	3.625	85	4.237	117	4.953
22	3.117	54	3.643	86	4.258	118	4.977
23	3.132	55	3.661	87	4.279	119	5.001
24	3.147	56	3.679	88	4.300	120	5.026
25	3.163	57	3.697	89	4.321	121	5.050
26	3.178	58	3.715	90	4.342	122	5.075
27	3.194	59	3.733	91	4.363	123	5.100
28	3.209	60	3.751	92	4.384	124	5.125
29	3.225	61	3.770	93	4.406	125	5.150
30	3.241	62	3.788	94	4.427	126	5.175
31	3.257	63	3.806	95	4.449	127	5.200

Table 7. Second Stage Gain and Gain Ranges vs. Second Stage Gain Code

Second Stage Gain Code	Second Stage Gain	Minimum Combined Gain	Maximum Combined Gain
0	10	28.0	52.0
1	16	44.8	83.2
2	25	70.0	130.0
3	40	112.0	208.0
4	63	176.4	327.6
5	100	280.0	520.0
6	160	448.0	832.0
7	250	700.0	1300.0

OPEN WIRE FAULT DETECTION

The inputs to A1 and A2, VNEG and VPOS, each have a comparator to detect whether VNEG or VPOS exceeds a threshold voltage, nominally VDD − 1.1 V. If VNEG > (VDD − 1.1 V) or VPOS > (VDD − 1.1 V), VOUT is clamped to VSS. The output current limit circuit is disabled in this mode, but the maximum sink current is approximately 10 mA when VDD = 5 V. The inputs to A1 and A2, VNEG and VPOS, are also pulled up to VDD by currents IP1 and IP2. These are both nominally 16 nA and matched to within 3 nA. If the inputs to A1 or A2 are accidentally left floating, as with an open wire fault, IP1 and IP2 pull them to VDD, which would cause VOUT to swing to VSS, allowing this fault to be detected. It is not possible to disable IP1 and IP2, nor the clamping of VOUT to VSS, when VNEG or VPOS approaches VDD.

SHORTED WIRE FAULT DETECTION

The AD8557 provides fault detection in the case where VPOS, VNEG, or VCLAMP shorts to VDD and VSS. Figure 46 shows the voltage regions at VPOS, VNEG, and VCLAMP that trigger an error condition. When an error condition occurs, the VOUT pin is shorted to VSS. Table 8 lists the voltage levels shown in Figure 46.

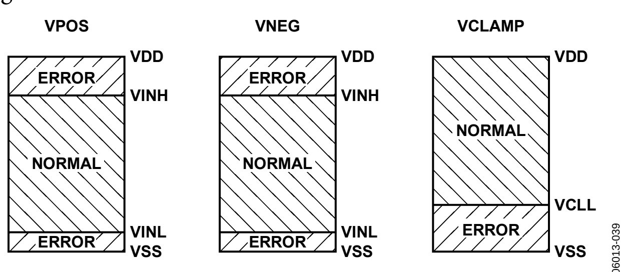


Figure 46. Voltage Regions at VPOS, VNEG, and VCLAMP that Trigger a Fault Condition

Table 8. Typical VINL, VINH, and VCLL Values (VDD = 5 V)

Voltage	Min (V)	Max (V)	VOUT Condition
VINH	3.9	4.2	Short to VDD fault detection
VINL	0.195	0.55	Short to VSS fault detection
VCLL	1.0	1.2	Short to VSS fault detection

FLOATING VPOS, VNEG, OR VCLAMP FAULT DETECTION

A floating fault condition at the VPOS, VNEG, or VCLAMP pins is detected by using a low current to pull a floating input into an error voltage range, defined in the previous section. In this way, the VOUT pin is shorted to VSS when a floating input is detected. Table 9 lists the currents used.

Table 9. Floating Fault Detection at VPOS, VNEG, and VCLAMP

Pin	Typical Current	Goal of Current
VPOS	16 nA pull-up	Pull VPOS above VINH
VNEG	16 nA pull-up	Pull VNEG above VINH
VCLAMP	0.2 μA pull-down	Pull VCLAMP below VCLL

DEVICE PROGRAMMING

Digital Interface

The digital interface allows the first stage gain, second stage gain, and output offset to be adjusted and allows desired values for these parameters to be permanently stored by selectively blowing polysilicon fuses. To minimize pin count and board space, a single-wire digital interface is used. The digital input pin, DIGIN, has hysteresis to minimize the possibility of inadvertent triggering with slow signals. It also has a pull-down current sink to allow it to be left floating when programming is not being performed. The pull-down ensures inactive status of the digital input by forcing a dc low voltage on DIGIN.

A short pulse at DIGIN from low to high and back to low again, such as between 50 ns and 10 μs long, loads a 0 into a shift register. A long pulse at DIGIN, such as 50 μs or longer, loads a 1 into the shift register. The time between pulses should be at least 10 μs. Assuming VSS = 0 V, voltages at DIGIN between VSS and 0.2 × VDD are recognized as a low, and voltages at DIGIN between 0.8 × VDD and VDD are recognized as a high. A timing diagram example, Figure 47, shows the waveform for entering Code 010011 into the shift register.

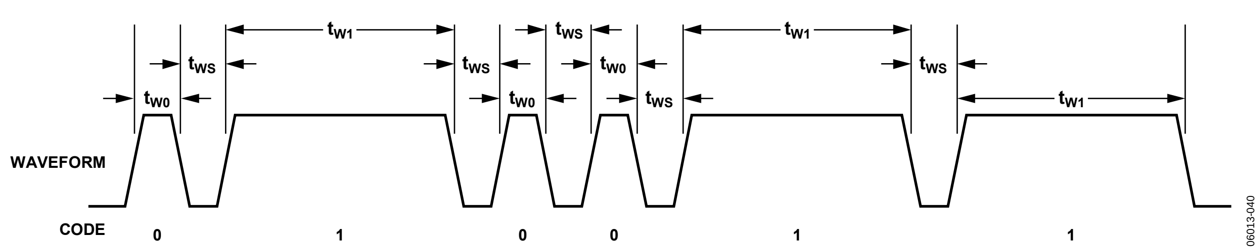


Figure 47. Timing Diagram for Code 010011

Table 10. Timing Specifications

Timing Parameter	Description	Specification
t_{W0}	Pulse width for loading 0 into shift register	Between 50 ns and 10 µs
t_{W1}	Pulse width for loading 1 into shift register	≥50 µs
t_{WS}	Width between pulses	≥10 µs

Table 11. 38-Bit Serial Word Format

Field No.	Bits	Description
0	0 to 11	12-bit start of packet 1000 0000 0001
1	12 to 13	2-bit function 00: change sense current 01: simulate parameter value 10: program parameter value 11: read parameter value
2	14 to 15	2-bit parameter 00: second stage gain code 01: first stage gain code 10: output offset code 11: other functions
3	16 to 17	2-bit dummy 10
4	18 to 25	8-bit value Parameter 00 (second stage gain code): 3 LSBs used Parameter 01 (first stage gain code): 7 LSBs used Parameter 10 (output offset code): all 8 bits used Parameter 11 (other functions) Bit 0 (LSB): master fuse Bit 1: fuse for production test at Analog Devices
5	26 to 37	12-bit end of packet 0111 1111 1110

A 38-bit serial word is used, divided into 6 fields. Assuming each bit can be loaded in 60 µs, the 38-bit serial word transfers in 2.3 ms. Table 11 summarizes the word format.

Field 0 and Field 5 are the start-of-packet field and end-of-packet field, respectively. Matching the start-of-packet field with 1000 0000 0001 and the end-of-packet field with 0111 1111 1110 ensures that the serial word is valid and enables decoding of the other fields.

Field 3 breaks up the data and ensures that no data combination can inadvertently trigger the start-of-packet and end-of-packet fields. Field 0 should be written first and Field 5 written last.

Within each field, the MSB must be written first and the LSB written last. The shift register features power-on reset to minimize the risk of inadvertent programming; power-on reset occurs when VDD is between 0.7 V and 2.2 V.

Initial State

Initially, all the polysilicon fuses are intact. Each parameter has the value 0 assigned (see Table 12).

Table 12. Initial State Before Programming

Second Stage Gain Code = 0	Second Stage Gain = 10
First stage gain code = 0	First stage gain = 2.8
Output offset code = 0	Output offset = VSS
Master fuse = 0	Master fuse not blown

When power is applied to a device, parameter values are taken either from internal registers, if the master fuse is not blown, or from the polysilicon fuses, if the master fuse is blown. Programmed values have no effect until the master fuse is blown. The internal registers feature power-on reset, so the unprogrammed devices enter a known state after power-up. Power-on reset occurs when VDD is between 0.7 V and 2.2 V.

Simulation Mode

The simulation mode allows any parameter to be temporarily changed. These changes are retained until the simulated value is reprogrammed, the power is removed, or the master fuse is blown. Parameters are simulated by setting Field 1 to 01, selecting the desired parameter in Field 2, and selecting the desired value for the parameter in Field 4. Note that a value of 11 for Field 2 is ignored during the simulation mode. Examples of temporary settings follow:

- Setting the second stage gain code (Parameter 00) to 011 and the second stage gain to 40 produces: 1000 0000 0001 01 00 10 0000 0011 0111 1111 1110
- Setting the first stage gain code (Parameter 01) to 000 1011 and the first stage gain to 4.166 produces: 1000 0000 0001 01 01 10 0000 1011 0111 1111 1110
- A first stage gain of 2.954 with a second stage gain of 40 gives a total gain of 118.16. This gain has a maximum tolerance of 2.5%.
- Set the output offset code (Parameter 10) to 0100 0000 and the output offset to 1.260 V when VDD = 5 V and VSS = 0 V. This output offset has a maximum tolerance of 0.8%: 1000 0000 0001 01 10 10 0100 0000 0111 1111 1110

Programming Mode

Intact fuses give a bit value of 0. Bits with a desired value of 1 need to have the associated fuse blown. Because a relatively large current is needed to blow a fuse, only one fuse can be reliably blown at a time. Thus, a given parameter value may need several 38-bit words to allow reliable programming.

A 5.75 V (±0.25 V) supply is required when blowing fuses to minimize the on resistance of the internal MOS switches that blow the fuse. The power supply voltage must not exceed the absolute maximum rating and must be able to deliver 250 mA of current.

At least 10 μF (tantalum type) of decoupling capacitance is needed across the power pins of the device during programming. The capacitance can be on the programming apparatus as long as it is within 2 inches of the device being programmed. An additional 0.1 μF (ceramic type) in parallel with the 10 μF is recommended within ½ inch of the device being programmed. A minimum period of 1 ms should be allowed for each fuse to blow. There is no need to measure the supply current during programming.

The best way to verify correct programming is to use the read mode to read back the programmed values. Then, remeasure the gain and offset to verify these values. Programmed fuses have no effect on the gain and output offset until the master fuse is blown. After blowing the master fuse, the gain and output offset are determined solely by the blown fuses, and the simulation mode is permanently deactivated.

Parameters are programmed by setting Field 1 to 10, selecting the desired parameter in Field 2, and selecting a single bit with the value 1 in Field 4.

As an example, suppose the user wants to permanently set the second stage gain to 40. Parameter 00 needs to have the value 0000 0011 assigned. Two bits have the value 1, so two fuses need to be blown. Because only one fuse can be blown at a time, this code can be used to blow one fuse:
1000 0000 0001 10 00 10 0000 0010 0111 1111 1110

The MOS switch that blows the fuse closes when the complete packet is recognized, and opens when the start-of-packet, dummy, or end-of-packet fields are no longer valid. After 1 ms, this second code is entered to blow the second fuse:
1000 0000 0001 10 00 10 0000 0001 0111 1111 1110

To permanently set the first stage gain to a nominal value of 2.954, Parameter 01 needs to have the value 000 1011 assigned. Three fuses need to be blown, and the following codes are used, with a 1 ms delay after each code:
1000 0000 0001 10 01 10 0000 1000 0111 1111 1110
1000 0000 0001 10 01 10 0000 0010 0111 1111 1110
1000 0000 0001 10 01 10 0000 0001 0111 1111 1110

To permanently set the output offset to a nominal value of 1.260 V when VDD = 5 V and VSS = 0 V, Parameter 10 needs to have the value 0100 0000 assigned. If one fuse needs to be blown, use the following code:
1000 0000 0001 10 10 10 0100 0000 0111 1111 1110

Finally, to blow the master fuse to deactivate the simulation mode and prevent further programming, use code:
1000 0000 0001 10 11 10 0000 0001 0111 1111 1110

There are a total of 20 programmable fuses. Because each fuse requires 1 ms to blow, and each serial word can be loaded in 2.3 ms, the maximum time needed to program the fuses can be as low as 66 ms.

Read Mode

The values stored by the polysilicon fuses can be sent to the DIGOUT pin to verify correct programming. Normally, the DIGOUT pin is only connected to the second gain stage output. During read mode, however, the DIGOUT pin is also connected to the output of a shift register to allow the polysilicon fuse contents to be read. Because VOUT is a buffered version of DIGOUT, VOUT also outputs a digital signal during read mode.

Read mode is entered by setting Field 1 to 11 and selecting the desired parameter in Field 2. Field 4 is ignored. The parameter value, stored in the polysilicon fuses, is loaded into an internal shift register, and the MSB of the shift register is connected to the DIGOUT pin. Pulses at DIGIN shift out the shift register contents to the DIGOUT pin, allowing the 8-bit parameter value to be read after seven additional pulses; shifting occurs on the falling edge of DIGIN. An eighth pulse at DIGIN disconnects DIGOUT from the shift register and terminates the read mode.

If a parameter value is less than eight bits long, the MSBs of the shift register are padded with 0s.

For example, to read the second stage gain, this code is used:
1000 0000 0001 11 00 10 0000 0000 0111 1111 1110
Because the second stage gain parameter value is only three bits long, the DIGOUT pin has a value of 0 when this code is entered, and remains 0 during four additional pulses at DIGIN. The fifth, sixth, and seventh pulses at DIGIN return the 3-bit value at DIGOUT, the seventh pulse returns the LSB. An eighth pulse at DIGIN terminates the read mode.

Sense Current

A sense current is sent across each polysilicon fuse to determine whether it has been blown. When the voltage across the fuse is less than approximately 1.5 V, the fuse is considered not blown, and Logic 0 is output from the OTP cell. When the voltage across the fuse is greater than approximately 1.5 V, the fuse is considered blown, and Logic 1 is output.

When the AD8557 is manufactured, all fuses have a low resistance. When a sense current is sent through the fuse, a voltage less than 0.1 V is developed across the fuse. This is much lower than 1.5 V, so Logic 0 is output from the OTP cell. When a fuse is electrically blown, it should have a very high resistance. When the sense current is applied to the blown fuse, the voltage across the fuse should be larger than 1.5 V, so Logic 1 is output from the OTP cell.

It is theoretically possible, though very unlikely, for a fuse to be incompletely blown during programming, assuming the required conditions are met. In this situation, the fuse can have a medium resistance, neither low nor high, and a voltage of approximately 1.5 V can be developed across the fuse. Thus, the OTP cell can output Logic 0 or Logic 1, depending on temperature, supply voltage, and other variables.

To detect this undesirable situation, the sense current can be lowered by a factor of 4 using a specific code. The voltage developed across the fuse would then change from 1.5 V to 0.38 V, and the output of the OTP would be a Logic 0 instead of the expected Logic 1 from a blown fuse. Correctly blown fuses would still output a Logic 1. In this way, incorrectly blown fuses can be detected. Another specific code would return the sense current to the normal (larger) value. The sense current cannot be permanently programmed to the low value. When the AD8557 is powered up, the sense current defaults to the high value.

The low sense current code is
1000 0000 0001 00 00 10 XXXX XXX1 0111 1111 1110

The normal (high) sense current code is
1000 0000 0001 00 00 10 XXXX XXX0 0111 1111 1110

Programming Procedure

For reliable fuse programming, it is imperative to follow the programming procedure requirements, especially the proper supply voltage during programming:

1. When programming the AD8557, the temperature of the device must be between 10°C to 40°C.
2. Set VDD and VSS to the desired values in the application. Use simulation mode to test and determine the desired codes for the second stage gain, first stage gain, and output offset. The nominal values for these parameters are shown in Table 6, Table 7, Equation 2, and Equation 3; use the codes corresponding to these values as a starting point. However, because actual parameter values for given codes vary from device to device, some fine tuning is necessary for the best possible accuracy.
3. One way to choose these values is to set the output offset to an approximate value, such as Code 128 for midsupply, to allow the required gain to be determined. Then, set the second stage gain so the minimum first stage gain (Code 0) gives a lower gain than required, and the maximum first stage gain (Code 127) gives a higher gain than required. After choosing the second stage gain, the first stage gain can be chosen to fine tune the total gain. Finally, the output offset can be adjusted to give the desired value. After determining the desired codes for second stage gain, first stage gain, and output offset, the device is ready for permanent programming.
4. Note that once a programming attempt has been made for any fuse, there should be no further attempt to blow that fuse. If a fuse does not program to the expected state, discard the unit. The expected incidence rate of attempted but unblown fuses is very small when following the proper programming procedure and conditions.
5. Set VSS to 0 V and VDD to 5.75 V (±0.25 V). Power supplies should be capable of supplying 250 mA at the required voltage and properly bypassed as described in the Programming Mode section. Use program mode to permanently enter the desired codes for the first stage gain, second stage gain, and output offset. Blow the master fuse to allow the AD8557 to read data from the fuses and to prevent further programming.
6. Set VDD and VSS to the desired values in the application. Use read mode with low sense current followed by high sense current to verify programmed codes.
7. Measure gain and offset to verify correct functionality.

Determining Optimal Gain and Offset Codes

First, determine the desired gain:

1. Determine the desired gain, G_A (using the measurements obtained from the simulation).
2. Use Table 7 to determine G_2, the second stage gain, such that $(2.8 \times 1.05) < (G_A/G_2) < (5.2/1.05)$. This ensures the first and last codes for the first stage gain are not used, thereby allowing enough first stage gain codes within each second stage gain range to adjust for the 3% accuracy.

Next, set the second stage gain:

1. Use the simulation mode to set the second stage gain to G_2.
2. Set the output offset to allow the AD8557 gain to be measured, for example, use Code 128 to set it to midsupply.
3. Use Table 6 or Equation 1 to set the first stage gain code C_{G1}, so the first stage gain is nominally G_A/G_2.
4. Measure the resulting gain (G_B). G_B should be within 3% of G_A.
5. Calculate the first stage gain error (in relative terms) $E_{G1} = G_B/G_A - 1$.
6. Calculate the error (in the number of the first stage gain codes) $C_{EG1} = E_{G1}/0.00489$.
7. Set the first stage gain code to $C_{G1} - C_{EG1}$.
8. Measure the gain (G_C). G_C should be closer to G_A than to G_B.
9. Calculate the error (in relative terms) $E_{G2} = G_C/G_A - 1$.
10. Calculate the error (in the number of the first stage gain codes) $C_{EG2} = E_{G2}/0.00489$.
11. Set the first stage gain code to $C_{G1} - C_{EG1} - C_{EG2}$. The resulting gain should be within one code of G_A.
12. Finally, determine the desired output offset:
13. Determine the desired output offset O_A (using the measurements obtained from the simulation).
14. Use Equation 2 to set the output offset code C_{O1} such that the output offset is nominally O_A.
15. Measure the output offset (O_B). O_B should be within 3% of O_A.
16. Calculate the error (in relative terms) $E_{O1} = O_B/O_A - 1$.
17. Calculate the error (in the number of the output offset codes) $C_{EO1} = E_{O1}/0.00392$.
18. Set the output offset code to $C_{O1} - C_{EO1}$.
19. Measure the output offset (O_C). O_C should be closer to O_A than to O_B.
20. Calculate the error (in relative terms) $E_{O2} = O_C/O_A - 1$.
21. Calculate the error (in the number of the output offset codes) $C_{EO2} = E_{O2}/0.00392$.
22. Set the output offset code to $C_{O1} - C_{EO1} - C_{EO2}$. The resulting offset should be within one code of O_A.

OUTLINE DIMENSIONS

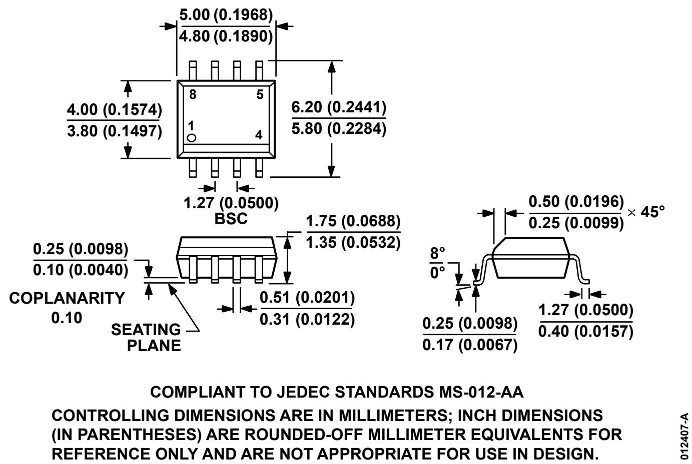


Figure 48. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

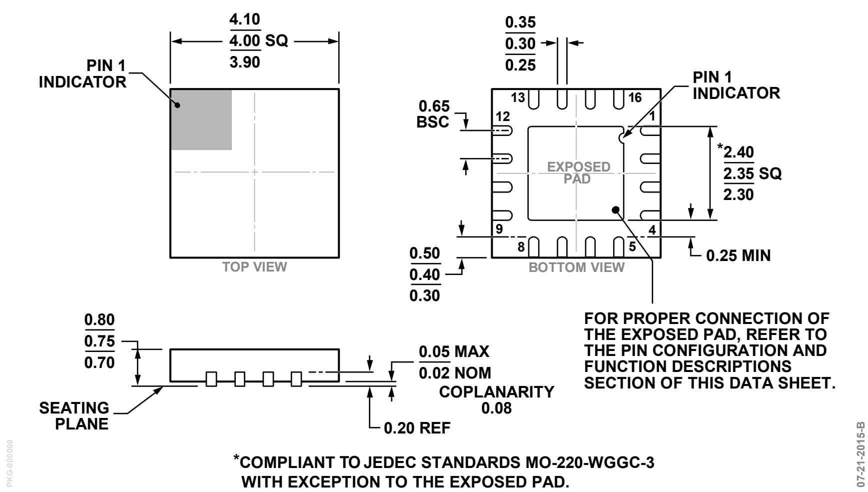


Figure 49. 16-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.75 mm Package Height
(CP-16-20)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD8557ACPZ-R2	−40°C to +125°C	16-Lead LFCSP	CP-16-20
AD8557ACPZ-REEL	−40°C to +125°C	16-Lead LFCSP	CP-16-20
AD8557ACPZ-REEL7	−40°C to +125°C	16-Lead LFCSP	CP-16-20
AD8557ARZ	−40°C to +125°C	8-Lead SOIC_N	R-8
AD8557ARZ-REEL	−40°C to +125°C	8-Lead SOIC_N	R-8
AD8557ARZ-REEL7	−40°C to +125°C	8-Lead SOIC_N	R-8

[1] Z = RoHS Compliant Part.

AUTOMOTIVE PRODUCTS

The AD8557 models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

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