

## CMP401/CMP402

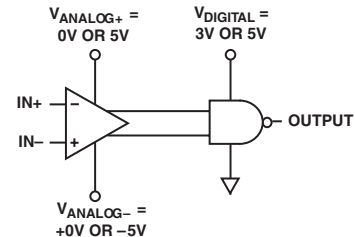
### FEATURES

- 23 ns or 65 ns Propagation Delay
- Single-Supply Operation
- Compatible with 3 V and 5 V Logic
- Separate Input and Output Sections
- Low Power
- Wide Input Range: -5 V to +3.9 V

### APPLICATIONS

- Battery-Operated Instrumentation
- Line Receivers
- Level Translators
- Read Channel Detection

### FUNCTIONAL BLOCK DIAGRAM

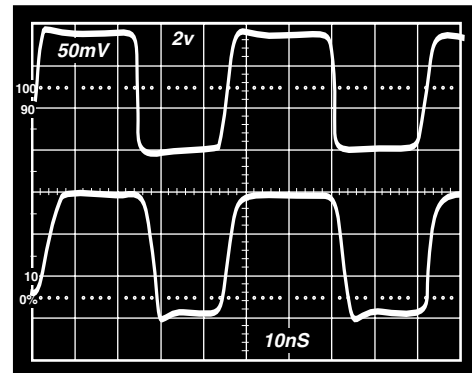


NOTE:  $(V_{ANALOG+}) - (V_{ANALOG-}) \geq 3V$

### GENERAL DESCRIPTION

The CMP401 and CMP402 are 23 ns and 65 ns quad comparators with separate input and output supplies. Separate supplies enable the input stage to be operated from +3 V to as high as  $\pm 6$  V. The output can be supplied with either 3 V or 5 V as determined by the interface logic or available supplies. Independent input and output supplies combined with fast propagation make the CMP401 and CMP402 excellent choices for interfacing to portable instrumentation.

The CMP401 and CMP402 are specified over the extended industrial ( $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ) temperature range. Both are available in narrow 16-lead SOIC surface-mount packages and 16-lead TSSOP.



CMP401: 20 MHz Noninverting Switching,  $V_{IN} = \pm 100$  mV

REV. B

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# CMP401/CMP402—SPECIFICATIONS

## ELECTRICAL SPECIFICATIONS (@ $V_{+ANA} = V_{+DIG} = 5.0\text{ V}$ , $V_{CM} = 0.1\text{ V}$ , $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ , unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
<b>INPUT CHARACTERISTICS</b>						
Offset Voltage <sup>1</sup>	$V_{OS}$	$T_A = 25^{\circ}\text{C}$			3	mV
	$V_{OS}$				4	mV
Hysteresis				2		mV
Input Bias Current	$I_B$	$T_A = 25^{\circ}\text{C}$			3	$\mu\text{A}$
	$I_B$				4	$\mu\text{A}$
Input Offset Current	$I_{OS}$				$\pm 3$	$\mu\text{A}$
Input Common-Mode Voltage Range	$V_{CM}$		0		4.0	V
Common-Mode Rejection	CMRR	$0.1\text{ V} \leq V_{CM} \leq 3.9\text{ V}$	60			dB
Large-Signal Voltage Gain	$A_{VO}$	$R_L = 10\text{ k}\Omega$		10		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			1		$\mu\text{V}/^{\circ}\text{C}$
<b>OUTPUT CHARACTERISTICS</b>						
Output High Voltage	$V_{OH}$	$I_{OH} = -3.2\text{ mA}$	4.6			V
Output Low Voltage	$V_{OL}$	$I_{OL} = 3.2\text{ mA}$			0.2	V
<b>POWER SUPPLY</b>						
Power Supply Rejection Ratio	PSRR	$V_{+ANA}$ and $V_{+DIG}$ 2.7 V to 6 V	60			dB
Analog Supply Current – CMP401	$I_{ANA}$	$T_A = 25^{\circ}\text{C}$			6.5	mA
Digital Supply Current – CMP401	$I_{DIG}$	$V_O = 0\text{ V}$ , $R_L = \infty$ , $T_A = 25^{\circ}\text{C}$			2.0	mA
Analog Supply Current – CMP401	$I_{ANA}$				8.0	mA
Digital Supply Current – CMP401	$I_{DIG}$	$V_O = 0\text{ V}$ , $R_L = \infty$			2.25	mA
Analog Supply Current – CMP402	$I_{ANA}$	$T_A = 25^{\circ}\text{C}$			1.4	mA
Digital Supply Current – CMP402	$I_{DIG}$	$V_O = 0\text{ V}$ , $R_L = \infty$ , $T_A = 25^{\circ}\text{C}$			2.0	mA
Analog Supply Current – CMP402	$I_{ANA}$				1.75	mA
Digital Supply Current – CMP402	$I_{DIG}$	$V_O = 0\text{ V}$ , $R_L = \infty$			2.25	mA
<b>DYNAMIC PERFORMANCE</b>						
Propagation Delay – CMP401	$t_p$	100 mV Step with 20 mV OD $T_A = 25^{\circ}\text{C}$		17	23	ns
	$t_p$	100 mV Step with 5 mV OD $T_A = 25^{\circ}\text{C}$		33		ns
Propagation Delay – CMP402	$t_p$	100 mV Step with 20 mV OD $T_A = 25^{\circ}\text{C}$			30	ns
	$t_p$	100 mV Step with 20 mV OD $T_A = 25^{\circ}\text{C}$		54	65	ns
	$t_p$	100 mV Step with 5 mV OD $T_A = 25^{\circ}\text{C}$		60		ns
	$t_p$	100 mV Step with 20 mV OD			75	ns

## ELECTRICAL SPECIFICATIONS (@ $V_{ANA} = V_{DIG} = 3.0\text{ V}$ , $V_{CM} = 0.1\text{ V}$ , $T_A = 25^{\circ}\text{C}$ , unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
<b>INPUT CHARACTERISTICS</b>						
Offset Voltage <sup>1</sup>	$V_{OS}$				4.5	mV
Input Common-Mode Voltage Range	$V_{CM}$		0		2.0	V
Input Differential Voltage Range	$V_{DIFF}$		$\pm 2.0$			V
Common-Mode Rejection	CMRR	$0.1\text{ V} \leq V_{CM} \leq 1.9\text{ V}$	60			dB
<b>OUTPUT CHARACTERISTICS</b>						
Output High Voltage	$V_{OH}$	$I_{OH} = -3.2\text{ mA}$	2.6			V
Output Low Voltage	$V_{OL}$	$I_{OL} = 3.2\text{ mA}$			0.25	V
<b>POWER SUPPLY</b>						
Power Supply Rejection Ratio	PSRR	$V_{+ANA}$ and $V_{+DIG}$ 2.7 V to 6 V	60			dB
Analog Supply Current – CMP401	$I_{ANA}$				6	mA
Digital Supply Current – CMP401	$I_{DIG}$	$V_O = 0\text{ V}$ , $R_L = \infty$			1	mA
Analog Supply Current – CMP402	$I_{ANA}$				1.2	mA
Digital Supply Current – CMP402	$I_{DIG}$	$V_O = 0\text{ V}$ , $R_L = \infty$			1	mA
<b>DYNAMIC PERFORMANCE</b>						
Propagation Delay – CMP401	$t_p$	100 mV Step with 20 mV OD		32		ns
Propagation Delay – CMP402	$t_p$	100 mV Step with 20 mV OD		70		ns

## ELECTRICAL SPECIFICATIONS (@ $V_{\pm ANA} = \pm 5\text{ V}$ , $V_{DIG} = 5.0\text{ V}$ , $T_A = 25^\circ\text{C}$ , unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
<b>INPUT CHARACTERISTICS</b>						
Offset Voltage <sup>1</sup>	$V_{OS}$	$V_{CM} = 0\text{ V}$			3	mV
Input Common-Mode Voltage Range	$V_{CM}$		-5.0		+4.0	V
Input Differential Voltage Range	$V_{DIFF}$		$\pm 8.0$			V
Common-Mode Rejection	CMRR	$-4.9\text{ V} \leq V_{CM} \leq 3.9\text{ V}$	60			dB
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			1	5	$\mu\text{V}/^\circ\text{C}$
<b>POWER SUPPLY</b>						
Power Supply Rejection Ratio	PSRR	$V_{\pm ANA} \pm 3\text{ V}$ to $\pm 6\text{ V}$	60			dB
Analog Supply Current – CMP401	$I_{ANA}$				6.5	mA
Digital Supply Current – CMP401	$I_{DIG}$	$V_O = 0\text{ V}$ , $R_L = \infty$			2.0	mA
Analog Supply Current – CMP402	$I_{ANA}$				2.0	mA
Digital Supply Current – CMP402	$I_{DIG}$	$V_O = 0\text{ V}$ , $R_L = \infty$			2.0	mA
<b>DYNAMIC PERFORMANCE</b>						
Propagation Delay – CMP401	$t_p$	100 mV Step with 20 mV OD			23	ns
Propagation Delay – CMP402	$t_p$	100 mV Step with 20 mV OD			65	ns

### NOTES

<sup>1</sup>Offset voltage is defined as  $(V_{OS+} + V_{OS-})/2$ .

Specifications subject to change without notice.

# CMP401/CMP402

## ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

Total Analog Supply Voltage	16 V
Digital Supply Voltage	7 V
Analog Positive Supply—Digital Positive Supply	-200 mV
Input Voltage <sup>2</sup>	±7 V
Differential Input Voltage	±9 V
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	
S, RU Package	-65°C to +150°C
Operating Temperature Range	
CMP401G, CMP402G	-40°C to +125°C
Junction Temperature Range	
S, RU Package	-65°C to +150°C
Lead Temperature Range (Soldering 60 sec)	300°C

Package Type	$\theta_{JA}$ <sup>3</sup>	$\theta_{JC}$	Units
16-Lead SOIC (S)	113	37	°C/W
16-Lead TSSOP (RU)	180	37	°C/W

### NOTES

- <sup>1</sup>Absolute Maximum Ratings apply to packaged parts, unless otherwise noted.  
<sup>2</sup>The analog input voltage is equal to ±7 V or the analog supply voltage, whichever is less.  
<sup>3</sup> $\theta_{JA}$  is specified for the worst-case conditions, i.e.,  $\theta_{JA}$  is specified for device soldered in circuit board for SOIC and TSSOP packages.

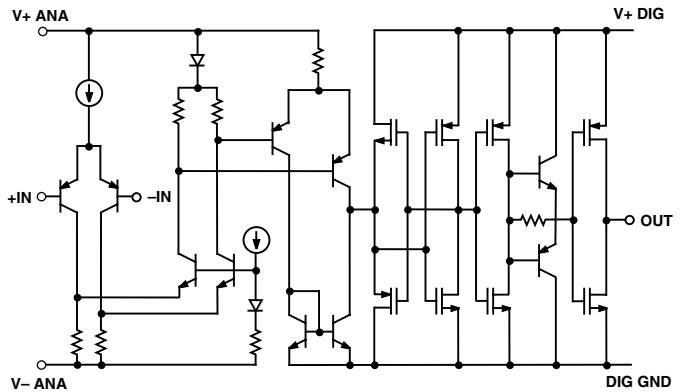
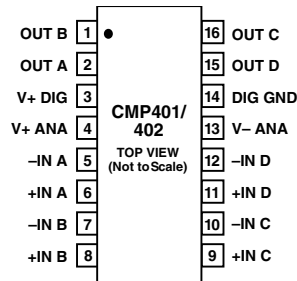


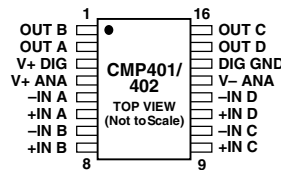
Figure 1. Simplified Schematic

## PIN CONFIGURATIONS

### 16-Lead Narrow-SOIC (S-Suffix)



### 16-Lead TSSOP (RU-Suffix)



## CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the CMP401/CMP402 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

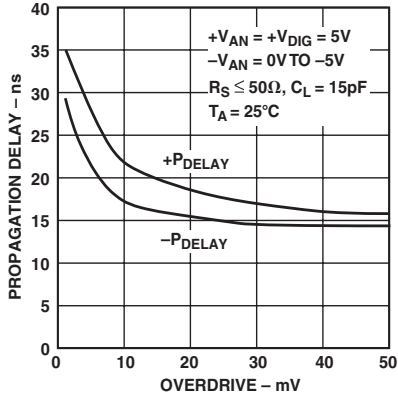


## Revision History

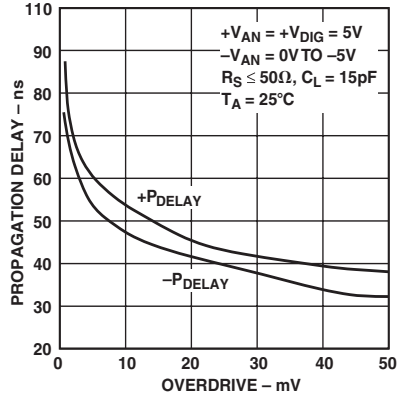
Location	Page
<b>Data Sheet changed from REV. A to REV. B.</b>	
Changed SO-16 to 16-Lead SOIC	Throughout
Moved Revision History	4
Moved Outline Dimensions	8
Updated Outline Dimensions	8
Changes to Ordering Guide	8

Location	Page
<b>Data Sheet changed from REV. 0 to REV. A.</b>	
Edits to GENERAL DESCRIPTION	1
Edits to ABSOLUTE MAXIMUM RATINGS	4
Edits to PACKAGE TYPE	4
Edits to ORDERING GUIDE	4
Deleted DICE CHARACTERISTICS	4
Edits to CMP401/CMP402 PIN CONFIGURATIONS	4

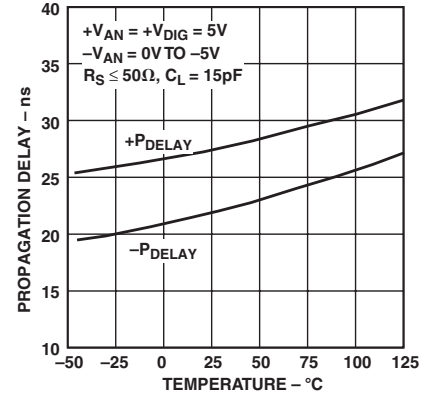
# Typical Performance Characteristics—CMP401/CMP402



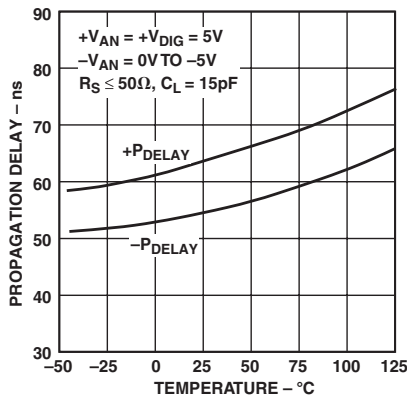
TPC 1. CMP401 Propagation Delay vs. Overdrive



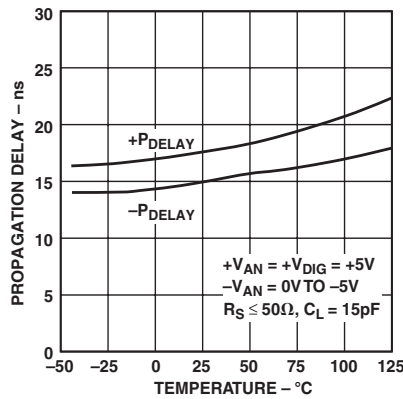
TPC 2. CMP402 Propagation Delay vs. Overdrive



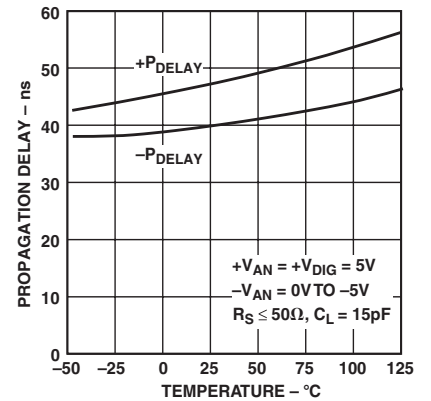
TPC 3. CMP401 Propagation Delay vs. Temperature - 5 mV OD



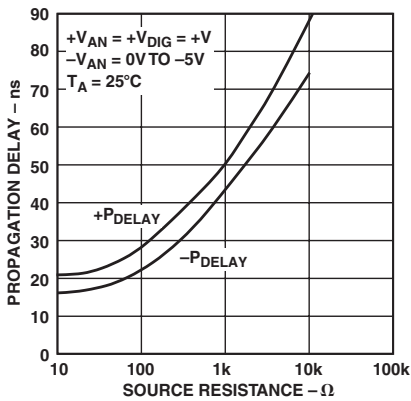
TPC 4. CMP402 Propagation Delay vs. Temperature - 5 mV OD



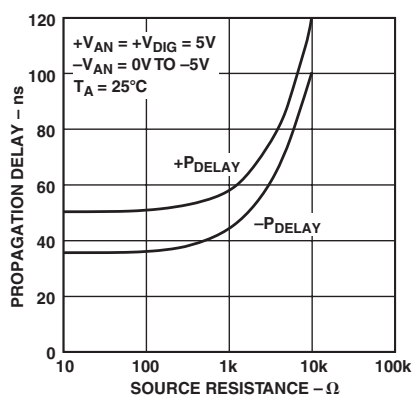
TPC 5. CMP401 Propagation Delay vs. Temperature - 20 mV OD



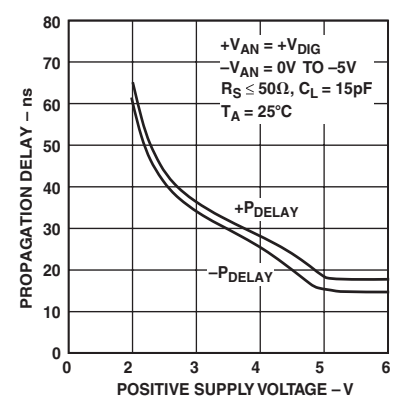
TPC 6. CMP402 Propagation Delay vs. Temperature - 20 mV OD



TPC 7. CMP401 Propagation Delay vs. Source Resistance - 20 mV OD

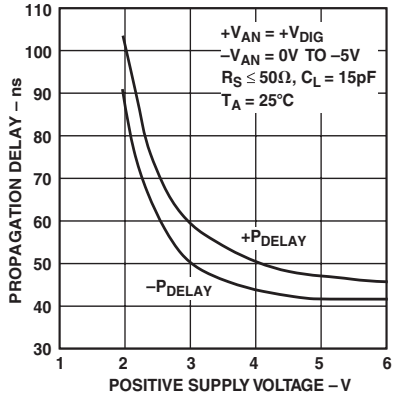


TPC 8. CMP402 Propagation Delay vs. Source Resistance - 20 mV OD

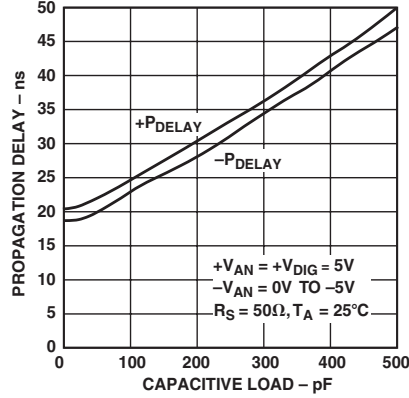


TPC 9. CMP401 Propagation Delay vs. Supply Voltage - 20 mV OD

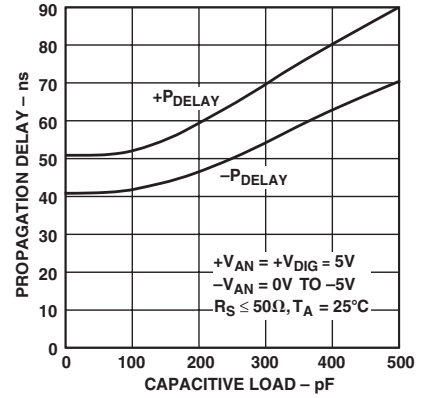
# CMP401/CMP402



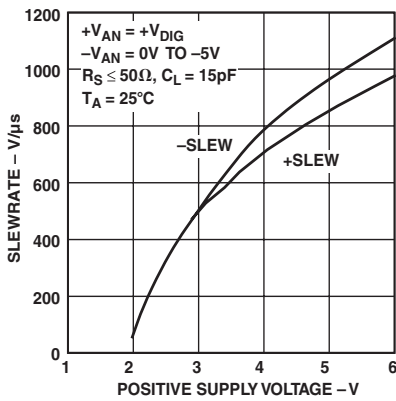
TPC 10. CMP402 Propagation Delay vs. Supply Voltage – 20 mV OD



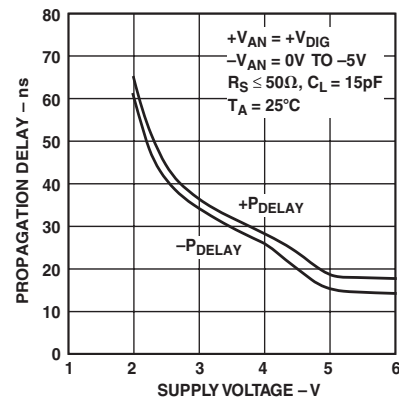
TPC 11. CMP401 Propagation Delay vs. Capacitive Load



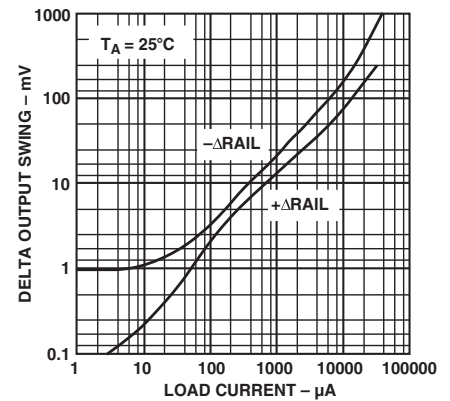
TPC 12. CMP402 Propagation Delay vs. Capacitive Load



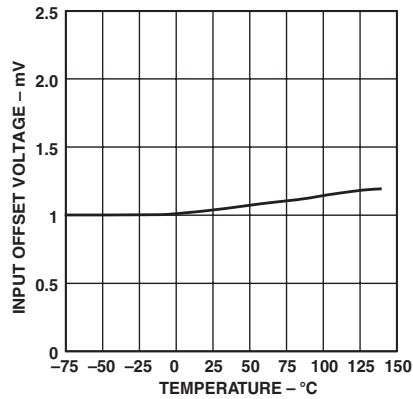
TPC 13. CMP401/CMP402 Slew Rate vs. Positive Supply Voltage



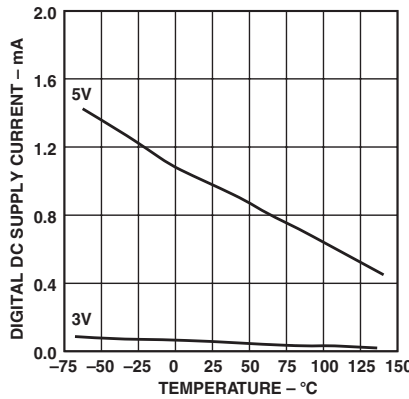
TPC 14. CMP401 Propagation Delay vs. Supply Voltage



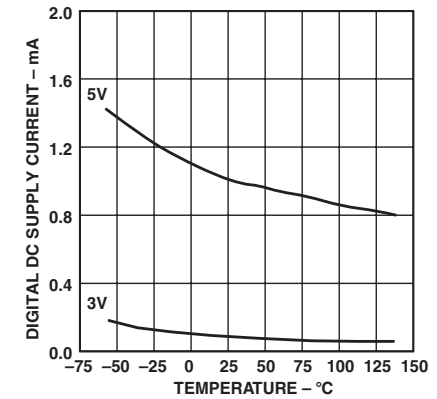
TPC 15. CMP401/CMP402 Delta Output Swing from Power Supplies vs. Load Current



TPC 16. CMP401/CMP402 Input Offset Voltage vs. Temperature



TPC 17. CMP401 Digital Supply Current vs. Temperature



TPC 18. CMP402 Digital Supply Current vs. Temperature

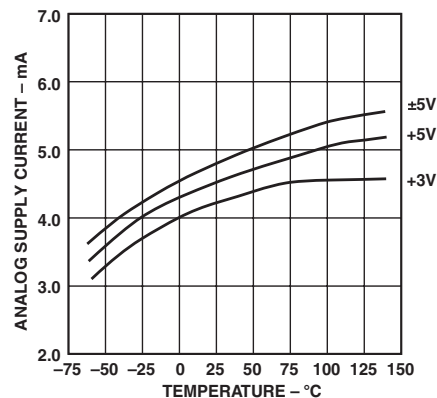
# Typical Performance Characteristics—CMP401/CMP402



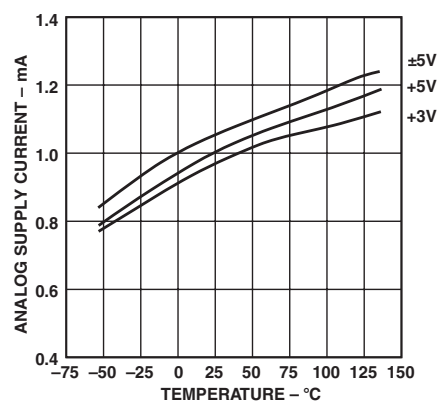
TPC 19. CMP401 Digital Supply Current vs. Digital Supply Voltage



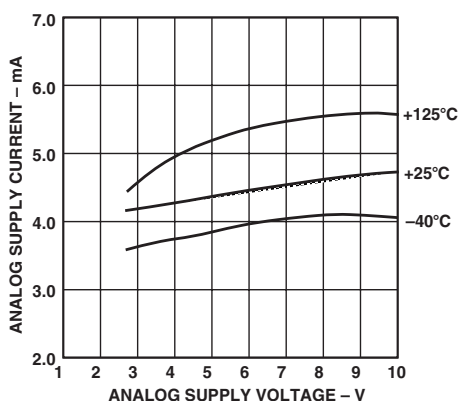
TPC 20. CMP402 Digital Supply Current vs. Digital Supply Voltage



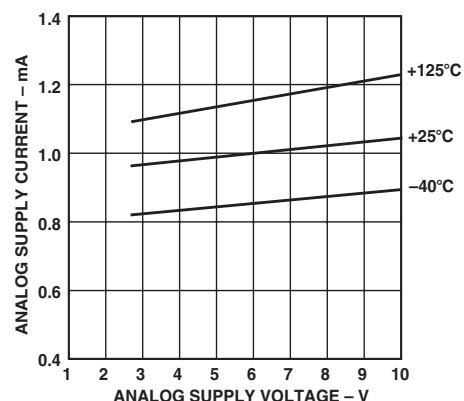
TPC 21. CMP401 Analog Supply Current vs. Temperature



TPC 22. CMP402 Analog Supply Current vs. Temperature

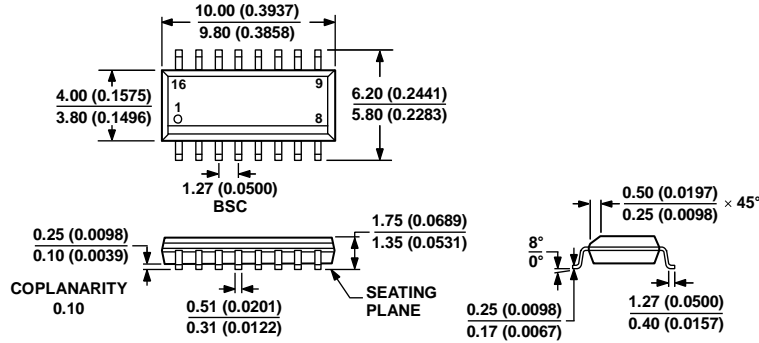


TPC 23. CMP401 Analog Supply Current vs. Analog Supply Voltage



TPC 24. CMP402 Analog Supply Current vs. Analog Supply Voltage

OUTLINE DIMENSIONS

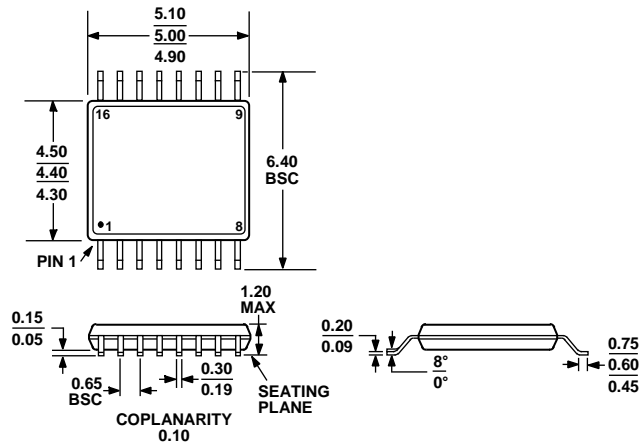


COMPLIANT TO JEDEC STANDARDS MS-012-AC  
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS  
 (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR  
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

060906-A

Figure 1. 16-Lead Standard Small Outline Package [SOIC\_N]  
 Narrow Body  
 (R-16)  
 S-Suffix

Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 2. 16-Lead Thin Shrink Small Outline Package [TSSOP]  
 (RU-16)

Dimensions shown in millimeters

ORDERING GUIDE

Model <sup>1</sup>	Temperature Range	Package Description	Package Option
CMP401GRUZ-REEL	-40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
CMP401GSZ	-40°C to +125°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
CMP401GSZ-REEL	-40°C to +125°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
CMP402GRUZ-REEL	-40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
CMP402GSZ	-40°C to +125°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
CMP402GSZ-REEL	-40°C to +125°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16

<sup>1</sup> Z = RoHS Compliant Part.



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