CY62158EV30 MoBL®

8-Mbit (1024 K × 8) Static RAM

Features

- Very high speed: 45 ns
  - Wide voltage range: 2.20 V–3.60 V
- Pin compatible with CY62158DV30
- Ultra low standby power
  - Typical standby current: 2 μA
  - Maximum standby current: 8 μA
- Ultra low active power
  - Typical active current: 1.8 mA at f = 1 MHz
- Easy memory expansion with $\overline{CE}_1$, CE_2, and $\overline{OE}$ features
- Automatic power down when deselected
- CMOS for optimum speed/power
- Offered in Pb-free 48-ball VFBGA and 44-pin TSOP II packages

Functional Description

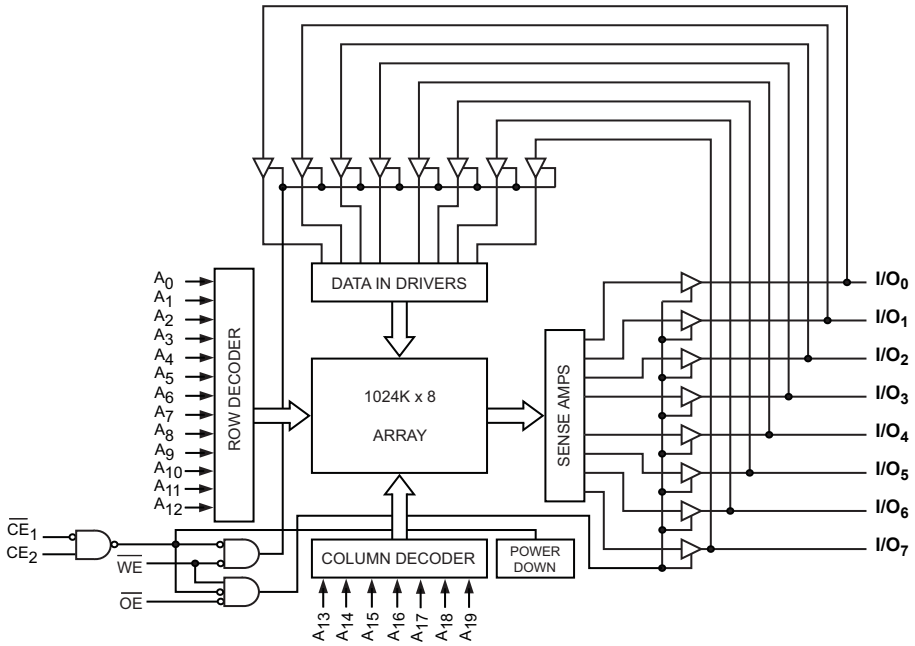
The CY62158EV30 is a high performance CMOS static RAM organized as 1024K words by 8 bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power consumption. Placing the device into standby mode reduces power consumption significantly when deselected ($\overline{CE}_1$ HIGH or CE_2 LOW). The eight input and output pins (I/O_0 through I/O_7) are placed in a high impedance state when the device is deselected ($\overline{CE}_1$ HIGH or CE_2 LOW), the outputs are disabled ($\overline{OE}$ HIGH), or a write operation is in progress ($\overline{CE}_1$ LOW and CE_2 HIGH and $\overline{WE}$ LOW).

To write to the device, take Chip Enables ($\overline{CE}_1$ LOW and CE_2 HIGH) and Write Enable ($\overline{WE}$) input LOW. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{19}).

To read from the device, take Chip Enables ($\overline{CE}_1$ LOW and CE_2 HIGH) and $\overline{OE}$ LOW while forcing the $\overline{WE}$ HIGH. Under these conditions, the contents of the memory location specified by the address pins appear on the I/O pins. See Truth Table on page 11 for a complete description of read and write modes.

For a complete list of related documentation, click here.

Logic Block Diagram



Contents

Pin Configurations

Figure 1. 48-ball VFBGA pinout (Top View) [1]

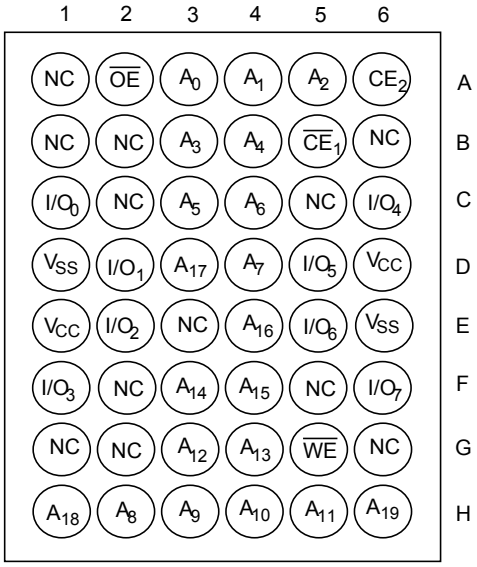
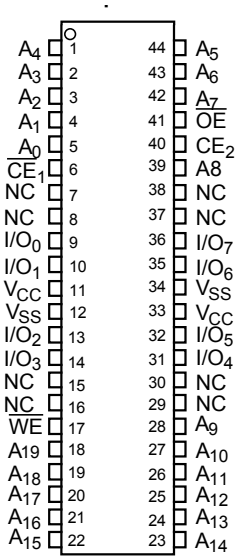


Figure 2. 44-pin TSOP II pinout (Top View) [1]



Product Portfolio

Product	V_{CC} Range (V)			Speed (ns)	Power Dissipation					
					Operating I_{CC} (mA)				Standby, I_{SB2} (µA)	
					f = 1 MHz		f = f_{max}			
	Min	Typ[2]	Max		Typ[2]	Max	Typ[2]	Max	Typ[2]	Max
CY62158EV30LL	2.2	3.0	3.6	45	1.8	3	18	25	2	8

Notes
1. NC pins are not connected on the die.
2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, T_A = 25 °C.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage Temperature ..... –65 °C to +150 °C

Ambient Temperature with Power Applied ..... –55 °C to +125 °C

Supply Voltage to Ground Potential .....–0.3 V to $V_{CC(max)}$ + 0.3 V

DC Voltage Applied to Outputs in High Z State [3, 4] ..... –0.3 V to $V_{CC(max)}$ + 0.3 V

DC Input Voltage [3, 4] ..... –0.3 V to $V_{CC(max)}$ + 0.3 V

Output Current into Outputs (LOW) .....20 mA

Static Discharge Voltage (MIL-STD-883, Method 3015) .....> 2001 V

Latch up Current .....> 200 mA

Operating Range

Product	Range	Ambient Temperature (T_A)	V_{CC}[5]
CY62158EV30LL	Industrial	–40 °C to +85 °C	2.2 V–3.6 V

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		45 ns			Unit
				Min	Typ [6]	Max	
V_{OH}	Output HIGH voltage	I_{OH} = –0.1 mA		2.0	–	–	V
		I_{OH} = –1.0 mA, $V_{CC} \geq$ 2.70 V		2.4	–	–	V
V_{OL}	Output LOW voltage	I_{OL} = 0.1 mA		–	–	0.4	V
		I_{OL} = 2.1 mA, $V_{CC} \geq$ 2.70 V		–	–	0.4	V
V_{IH}	Input HIGH voltage	V_{CC} = 2.2 V to 2.7 V		1.8	–	V_{CC} + 0.3 V	V
		V_{CC} = 2.7 V to 3.6 V		2.2	–	V_{CC} + 0.3 V	V
V_{IIL}	Input LOW voltage	V_{CC} = 2.2 V to 2.7 V		–0.3	–	0.6	V
		V_{CC} = 2.7 V to 3.6 V		–0.3	–	0.8	V
I_{IX}	Input leakage current	GND ≤ $V_I \leq V_{CC}$		–1	–	+1	µA
I_{OZ}	Output leakage current	GND ≤ $V_O \leq V_{CC}$, Output Disabled		–1	–	+1	µA
I_{CC}	V_{CC} operating supply current	f = f_{max} = $1/t_{RC}$	V_{CC} = V_{CCmax}, I_{OUT} = 0 mA, CMOS levels	–	18	25	mA
		f = 1 MHz		–	1.8	3	mA
I_{SB1}	Automatic CE power down current — CMOS Inputs	$\overline{CE}_1 \geq V_{CC}$ – 0.2 V, $CE_2 \leq$ 0.2 V, $V_{IN} \geq V_{CC}$ – 0.2 V, $V_{IN} \leq$ 0.2 V, f = f_{max} (Address and Data Only), f = 0 ($\overline{OE}$ and $\overline{WE}$), V_{CC} = 3.60 V		–	2	8	µA
I_{SB2}[7]	Automatic CE Power down Current — CMOS inputs	$\overline{CE}_1 \geq V_{CC}$ – 0.2 V or $CE_2 \leq$ 0.2 V, $V_{IN} \geq V_{CC}$ – 0.2 V or $V_{IN} \leq$ 0.2 V, f = 0, V_{CC} = 3.60 V		–	2	8	µA

Notes
3. $V_{IL(min)}$ = –2.0 V for pulse durations less than 20 ns.
4. $V_{IH(max)}$= V_{CC} + 0.75 V for pulse duration less than 20 ns.
5. Full device AC operation assumes a 100 µs ramp time from 0 to V_{CC}(min) and 200 µs wait time after V_{CC} stabilization.
6. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = $V_{CC(typ)}$, T_A = 25 °C.
7. Chip enables ($\overline{CE}_1$ and CE_2) must be at CMOS level to meet the I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.

Capacitance

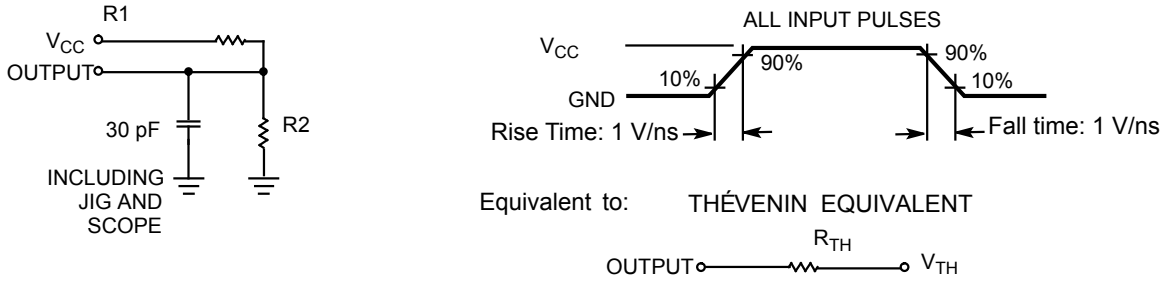
Parameter [8]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = $V_{CC(typ)}$	10	pF
C_{OUT}	Output capacitance		10	pF

Thermal Resistance

Parameter [8]	Description	Test Conditions	48-ball BGA	44-pin TSOP II	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still Air, soldered on a 3 × 4.5 inch, two-layer printed circuit board	72	76.88	°C/W
Θ_{JC}	Thermal resistance (junction to case)		8.86	13.52	°C/W

AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms



Parameters	2.5 V	3.0 V	Unit
R1	16667	1103	Ω
R2	15385	1554	Ω
R_{TH}	8000	645	Ω
V_{TH}	1.20	1.75	V

Note
8. Tested initially and after any design or process changes that may affect these parameters.

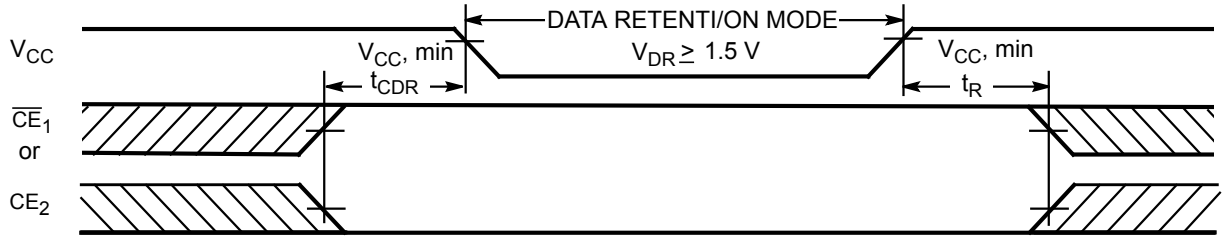
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ[9]	Max	Unit
V_{DR}	V_{CC} for data retention		1.5	–	–	V
I_{CCDR}[10]	Data retention current	V_{CC} = 1.5 V, $\overline{CE}_1 \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	–	2	5	µA
t_{CDR}[11]	Chip deselect to data retention time		0	–	–	ns
t_R[12]	Operation recovery time		45	–	–	ns

Data Retention Waveform

Figure 4. Data Retention Waveform



Notes

9. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, T_A = 25 °C.
10. Chip enables ($\overline{CE}_1$ and CE_2) must be at CMOS level to meet the I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.
11. Tested initially and after any design or process changes that may affect these parameters.
12. Full Device AC operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100$ µs or stable at $V_{CC(min)} \geq 100$ µs.

Switching Characteristics

Over the Operating Range

Parameter [13, 14]	Description	45 ns		Unit
		Min	Max	
Read Cycle				
t_{RC}	Read cycle time	45	–	ns
t_{AA}	Address to data valid	–	45	ns
t_{OHA}	Data Hold from address change	10	–	ns
t_{ACE}	$\overline{CE}_1$ LOW and CE_2 HIGH to data valid	–	45	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	22	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[15]	5	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[15, 16]	–	18	ns
t_{LZCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to Low Z[15]	10	–	ns
t_{HZCE}	$\overline{CE}_1$ HIGH or CE_2 LOW to High Z[15, 16]	–	18	ns
t_{PU}	$\overline{CE}_1$ LOW and CE_2 HIGH to Power Up	0	–	ns
t_{PD}	$\overline{CE}_1$ HIGH or CE_2 LOW to Power Down	–	45	ns
Write Cycle[17, 18]				
t_{WC}	Write cycle time	45	–	ns
t_{SCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to Write End	35	–	ns
t_{AW}	Address setup to Write End	35	–	ns
t_{HA}	Address Hold from Write End	0	–	ns
t_{SA}	Address setup to Write Start	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	35	–	ns
t_{SD}	Data setup to Write End	25	–	ns
t_{HD}	Data Hold from Write End	0	–	ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[15, 16]	–	18	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[15]	10	–	ns

Notes

13. In an earlier revision of this device, under a specific application condition, READ and WRITE operations were limited to switching of the chip enable signal as described in the Application Note AN66311. However, the issue has been fixed and in production now, and hence, this Application Note is no longer applicable. It is available for download on our website as it contains information on the date code of the parts, beyond which the fix has been in production.
14. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns or less (1V/ns), timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} as shown in AC Test Loads and Waveforms on page 5.
15. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
16. t_{HZOE}, t_{HZCE}, and t_{HZWE} transitions are measured when the outputs enter a high impedance state.
17. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}_1 = V_{IL}$, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.
18. The minimum write cycle pulse width for Write Cycle No. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) should be equal to the sum of t_{SD} and t_{HZWE}.

Switching Waveforms

Figure 5. Read Cycle No. 1 (Address Transition Controlled) [19, 20]

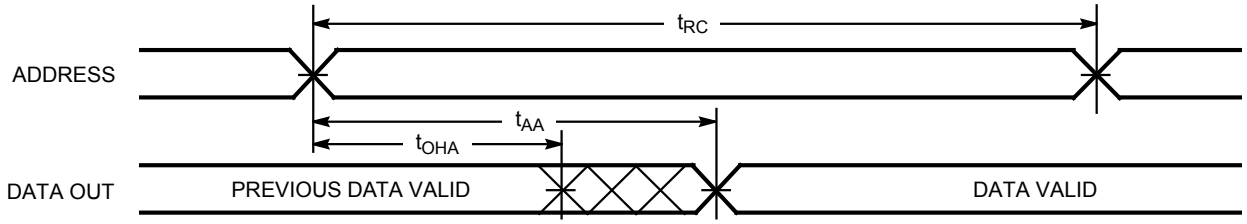
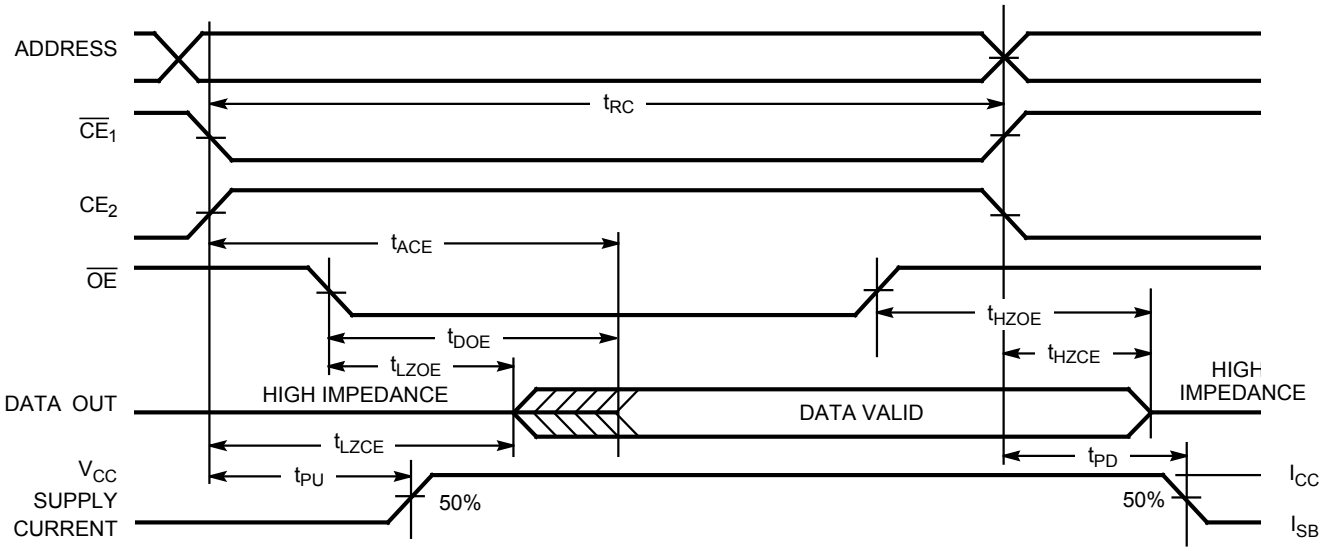


Figure 6. Read Cycle No. 2 ($\overline{OE}$ Controlled) [20, 21]



Notes
19. Device is continuously selected. $\overline{OE}$, $\overline{CE}_1$ = V_{IL}, CE_2 = V_{IH}.
20. $\overline{WE}$ is HIGH for read cycle.
21. Address valid before or similar to $\overline{CE}_1$ transition LOW and CE_2 transition HIGH.

Switching Waveforms (continued)

Figure 7. Write Cycle No. 1 ($\overline{WE}$ Controlled) [22, 23, 24]

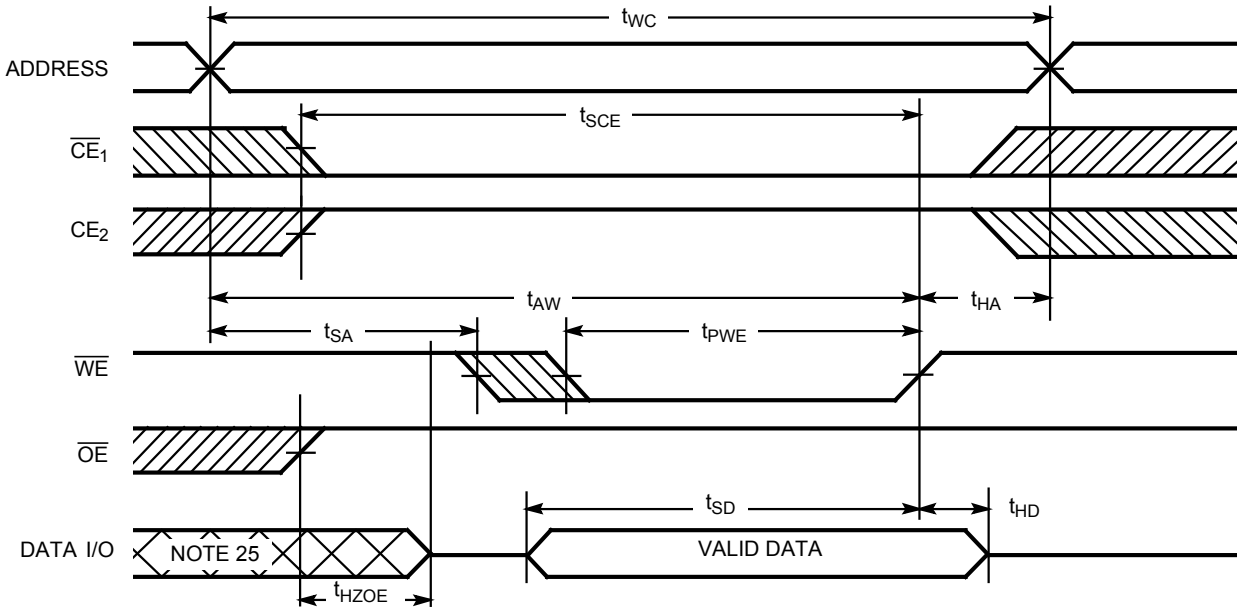
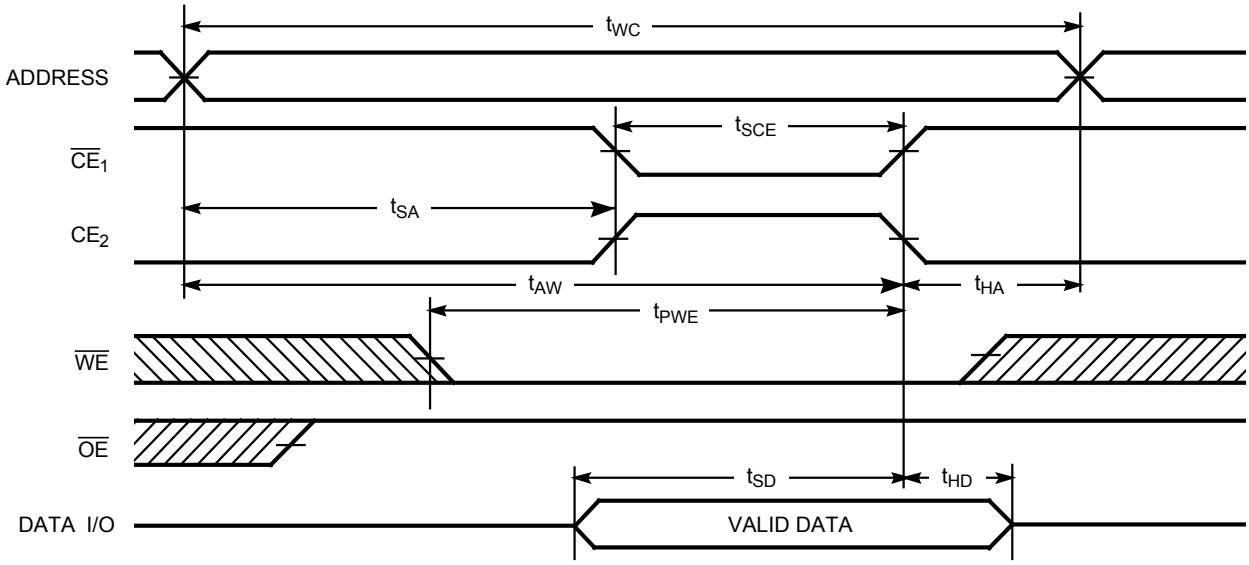


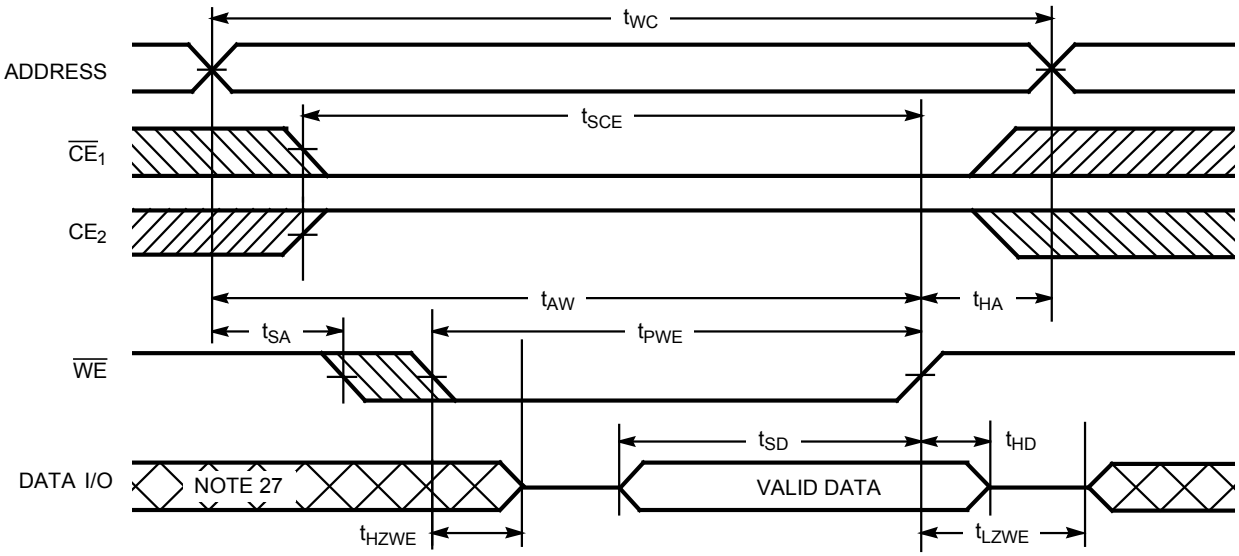
Figure 8. Write Cycle No. 2 ($\overline{CE_1}$ or CE_2 Controlled) [22, 23, 24]



Notes
22. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE_1}$ = V_{IL}, and CE_2 = V_{IH}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.
23. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
24. If $\overline{CE_1}$ goes HIGH or CE_2 goes LOW simultaneously with $\overline{WE}$ HIGH, the output remains in high impedance state.
25. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 9. Write Cycle No. 3 (WE Controlled, OE LOW) [26, 28]



Notes
26. If $\overline{CE}_1$ goes HIGH or CE_2 goes LOW simultaneously with $\overline{WE}$ HIGH, the output remains in high impedance state.
27. During this period, the I/Os are in output state. Do not apply input signals.
28. The minimum write cycle pulse width should be equal to the sum of t_{SD} and t_{HZWE}.

Truth Table

$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode	Power
H	X[29]	X	X	High Z	Deselect/Power down	Standby (I_{SB})
X[29]	L	X	X	High Z	Deselect/Power down	Standby (I_{SB})
L	H	H	L	Data Out	Read	Active (I_{CC})
L	H	L	X	Data In	Write	Active (I_{CC})
L	H	H	H	High Z	Selected, Outputs Disabled	Active (I_{CC})

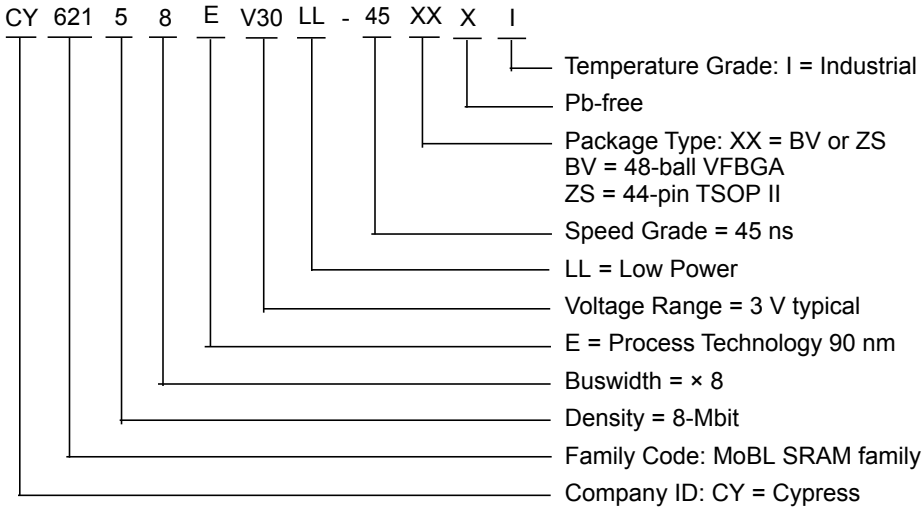
Note
29. The 'X' (Don't care) state for the Chip enables in the truth table refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62158EV30LL-45BVXI	51-85150	48-ball VFBGA (Pb-free)	Industrial
	CY62158EV30LL-45ZSXI	51-85087	44-pin TSOP Type II (Pb-free)	

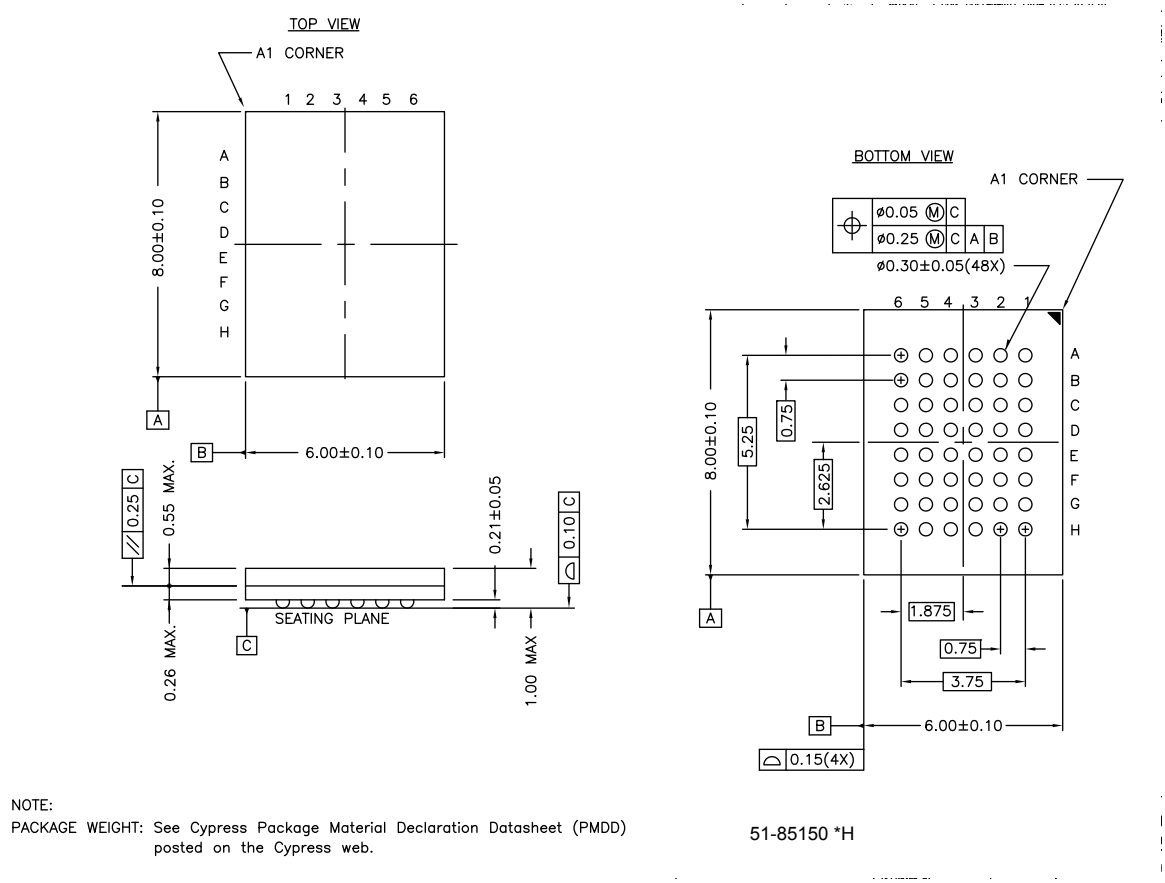
Contact your local Cypress sales representative for availability of these parts.

Ordering Code Definitions



Package Diagrams

Figure 10. 48-ball VFBGA (6 × 8 × 1 mm) BV48/BZ48 Package Outline, 51-85150

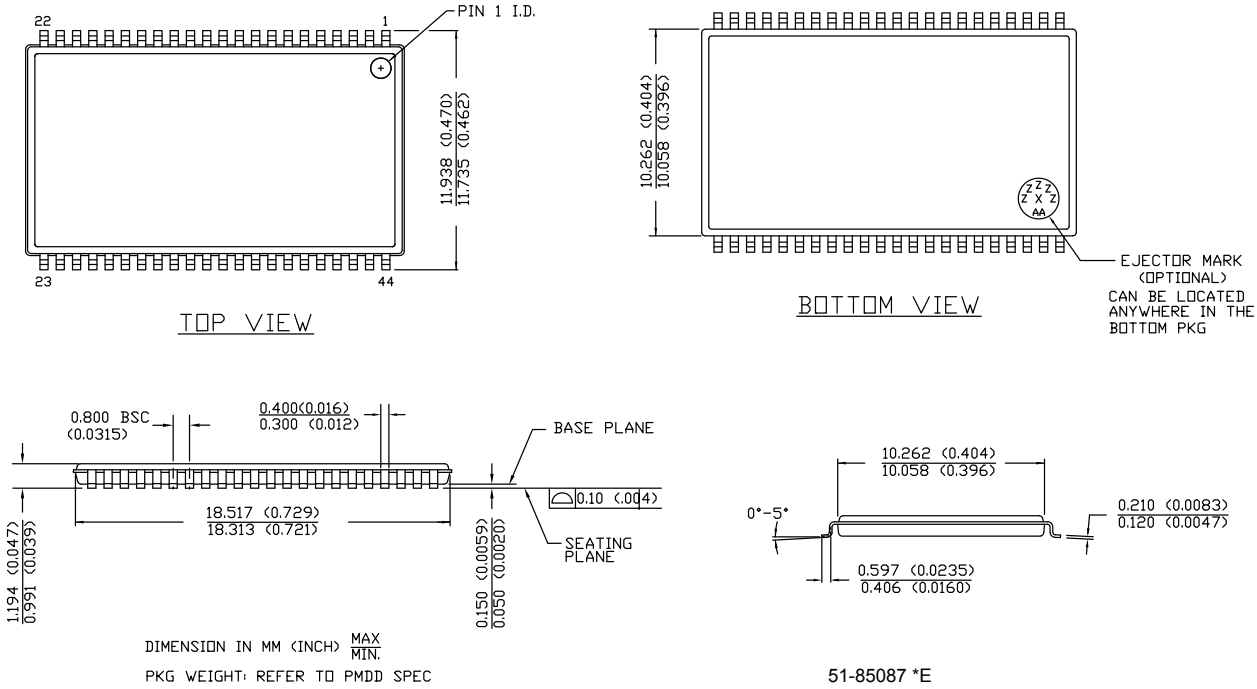


NOTE:
PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD) posted on the Cypress web.

51-85150 *H

Package Diagrams (continued)

Figure 11. 44-pin TSOP Z44-II Package Outline, 51-85087



Acronyms

Acronym	Description
$\overline{CE}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{OE}$	Output Enable
RAM	Random Access Memory
SRAM	Static Random Access Memory
TTL	Transistor-Transistor Logic
TSOP	Thin Small Outline Package
VFBGA	Very Fine-Pitch Ball Grid Array
$\overline{WE}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
µs	microsecond
mA	milliampere
mm	millimeter
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY62158EV30 MoBL®, 8-Mbit (1024 K × 8) Static RAM Document Number: 38-05578				
Rev.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	270329	See ECN	PCI	New data sheet.
*A	291271	See ECN	SYT	Converted from Advance Information to Preliminary Changed I_{CCDR} from 4 to 4.5 μA
*B	444306	See ECN	NXR	Converted from Preliminary to Final. Removed 35 ns speed bin Removed “L” bin. Removed 44 pin TSOP II package Included 48 pin TSOP I package Changed the I_{CC} Typ value from 16 mA to 18 mA and I_{CC} max value from 28 mA to 25 mA for test condition f = fax = $1/t_{RC}$. Changed the I_{CC} max value from 2.3 mA to 3 mA for test condition f = 1MHz. Changed the I_{SB1} and I_{SB2} max value from 4.5 μA to 8 μA and Typ value from 0.9 μA to 2 μA respectively. Updated Thermal Resistance table Changed Test Load Capacitance from 50 pF to 30 pF. Added Typ value for I_{CCDR} . Changed the I_{CCDR} max value from 4.5 μA to 5 μA Corrected t_R in Data Retention Characteristics from 100 μs to t_{RC} ns Changed t_{LZOE} from 3 to 5 Changed t_{LZCE} from 6 to 10 Changed t_{HZCE} from 22 to 18 Changed t_{PWE} from 30 to 35 Changed t_{SD} from 22 to 25 Changed t_{LZWE} from 6 to 10 Updated the ordering Information and replaced the Package Name column with Package Diagram.
*C	467052	See ECN	NXR	Included 44 pin TSOP II package in Product Offering. Removed TSOP I package; Added reference to CY62157EV30 TSOP I Updated the ordering Information table
*D	1015643	See ECN	VKN	Added footnote #8 related to I_{SB2} and I_{CCDR}
*E	2934396	06/03/10	VKN	Added footnote #21 related to chip enable Updated package diagrams Updated template
*F	3110202	12/14/2010	PRAS	Updated Logic Block Diagram and Package Diagram. Added Ordering Code Definitions.
*G	3269641	05/30/2011	RAME	Updated Features. Removed the note “For best practice recommendations, refer to the Cypress application note “System Design Guidelines” at http://www.cypress.com.” and its reference in Functional Description. Updated Data Retention Characteristics. Added Acronyms and Units of Measure. Updated in new template.
*H	3598409	04/24/2012	TAVA	Updated Package Diagram 51-85150 (from Rev *F to *G) and 51-85087 (from Rev *C to *D).
*I	4100078	08/20/2013	VINI	Updated Switching Characteristics: Added Note 13 and referred the same note in “Parameter” column. Updated Package Diagrams: spec 51-85150 – Changed revision from *G to *H. spec 51-85087 – Changed revision from *D to *E. Updated in new template.

Document History Page (continued)

Document Title: CY62158EV30 MoBL®, 8-Mbit (1024 K × 8) Static RAM Document Number: 38-05578				
Rev.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
*J	4576526	11/21/2014	VINI	Added related documentation hyperlink in page 1. Added Note 18 in Switching Characteristics. Added note reference 18 in the Switching Characteristics table. Added Note 28 in Switching Waveforms. Added note reference 28 in Figure 9.

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