CY7C1012DV33

12-Mbit (512 K × 24) Static RAM

Features

- High speed
  - t_{AA} = 10 ns
- Low active power
  - I_{CC} = 175 mA at 10 ns
- Low CMOS standby power
  - I_{SB2} = 25 mA
- Operating voltages of 3.3 ± 0.3 V
- 2.0 V data retention
- Automatic power down when deselected
- TTL compatible inputs and outputs
- Available in Pb-free standard 119-ball PBGA

Functional Description

The CY7C1012DV33 is a high performance CMOS static RAM organized as 512K words by 24 bits. Each data byte is separately controlled by the individual chip selects ($\overline{CE}_1$, $\overline{CE}_2$, and $\overline{CE}_3$). $\overline{CE}_1$ controls the data on the I/O_0–I/O_7, while $\overline{CE}_2$ controls the data on I/O_8–I/O_{15}, and $\overline{CE}_3$ controls the data on the data pins I/O_{16}–I/O_{23}. This device has an automatic power down feature that significantly reduces power consumption when deselected.

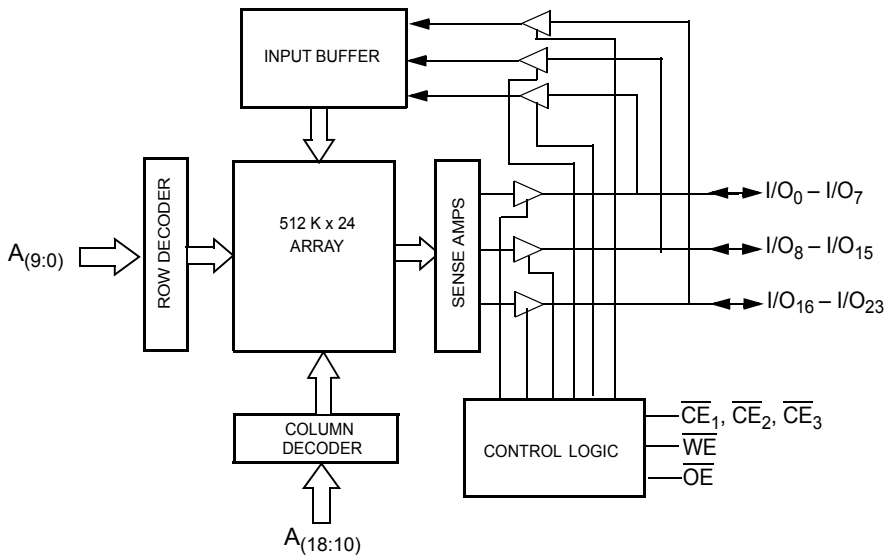
Writing the data bytes into the SRAM is accomplished when the chip select controlling that byte is LOW and the write enable input ($\overline{WE}$) input is LOW. Data on the respective input and output (I/O) pins is then written into the location specified on the address pins (A_0–A_{18}). Asserting all of the chip selects LOW and write enable LOW writes all 24 bits of data into the SRAM. Output enable ($\overline{OE}$) is ignored while in WRITE mode.

Data bytes are also individually read from the device. Reading a byte is accomplished when the chip select controlling that byte is LOW and write enable ($\overline{WE}$) HIGH, while output enable ($\overline{OE}$) remains LOW. Under these conditions, the contents of the memory location specified on the address pins appear on the specified data input and output (I/O) pins. Asserting all the chip selects LOW reads all 24 bits of data from the SRAM.

The 24 I/O pins (I/O_0–I/O_{23}) are placed in a high impedance state when all the chip selects are HIGH or when the output enable ($\overline{OE}$) is HIGH during a READ mode. For more information, see the Truth Table on page 10.

For a complete list of related documentation, click here.

Logic Block Diagram



Contents

Selection Guide

Description	-10	Unit
Maximum Access Time	10	ns
Maximum Operating Current	175	mA
Maximum CMOS Standby Current	25	mA

Pin Configuration

Figure 1. 119-ball PBGA (Top View) [1]

	1	2	3	4	5	6	7
A	NC	A	A	A	A	A	NC
B	NC	A	A	$\overline{CE}_1$	A	A	NC
C	I/O_{12}	NC	$\overline{CE}_2$	NC	$\overline{CE}_3$	NC	I/O_0
D	I/O_{13}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	I/O_1
E	I/O_{14}	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V_{SS}	I/O_2
F	I/O_{15}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	I/O_3
G	I/O_{16}	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V_{SS}	I/O_4
H	I/O_{17}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	I/O_5
J	NC	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V_{SS}	NC
K	I/O_{18}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	I/O_6
L	I/O_{19}	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V_{SS}	I/O_7
M	I/O_{20}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	I/O_8
N	I/O_{21}	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V_{SS}	I/O_9
P	I/O_{22}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	I/O_{10}
R	I/O_{23}	A	NC	NC	NC	A	I/O_{11}
T	NC	A	A	$\overline{WE}$	A	A	NC
U	NC	A	A	$\overline{OE}$	A	A	NC

Note
1. NC pins are not connected on the die.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... –65 °C to +150 °C

Ambient Temperature with Power Applied ..... –55 °C to +125 °C

Supply Voltage on V_{CC} Relative to GND [2] .....–0.5 V to +4.6 V

DC Voltage Applied to Outputs in High Z State [2] ..... –0.5 V to V_{CC} + 0.5 V

DC Input Voltage [2] ..... –0.5 V to V_{CC} + 0.5 V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage (MIL-STD-883, Method 3015) ..... > 2001 V

Latch Up Current ..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Industrial	–40 °C to +85 °C	3.3 V ± 0.3 V

DC Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions [3]	-10		Unit
			Min	Max	
V_{OH}	Output HIGH voltage	Min V_{CC}, I_{OH} = –4.0 mA	2.4	–	V
V_{OL}	Output LOW voltage	Min V_{CC}, I_{OL} = 8.0 mA	–	0.4	V
V_{IH}	Input HIGH voltage		2.0	V_{CC} + 0.3	V
V_{IL} [2]	Input LOW voltage		–0.3	0.8	V
I_{IX}	Input leakage current	GND ≤ V_{IN} ≤ V_{CC}	–1	+1	µA
I_{OZ}	Output leakage current	GND ≤ V_{OUT} ≤ V_{CC}, output disabled	–1	+1	µA
I_{CC}	V_{CC} operating supply current	V_{CC} = Max, f = f_{MAX} = $1/t_{RC}$, I_{OUT} = 0 mA, CMOS levels	–	175	mA
I_{SB1}	Automatic CE power-down current – TTL inputs	Max V_{CC}, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}	–	30	mA
I_{SB2}	Automatic CE power-down current – CMOS inputs	Max V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.3 V, V_{IN} ≥ V_{CC} – 0.3 V or V_{IN} ≤ 0.3 V, f = 0	–	25	mA

Notes

2. $V_{IL(min)}$ = –2.0 V and $V_{IH(max)}$ = V_{CC} + 2 V for pulse durations of less than 20 ns.
3. $\overline{CE}$ indicates a combination of all three chip enables. When active LOW, $\overline{CE}$ indicates the $\overline{CE_1}$ or $\overline{CE_2}$, or $\overline{CE_3}$ is LOW. When HIGH, $\overline{CE}$ indicates the $\overline{CE_1}$, $\overline{CE_2}$, and $\overline{CE_3}$ are HIGH.

Capacitance

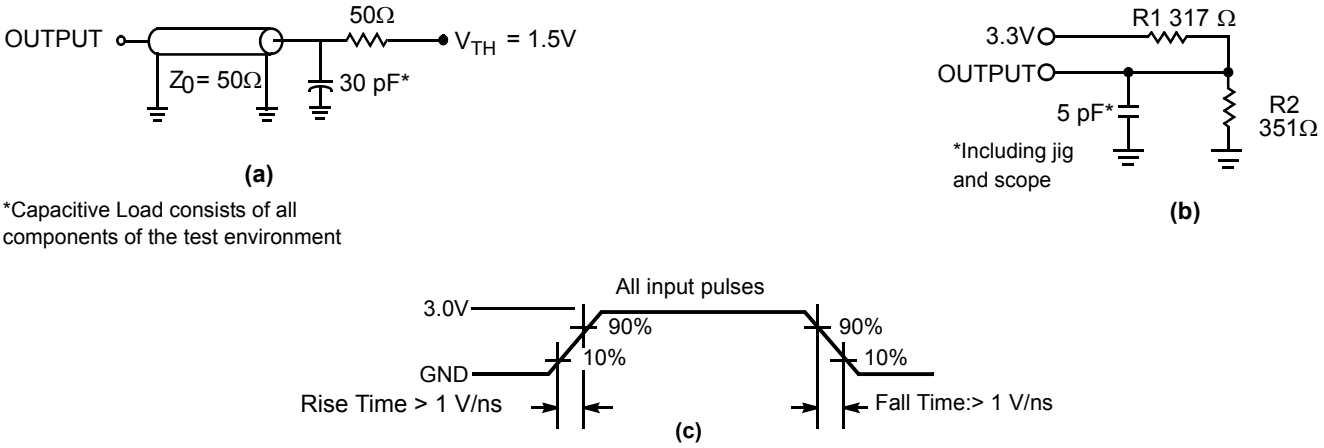
Parameter [4]	Description	Test Conditions	Max	Unit
C_{IN}	Input Capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = 3.3 V	8	pF
C_{OUT}	I/O Capacitance		10	pF

Thermal Resistance

Parameter [4]	Description	Test Conditions	119-ball PBGA	Unit
Θ_{JA}	Thermal Resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four layer printed circuit board	20.31	°C/W
Θ_{JC}	Thermal Resistance (junction to case)		8.35	°C/W

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms [5]



Notes
4. Tested initially and after any design or process changes that may affect these parameters.
5. Valid SRAM operation does not occur until the power supplies have reached the minimum operating V_{DD} (3.0 V). 100 µs (t_{power}) after reaching the minimum operating V_{DD}, normal SRAM operation begins including reduction in V_{DD} to the data retention (V_{CCDR}, 2.0 V) voltage.

AC Switching Characteristics

Over the Operating Range

Parameter [6]	Description	-10		Unit
		Min	Max	
Read Cycle				
t_{power} [7]	V_{CC}(typical) to the first access	100	–	µs
t_{RC}	Read cycle time	10	–	ns
t_{AA}	Address to data valid	–	10	ns
t_{OHA}	Data hold from address change	3	–	ns
t_{ACE}	$\overline{CE}$ active LOW to data valid [8]	–	10	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	5	ns
t_{LZOE}	$\overline{OE}$ LOW to low Z [9]	1	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to high Z [9]	–	5	ns
t_{LZCE}	$\overline{CE}$ active LOW to low Z [8, 9]	3	–	ns
t_{HZCE}	$\overline{CE}$ deselect HIGH to high Z [8, 9]	–	5	ns
t_{PU}	$\overline{CE}$ active LOW to power up [8, 10]	0	–	ns
t_{PD}	$\overline{CE}$ deselect HIGH to power down [8, 10]	–	10	ns
Write Cycle [11, 12]				
t_{WC}	Write cycle time	10	–	ns
t_{SCE}	$\overline{CE}$ active LOW to write end [8]	7	–	ns
t_{AW}	Address setup to write end	7	–	ns
t_{HA}	Address hold from write end	0	–	ns
t_{SA}	Address setup to write start	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	7	–	ns
t_{SD}	Data Setup to write end	5.5	–	ns
t_{HD}	Data Hold from write end	0	–	ns
t_{LZWE}	$\overline{WE}$ HIGH to low Z [9]	3	–	ns
t_{HZWE}	$\overline{WE}$ LOW to high Z [9]	–	5	ns

Notes

6. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V. Test conditions for the read cycle use output loading as shown in part (a) of Figure 2 on page 5, unless specified otherwise.
7. t_{POWER} gives the minimum amount of time that the power supply is at typical V_{CC} values until the first memory access is performed.
8. $\overline{CE}$ indicates a combination of all three chip enables. When active LOW, $\overline{CE}$ indicates the $\overline{CE_1}$ or $\overline{CE_2}$, or $\overline{CE_3}$ is LOW. When HIGH, $\overline{CE}$ indicates the $\overline{CE_1}$, $\overline{CE_2}$, and $\overline{CE_3}$ are HIGH.
9. t_{HZOE}, t_{HZCE}, t_{HZWE}, t_{LZOE}, t_{LZCE}, and t_{LZWE} are specified with a load capacitance of 5 pF as in part (b) of Figure 2 on page 5. Transition is measured ±200 mV from steady state voltage.
10. These parameters are guaranteed by design and are not tested.
11. The internal write time of the memory is defined by the overlap of $\overline{CE_1}$ or $\overline{CE_2}$ or $\overline{CE_3}$ LOW and $\overline{WE}$ LOW. Chip enables must be active and $\overline{WE}$ must be LOW to initiate a write. The transition of any of these signals terminate the write. The input data setup and hold timing are referenced to the leading edge of the signal that terminates the write.
12. The minimum write cycle time for Write Cycle No. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

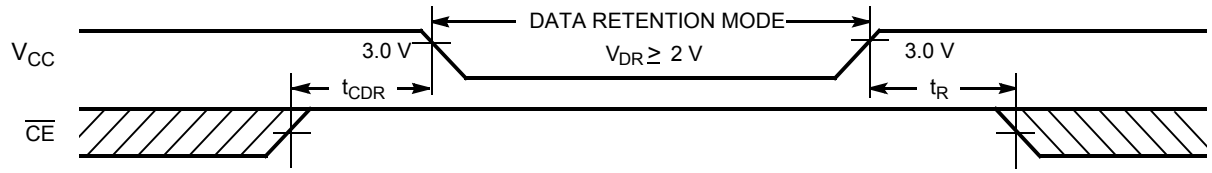
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions [13]	Min	Typ	Max	Unit
V_{DR}	V_{CC} for data retention		2	–	–	V
I_{CCDR}	Data retention current	V_{CC} = 2 V, $\overline{CE} \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	–	–	25	mA
t_{CDR} [14]	Chip deselect to data retention time		0	–	–	ns
t_R [15]	Operation recovery time		t_{RC}	–	–	ns

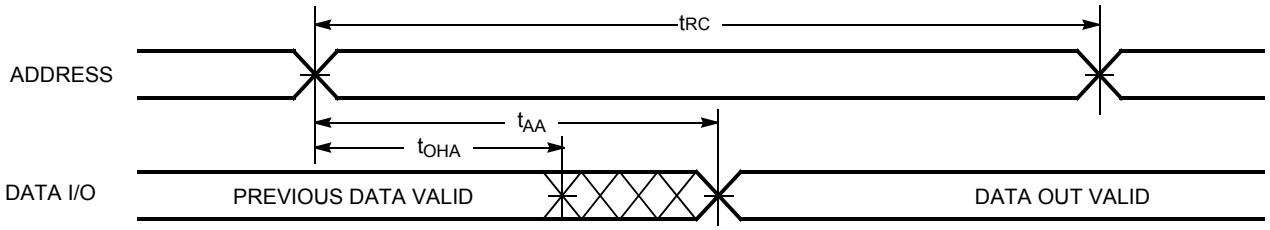
Data Retention Waveform

Figure 3. Data Retention Waveform



Switching Waveforms

Figure 4. Read Cycle No. 1 (Address Transition Controlled) [16, 17]



Notes

13. $\overline{CE}$ indicates a combination of all three chip enables. When active LOW, $\overline{CE}$ indicates the $\overline{CE_1}$ or $\overline{CE_2}$, or $\overline{CE_3}$ is LOW. When HIGH, $\overline{CE}$ indicates the $\overline{CE_1}$, $\overline{CE_2}$, and $\overline{CE_3}$ are HIGH.
14. Tested initially and after any design or process changes that may affect these parameters.
15. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 50$ µs or stable at $V_{CC(min)} \geq 50$ µs.
16. Device is continuously selected. $\overline{OE}$, $\overline{CE} = V_{IL}$.
17. $\overline{WE}$ is HIGH for read cycle.

Switching Waveforms (continued)

Figure 5. Read Cycle No. 2 ($\overline{OE}$ Controlled) [18, 19, 20]

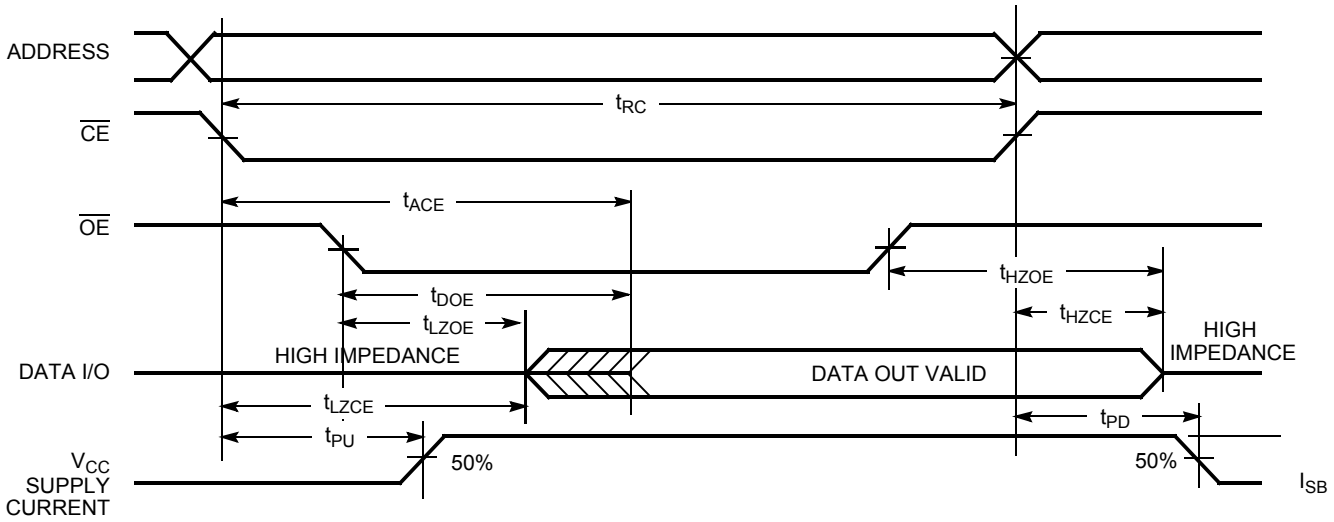
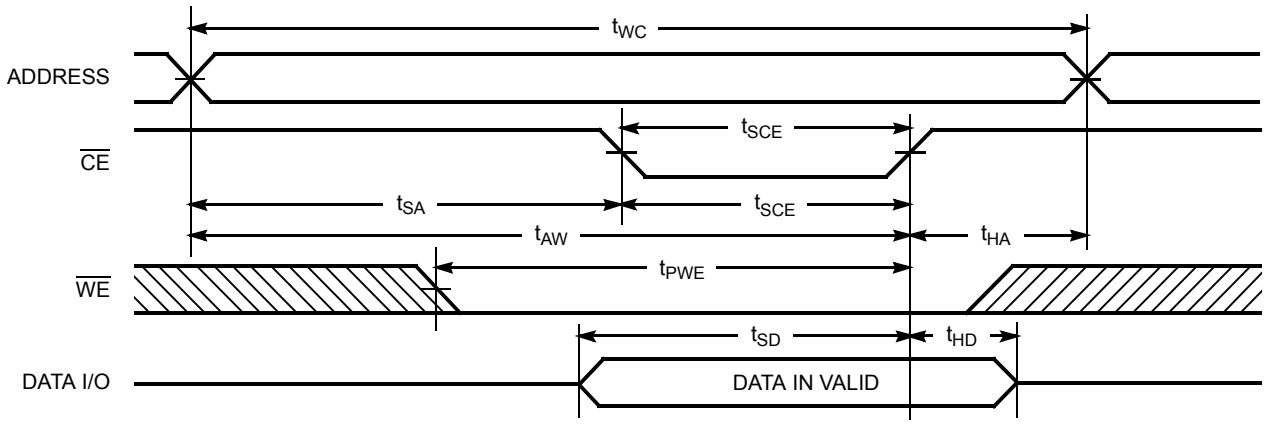


Figure 6. Write Cycle No. 1 ($\overline{CE}$ Controlled) [18, 21, 22]



Notes
18. $\overline{CE}$ indicates a combination of all three chip enables. When active LOW, $\overline{CE}$ indicates the $\overline{CE_1}$ or $\overline{CE_2}$, or $\overline{CE_3}$ is LOW. When HIGH, $\overline{CE}$ indicates the $\overline{CE_1}$, $\overline{CE_2}$, and $\overline{CE_3}$ are HIGH.
19. $\overline{WE}$ is HIGH for read cycle.
20. Address valid before or similar to $\overline{CE}$ transition LOW.
21. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
22. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high impedance state.

Switching Waveforms (continued)

Figure 7. Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ HIGH During Write) [23, 24, 25]

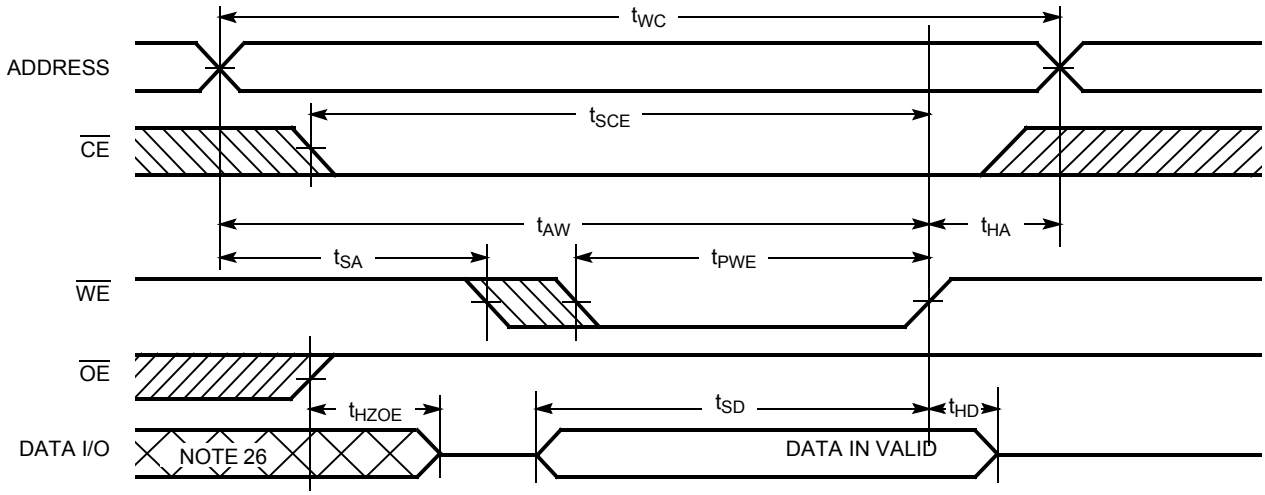
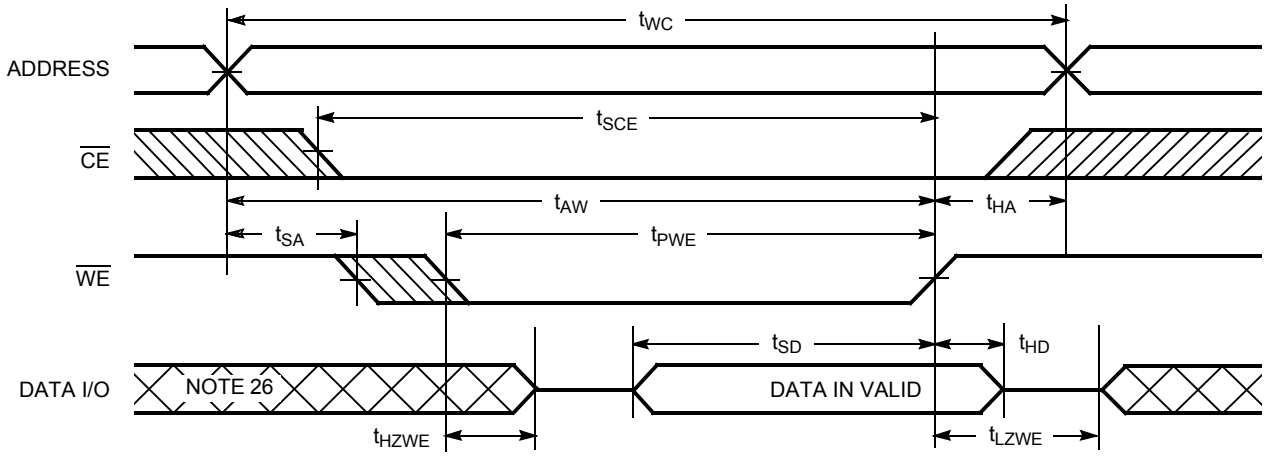


Figure 8. Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) [23, 25]



Notes
23. $\overline{CE}$ indicates a combination of all three chip enables. When active LOW, $\overline{CE}$ indicates the $\overline{CE}_1$ or $\overline{CE}_2$, or $\overline{CE}_3$ is LOW. When HIGH, $\overline{CE}$ indicates the $\overline{CE}_1$, $\overline{CE}_2$, and $\overline{CE}_3$ are HIGH.
24. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
25. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high impedance state.
26. During this period, the I/Os are in output state. Do not apply input signals.

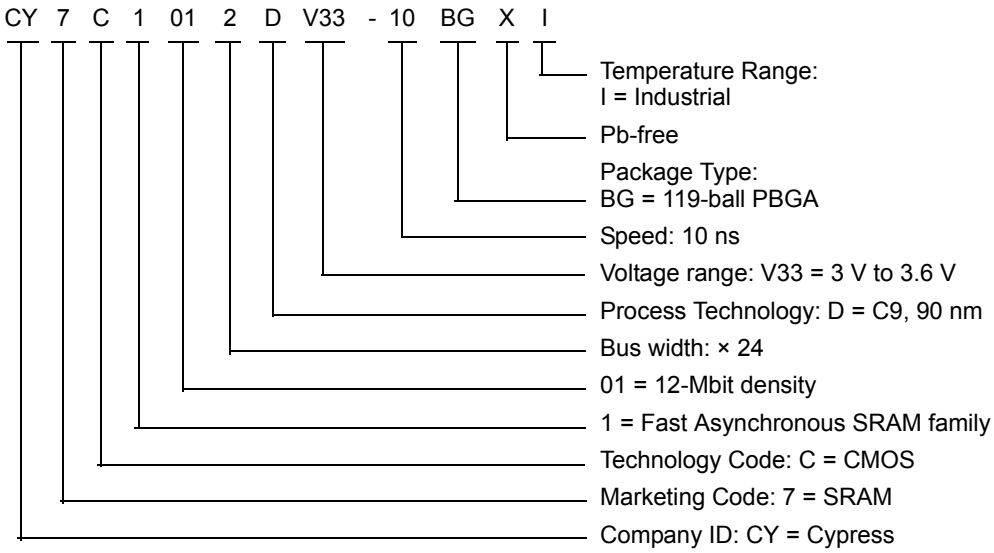
Truth Table

$\overline{CE_1}$	$\overline{CE_2}$	$\overline{CE_3}$	$\overline{OE}$	$\overline{WE}$	$I/O_0–I/O_7$	$I/O_8–I/O_{15}$	$I/O_{16}–I/O_{23}$	Mode	Power
H	H	H	X	X	High Z	High Z	High Z	Power Down	Standby (I_{SB})
L	H	H	L	H	Data Out	High Z	High Z	Read	Active (I_{CC})
H	L	H	L	H	High Z	Data Out	High Z	Read	Active (I_{CC})
H	H	L	L	H	High Z	High Z	Data Out	Read	Active (I_{CC})
L	L	L	L	H	Full Data Out	Full Data Out	Full Data Out	Read	Active (I_{CC})
L	H	H	X	L	Data In	High Z	High Z	Write	Active (I_{CC})
H	L	H	X	L	High Z	Data In	High Z	Write	Active (I_{CC})
H	H	L	X	L	High Z	High Z	Data In	Write	Active (I_{CC})
L	L	L	X	L	Full Data In	Full Data In	Full Data In	Write	Active (I_{CC})
L	L	L	H	H	High Z	High Z	High Z	Selected, Outputs Disabled	Active (I_{CC})

Ordering Information

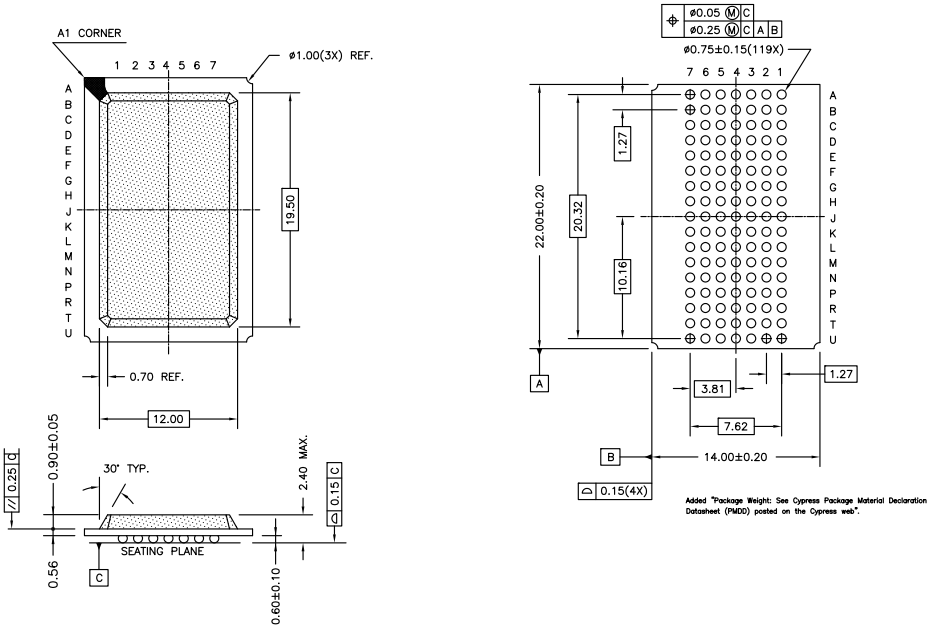
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C1012DV33-10BGXI	51-85115	119-ball Plastic Ball Grid Array (14 × 22 × 2.4 mm) (Pb-free)	Industrial

Ordering Code Definitions



Package Diagram

Figure 9. 119-ball PBGA (14 × 22 × 2.4 mm) BG119 Package Outline, 51-85115



51-85115 *D

Acronyms

Acronym	Description
$\overline{CE}$	chip enable
CMOS	complementary metal oxide semiconductor
I/O	input/output
$\overline{OE}$	output enable
PBGA	plastic ball grid array
SRAM	static random access memory
TTL	transistor-transistor logic
$\overline{WE}$	write enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
µs	microsecond
mA	milliampere
mm	millimeter
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY7C1012DV33, 12-Mbit (512 K × 24) Static RAM Document Number: 38-05610				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	250650	SYT	See ECN	New data sheet
*A	469517	NXR	See ECN	Converted from Advance Information to Preliminary Corrected typo in the Document Title Removed -10 and -12 speed bins from product offering Changed J7 ball of BGA from DNU to NC Removed Industrial Operating range from product offering Included the Maximum ratings for Static Discharge Voltage and Latch Up Current on page 3 Changed $I_{CC(Max)}$ from 220 mA to 150 mA Changed $I_{SB1(Max)}$ from 70 mA to 30 mA Changed $I_{SB2(Max)}$ from 40 mA to 25 mA Specified the Overshoot specification in footnote 1 Updated the Truth Table Updated the Ordering Information table
*B	499604	NXR	See ECN	Added note 1 for NC pins Changed I_{CC} specification from 150 mA to 185 mA Updated Test Condition for I_{CC} in DC Electrical Characteristics table Added note for t_{ACE}, t_{LZCE}, t_{HZCE}, t_{PU}, t_{PD}, and t_{SCE} in AC Switching Characteristics Table on page 4
*C	1462585	VKN	See ECN	Converted from preliminary to final Updated block diagram Changed I_{CC} specification from 185 mA to 225 mA Updated thermal specs
*D	2604677	VKN / PYRS	11/12/08	Removed Commercial operating range, Added Industrial operating range Removed 8 ns speed bin, Added 10 ns speed bin, Modified footnote# 3
*E	3104943	AJU	12/08/2010	Added Ordering Code Definitions. Updated Package Diagram.
*F	3417829	TAVA	10/21/2011	Updated DC Electrical Characteristics. Updated Switching Waveforms. Added Acronyms and Units of Measure. Updated in new template.
*G	4574311	TAVA	11/19 /2014	Added related documentation hyperlink in page 1. Updated Figure 9 in Package Diagram (spec 51-85115 *C to *D).

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