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FAN7346
4-Channel LED Current Balance Controller

Features

- Linear Balance Control for 4-Channel LED Arrays
- Wide LED String Voltage Range: ≤ 100V
- Wide V_{CC} Voltage: 10.5V to 35V
- External Linear Regulation Switch: MOSFET or BJT
- Internal Voltage Regulator for Feedback
- Monitoring Drain-Source Voltage of External Switch
- Precision Current Accuracy Trimmed to 1.5%
- Supports External PWM Dimming - Positive
- Supports Wide Dimming Ratio: 0.5%~100%
- Adaptive Linear Regulation Method
- Generate Integrated Feedback Signal for Primary Controller (Current Feedback + PWM Dimming)
- High Efficiency by Primary Side Direct Feedback
- Thermal Shutdown (Auto-Recovery)
- Over-Voltage Regulation
- Channel Individual Open-LED Protection
- Channel Individual Short-LED Protection
- Channel Individual Over-Current Protection
- Error Flag Output
- 28-Pin SOIC

Applications

- LED BLU for LCD TV
- LED BLU for LCD Monitor
- LED Lighting

Description

The FAN7346 is an LED current-balance controller that controls 4-LED arrays to maintain equal LED current.

The FAN7346 has a high withstanding voltage, so is suitable for edge-type LED BLU and LED Lighting. To minimize components between primary to secondary, the FAN7346 generates a new integrated feedback signal.

The FAN7346 provides various protections, such as over-voltage regulation, open-LED protection, thermal protection, and drain-source voltage protection of regulating switch (the FAN7346 monitors all LED arrays drain-source voltage for protection). To increase system reliability, FAN7346 applies individual string protection. Because FAN7346 integrates so many functions it reduces overall BOM costs.

LED brightness can be linearly varied up to LED current by applying an external Pulse Width Modulated (PWM) signal to the PWM pin.

The FAN7346 is available in a 28-SOIC package.

Ordering Information

Part Number	Operating Temperature	Package	Packing Method
FAN7346M	-40 to +125°C	28-Lead, Small-Outline Integrated Circuit (SOIC)	Rail
FAN7346MX			Tape & Reel

Block Diagram

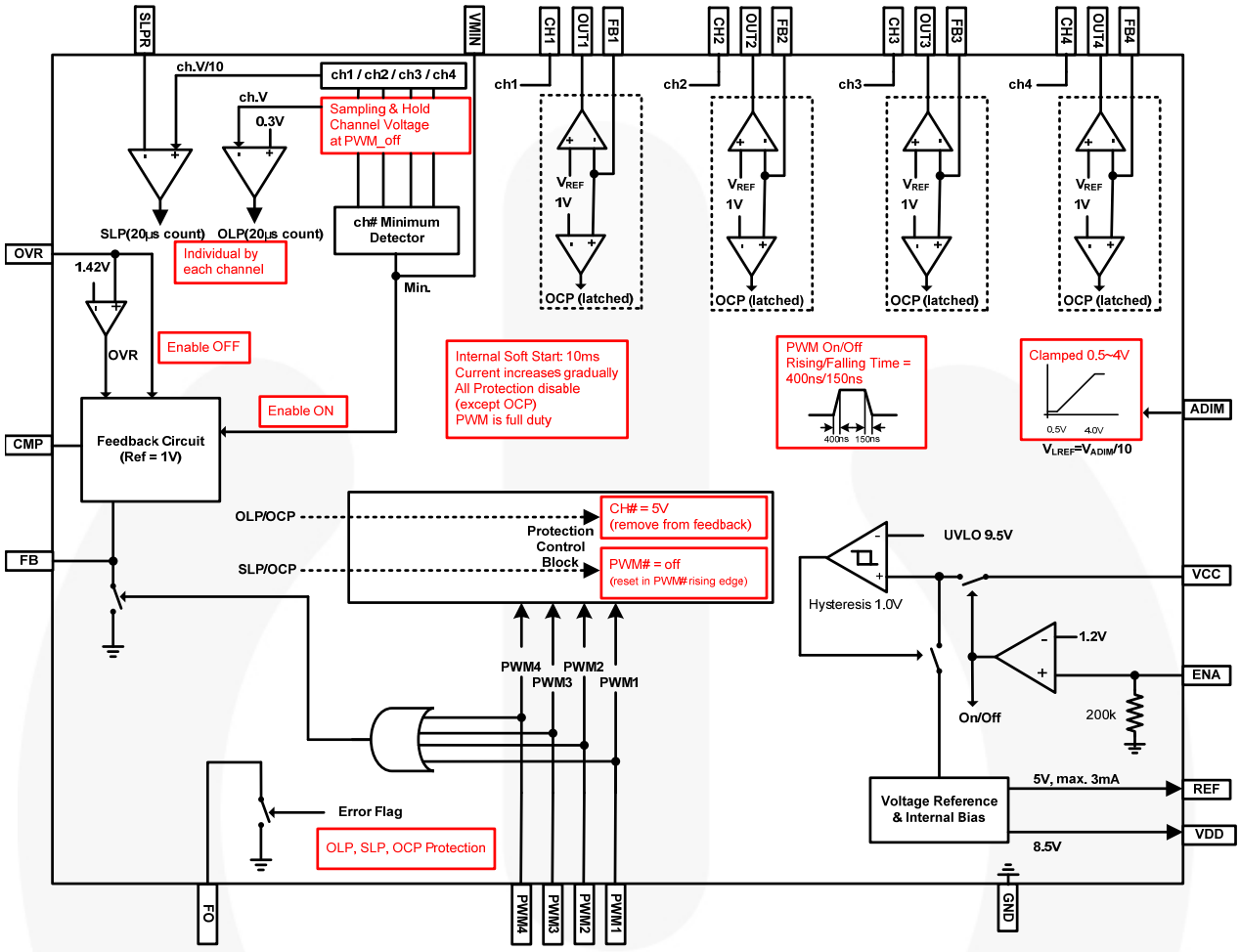

Figure 1. Internal Block Diagram

Pin Configuration

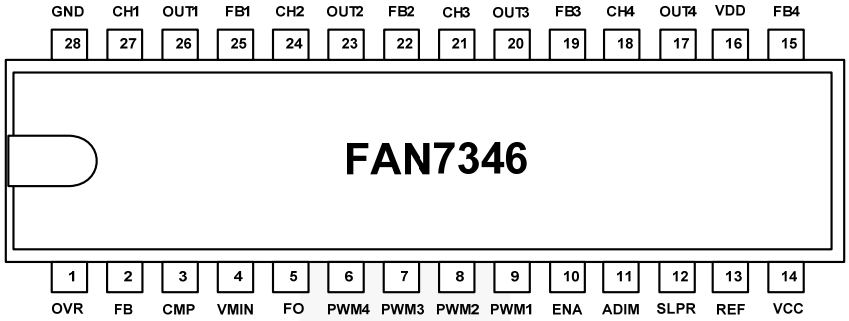

Figure 2. Package Diagram

Pin Definitions

Pin #	Name	Description
1	OVR	This pin is input for over-voltage regulation.
2	FB	This pin is for feedback of minimum drain voltage of external current regulation switch. This pin is externally connected to the cathode of the feedback photo-coupler.
3	CMP	This pin is for compensation of the minimum channel voltage feedback.
4	VMIN	Synchronous signal of channel drain-voltage. If multiple controllers are operated, this pin must be tied together. In single operation, this pin must be open.
5	FO	This pin is fault output. In case of OLP, SLP, and OCP; this pin is connected to ground.
6	PWM4	PWM dimming signal input pin of channel 4.
7	PWM3	PWM dimming signal input pin of channel 3.
8	PWM2	PWM dimming signal input pin of channel 2.
9	PWM1	PWM dimming signal input pin of channel 1.
10	ENA	Enable input.
11	ADIM	This pin is for the reference voltage of the LED current feedback voltage.
12	SLPR	This pin is for setting the reference of channel over-voltage protection (short-LED protection).
13	REF	This pin is the reference output. Voltage is 5V; current capability is 3mA.
14	VCC	This pin is the supply voltage of the controller.
15	FB4	This pin is for current sensing feedback of channel 4.
16	VDD	Internal gate driver power supply voltage. A large capacitor (1μF~2μF) must be connected from this pin to ground.
17	OUT4	This pin is for gate signal to the external balance FET of channel 4.
18	CH4	This pin is for drain voltage of the external balance FET of channel 4.
19	FB3	This pin is for current sensing feedback of channel 3.
20	OUT3	This pin is for gate signal to the external balance FET of channel 3.
21	CH3	This pin is for drain voltage of the external balance FET of channel 3.
22	FB2	This pin is for current sensing feedback of channel 2.
23	OUT2	This pin is for gate signal to the external balance FET of channel 2.
24	CH2	This pin is for drain voltage of the external balance FET of channel 2.
25	FB1	This pin is for current sensing feedback of channel 1.
26	OUT1	This pin is for gate signal to the external balance FET of channel 1.
27	CH1	This pin is for drain voltage of the external balance FET of channel 1.
28	GND	This pin is the ground.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V_{IN}	IC Supply Voltage	10.5	35.0	V
T_A	Operating Temperature Range	-40	+125	°C
T_J	Operating Junction Temperature		+150	°C
T_{STG}	Storage Temperature Range	-65	+150	°C
θ_{JA}	Thermal Resistance Junction-Air[1,2]		70	°C/W
P_D	Power Dissipation		1.4	W

Notes:
1. Thermal resistance test board. Size: 76.2mm x 114.3mm x 1.6mm (1S0P); JEDEC standard: JESD51-2, JESD51-3.
2. Assume no ambient airflow.

Pin Breakdown Voltage

Pin #	Name	Value	Unit		Pin #	Name	Value	Unit
1	OVR	6	V		15	FB4	6	V
2	FB	6			16	VDD	17	
3	CMP	6			17	OUT4	17	
4	VMIN	6			18	CH4	100	
5	FO	6			19	FB3	6	
6	PWM4	6			20	OUT3	17	
7	PWM3	6			21	CH3	100	
8	PWM2	6			22	FB2	6	
9	PWM1	6			23	OUT2	17	
10	ENA	6			24	CH2	100	
11	ADIM	6			25	FB1	6	
12	SLPR	6			26	OUT1	17	
13	REF	6			27	CH1	100	
14	VCC	35			28	GND		

Electrical Characteristics

For typical values; T_A = 25°C, V_{IN} = 12V, and -25°C ≤ T_A ≤ 85°C, unless otherwise specified. Specifications to -40°C ~ 125°C are guaranteed by design based on final characterization results.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Under-Voltage Lockout Section (UVLO)						
V_{th}	Start Threshold Voltage		8.5	9.5	10.5	V
V_{thhys}	Start Threshold Voltage Hysteresis		0.5	1.0	1.5	V
I_{st}	Startup Current	V_{IN}=8V		100	300	µA
I_{op}	Operating Supply Current	V_{IN}=12V, Not Switching		1	3	mA
ON/OFF Section						
V_{on}	On-State Input Voltage		1.4		5.0	V
V_{off}	Off-Stage Input Voltage				0.7	V
R_{ENA}	Pull-Down Resistor		130	200	270	kΩ
Reference Section (Recommend 1µF X7R Capacitor)						
V_{REF}	5V Regulation Voltage	I_{REF}=0mA	4.9	5.0	5.1	V
$V_{R\text{-}LINE}$	5V Line Regulation	10 ≤ V_{IN} ≤ 35V			50	mV
$V_{R\text{-}LOAD}$	5V Load Regulation	0 ≤ I_{REF} ≤ 3mA			50	mV
V_{DD}	8.5V Regulation Voltage	V_{IN}=12V	8.0	8.5	9.0	V
LED Current Section						
V_{FBX}	CH LED Current Reference Voltage	V_{ADIM}=2V	194	200	206	mV
V_{LREF}	LED Current Reference Voltage	0.5V ≤ V_{ADIM} ≤ 4V		V_{ADIM} /10		V
$V_{ADIM\text{-}CLAMPH}$	ADIM Voltage HIGH Clamping Voltage	V_{IN}=12V	3.84	4.00	4.16	V
$V_{ADIM\text{-}CLAMPL}$	ADIM Voltage LOW Clamping Voltage	V_{IN}=12V	0.45	0.50	0.55	
B_{CH}	Current Balance Between Channels	V_{ADIM}=2V	-1.5		1.5	%
Headroom Voltage Feedback Section						
V_{FBR}	Feedback Reference Voltage		0.95	1.00	1.05	V
I_{leak}	Channel Leakage Current	PWM ON, V_{CH}=1V	0		100	µA
		PWM OFF, V_{CH}=30V	0		2	µA
A_V	Open-Loop Gain(3)	V_{VMIN}=1V		65		dB
G_m	Error Amplifier Transconductance	V_{VMIN}=1.5V	140	180	220	µmho
I_{sin}	Output Sink Current	V_{VMIN}=0V	70	120	170	µA
I_{sur}	Output Source Current	V_{VMIN}=2V	70	120	170	µA

Continued on the following page…

Electrical Characteristics (Continued)

For typical values; T_A = 25°C, V_{IN} = 12V, and -25°C ≤ T_A ≤ 85°C, unless otherwise specified. Specifications to -40°C ~ 125°C are guaranteed by design based on final characterization results.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
PWM Dimming Section						
$V_{bdim(ON)}$	PWM Dimming On Voltage		2		5	V
$V_{bdim(Off)}$	PWM Dimming Off Voltage		0		0.8	V
f_{bdim}	PWM Dim Input Frequency Range(3)	On Duty Ratio=1%	100		500	Hz
t_{bdimR}	PWM Dim On Rising Time(3)	Ext. Switch Q_g=4.3nC		400		ns
t_{bdimF}	PWM Dim Off Falling Time(3)	Ext. Switch Q_g=4.3nC		150		ns
Soft-Start Section						
t_{SS}	Soft-Start Time(3)	V_{OVR}=1V, I_{LED}: 0 to Maximum		10		ms
Protection Section						
$V_{TH,OVR}$	OVR Threshold Voltage		1.35	1.42	1.49	V
$V_{TH,OCP}$	OCP Threshold Voltage		0.95	1.00	1.05	V
T_{OCP}	OCP Shutdown Time(3)			10		µs
$V_{TH,SLP}$	SLP Threshold Voltage	V_{SLPR}=1V	9.5	10.0	10.5	V
$T_{D,SLP}$	SLP Delay(3)			20		µs
$T_{D,OLP}$	OLP Delay(3)			20		µs
$V_{TH,OLP}$	OLP Threshold Voltage		0.27	0.30	0.33	V
T_{TRIP}	Internal Thermal Protection Threshold(3)			150		°C
T_{TYH}	Internal Thermal Protection Hysteresis(3)			25		°C
Output Section						
V_{GH}	NMOS Gate High Voltage	V_{IN}=12V	8.0	8.5	9.0	V
V_{GL}	NMOS Gate Low Voltage	V_{IN}=12V		0		V
$V_{G,UVLO}$	NMOS Gate Voltage with UVLO Activated	V_{IN}=7V			0.3	V
$I_{G,SOURCE}$	NMOS Gate Drive Source Current	V_{IN}=12V	50	150	250	mA
$I_{G,SINK}$	NMOS Gate Drive Sink Current	V_{IN}=12V	300	500	700	mA

Note:
3. These Parameters, although guaranteed, are not 100% tested in production.

Typical Performance Characteristics

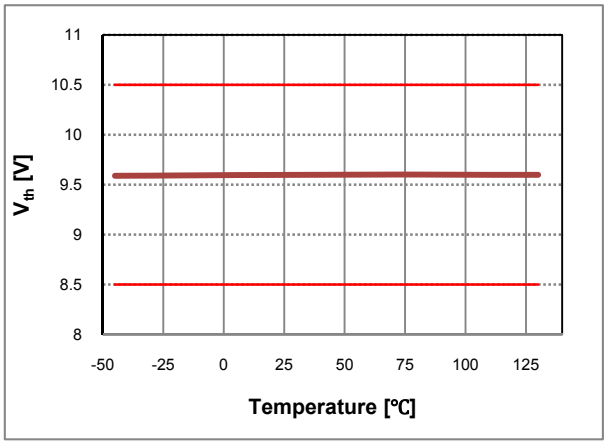

Figure 3. Start Threshold Voltage vs. Temperature

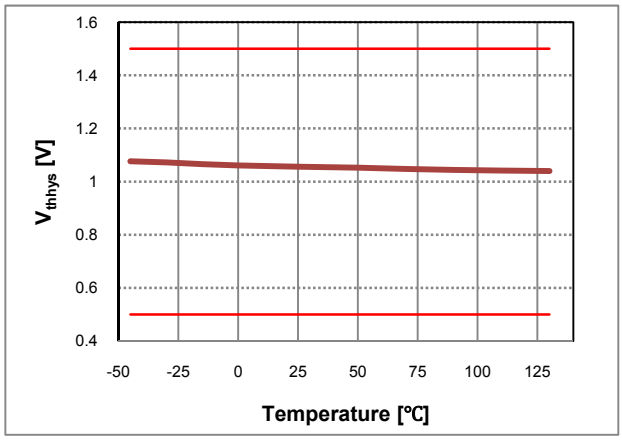

Figure 4. Start Threshold Voltage Hysteresis vs. Temperature

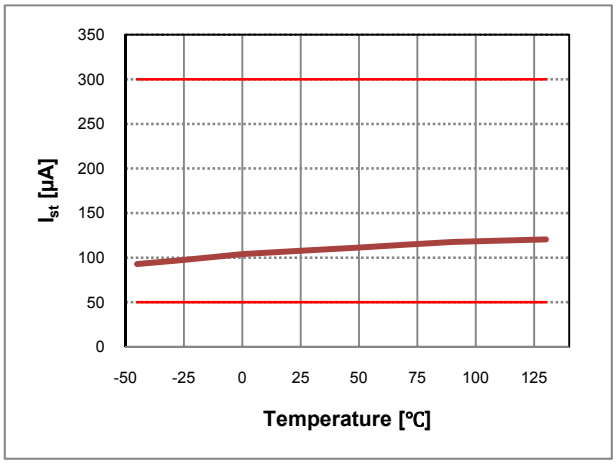

Figure 5. Startup Current vs. Temperature

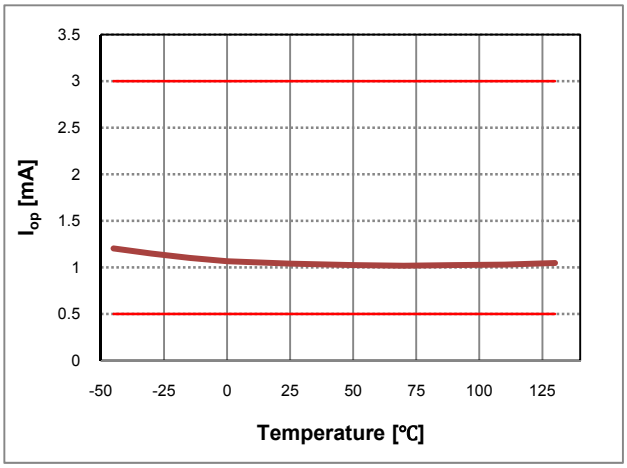

Figure 6. Operating Current vs. Temperature

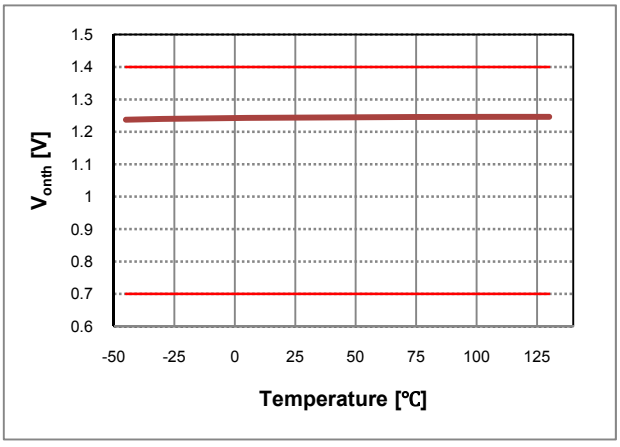

Figure 7. Enable Threshold Voltage vs. Temperature

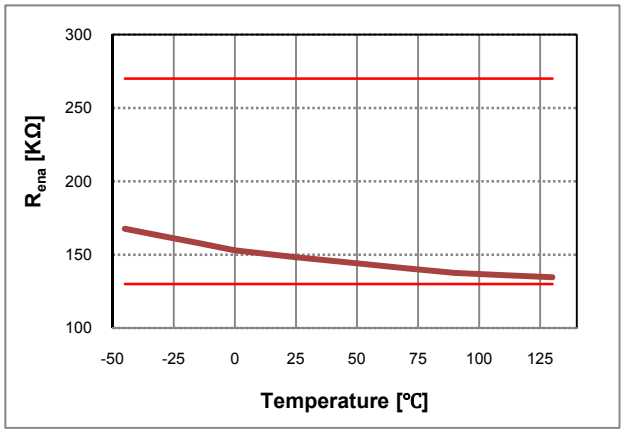

Figure 8. Pull-Down Resistor vs. Temperature

Typical Performance Characteristics (Continued)

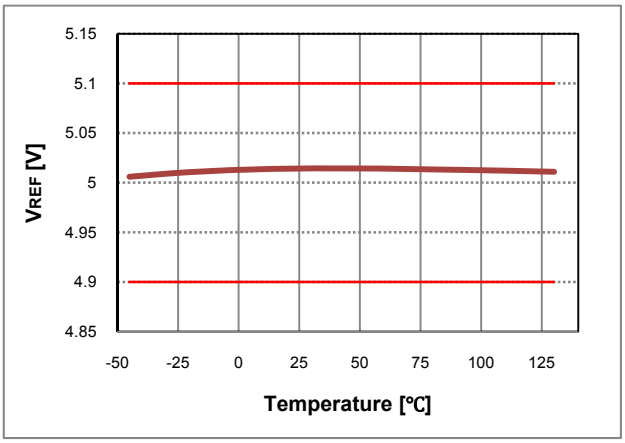

Figure 9. 5V Regulation Voltage vs. Temperature

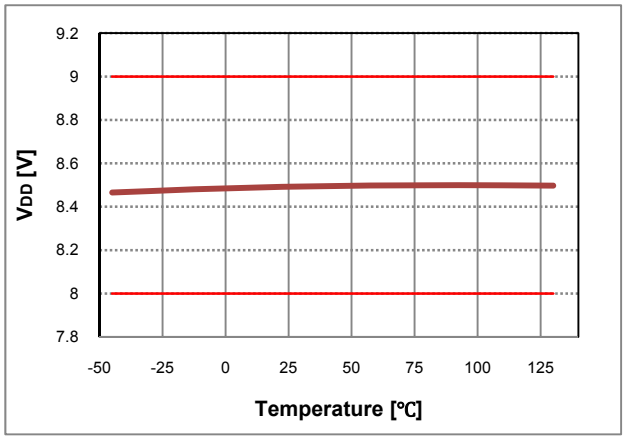

Figure 10. 8.5V Regulation Voltage vs. Temperature

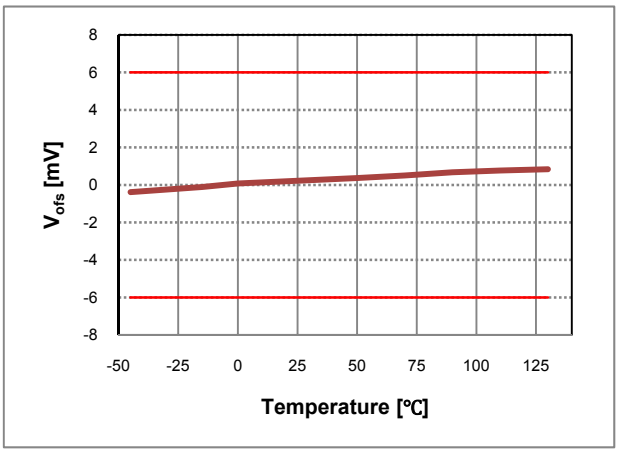

Figure 11. Offset of CH LED Current Reference Voltage vs. Temperature

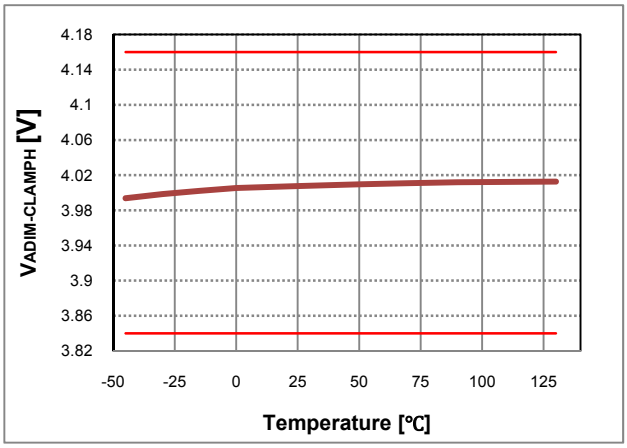

Figure 12. ADIM HIGH Clamping Voltage vs. Temperature

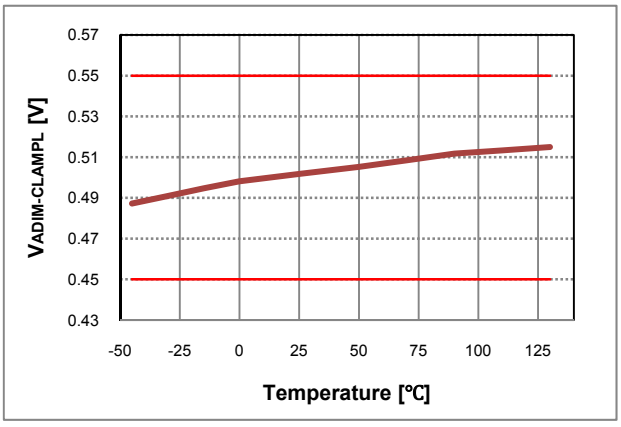

Figure 13. ADIM LOW Clamping Voltage vs. Temperature

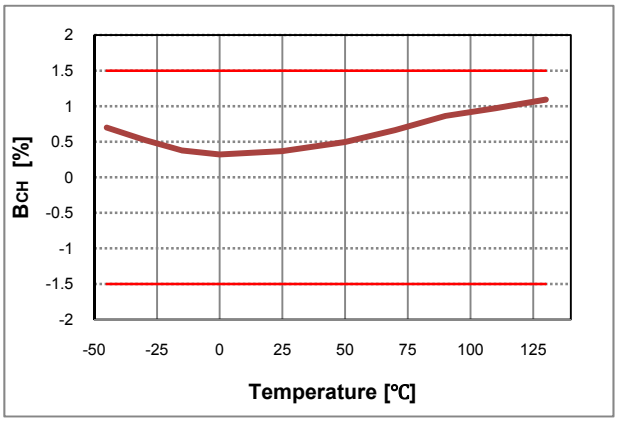

Figure 14. Current Balance Between Channels vs. Temperature

Typical Performance Characteristics (Continued)

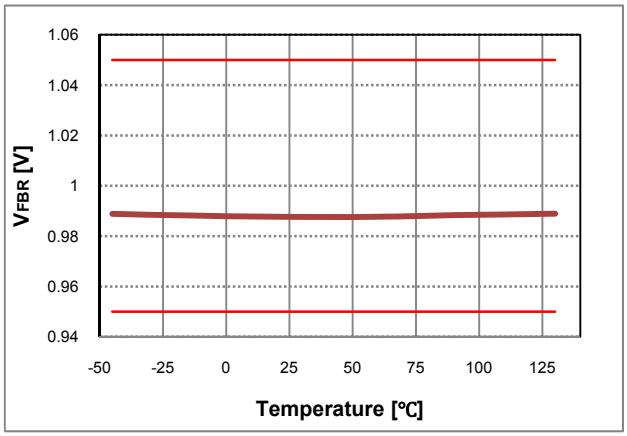

Figure 15. Feedback Reference Voltage vs. Temperature

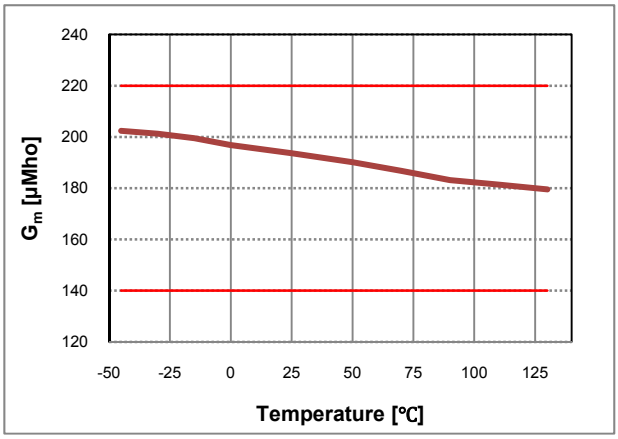

Figure 16. Error Amplifier Transconductance vs. Temperature

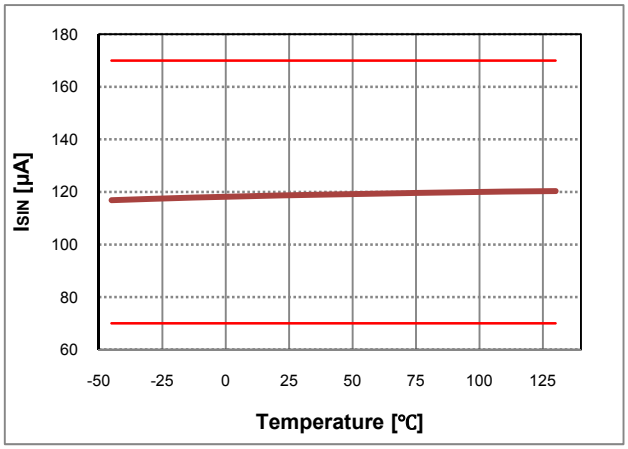

Figure 17. Error Amplifier Output Sink Current vs. Temperature

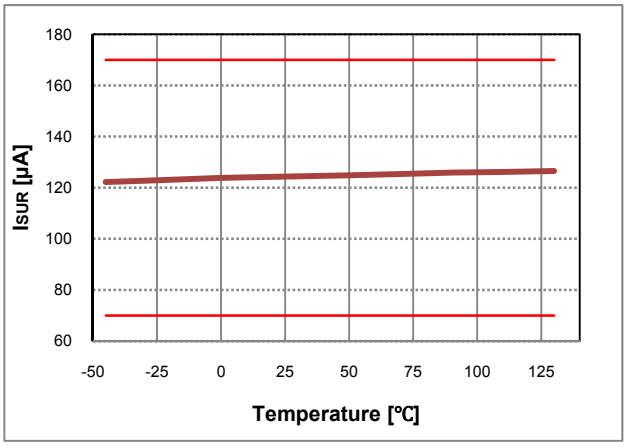

Figure 18. Error Amplifier Output Source current vs. Temperature

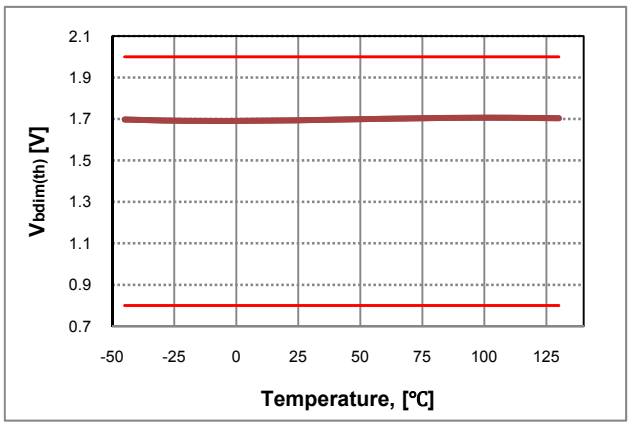

Figure 19. PWM Dimming On Threshold Voltage vs. Temperature

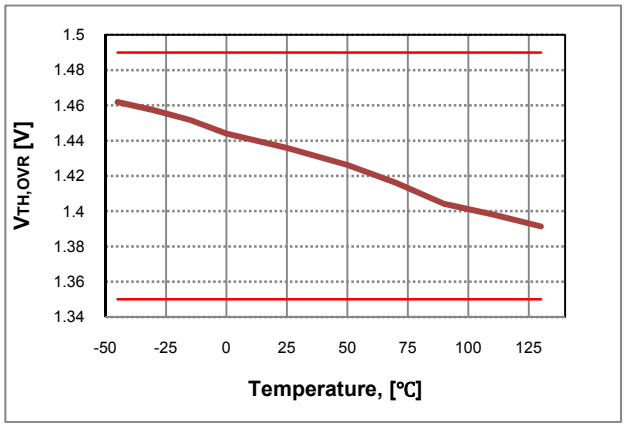

Figure 20. OVR Threshold Voltage vs. Temperature

Typical Performance Characteristics (Continued)

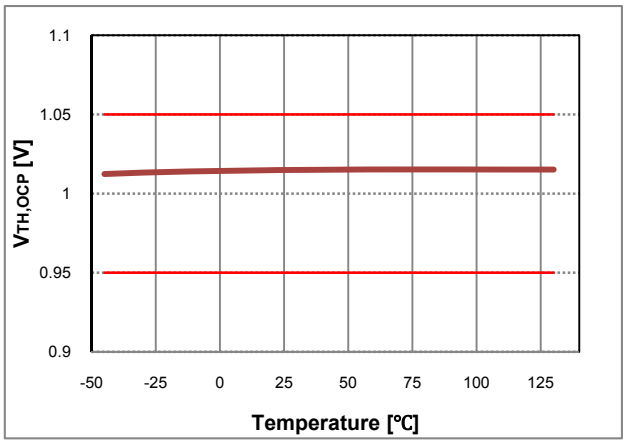

Figure 21. OCP Threshold Voltage vs. Temperature

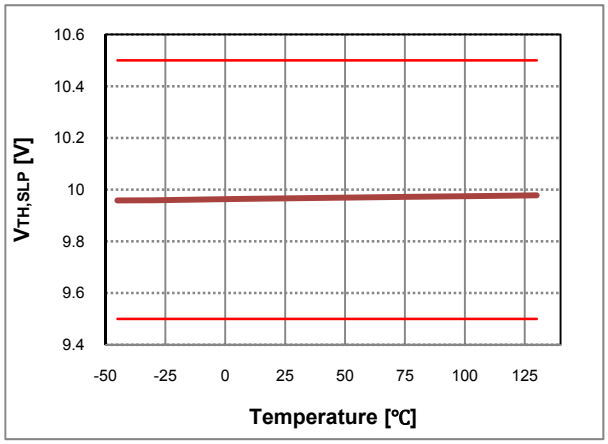

Figure 22. SLP Threshold Voltage vs. Temperature

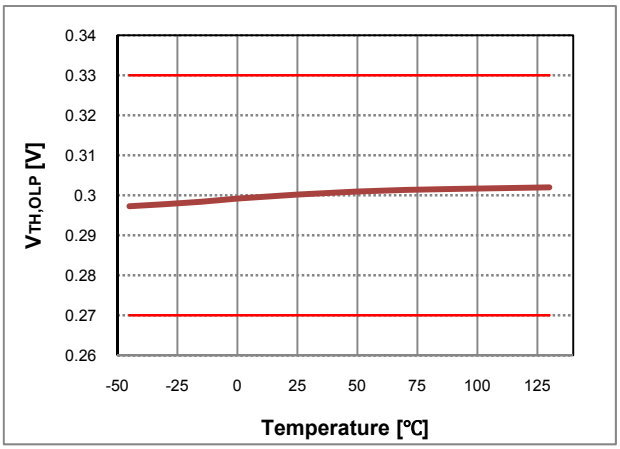

Figure 23. OLP Threshold Voltage vs. Temperature

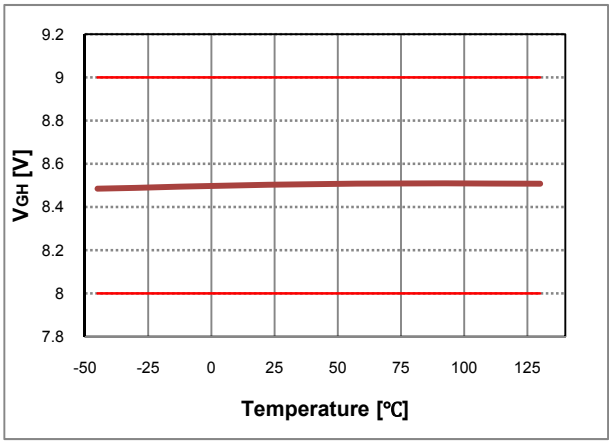

Figure 24. NMOS Gate High Voltage vs. Temperature

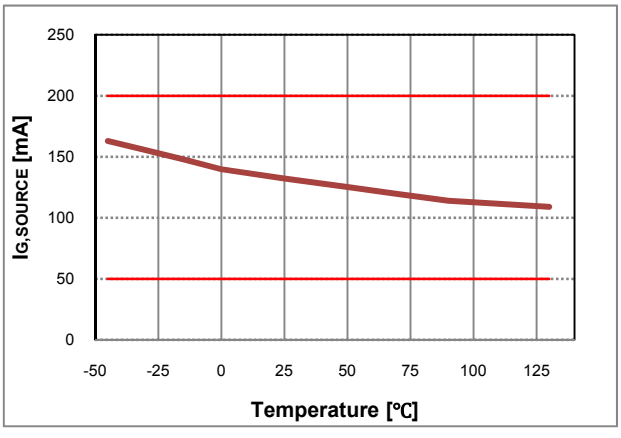

Figure 25. NMOS Gate Drive Source Current vs. Temperature

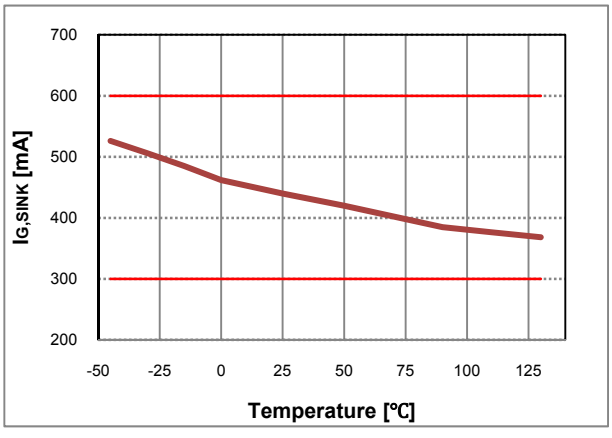

Figure 26. NMOS Gate Drive Sink Current vs. Temperature

Functional Description

The FAN7346 is a high-efficiency 4-channel LED driver. It can drive a 4-channel LED string with four external balance switches. It provides an integrated feedback for a DC-DC controller on the secondary side or on the flyback / LLC controller of the primary side.

Due to the high withstanding voltage of the sensing pin for drain voltage of external switch, the FAN7346 can be used in high-voltage LED string operation without any clamping circuit. Both MOSFET and transistor can be used as external balance switch, so the FAN7346 can drive a high-current LED string.

For four-string operation, the FAN7346 supports four individual PWM signal input pins. The FAN7346 can be operated by parallel connection mode.

For a primary-side direct-power control system, the FAN7346 supports an advanced power sequence and soft-start timing. LED driving voltage can be set before LED ignition for a reliable LED backlight ignition.

The FAN7346 supports various and programmable protections; Short-LED Protection (SLP), Open-LED Protection (OLP), Over-Current Protection (OCP), and Over-Voltage Regulation (OVR). Except OCP, all protection are auto-recovery / auto-restart. Except OVR, all protections are channel-individual protection. In case of SLP, OLP and OCP; even if some strings are in protection condition, other strings continues to operating for higher system reliability.

Figure 27 shows the work-flow of startup sequence.

1. Startup
When V_{CC} voltage is higher than UVLO threshold voltage, internal 5V regulation output is operated. At the same time, feedback starts to control OVR voltage as 1V. If OVR voltage is lower than 1V, feedback is pulled up. If OVR voltage is higher than 1V, feedback is pulled down.

After enable is applied, the FAN7346 begins soft-start procedure. The FAN7346 checks if OVR voltage is higher than 0.9V. If OVR voltage is lower than 0.9V, soft-start function is not started. If OVR voltage is higher than 0.9V, the FAN7346 starts LED current balance and soft-start. The LED current of each string is increased gradually for 10ms, which is fixed soft-start timing. During soft-start timing, SLP and OLP are disabled.

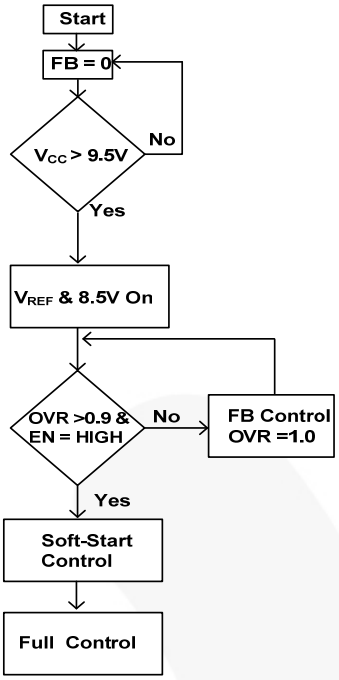

Figure 27. Startup Sequence

2. Feedback
After soft-start, the FAN7346 starts feedback drain-voltage of external balance switch.

Drain voltage of each channel is sensed on the CHx pin. CHx means any of the CH1 / CH2 / CH3 / CH4 pins. Minimum drain voltage is selected between four CHx voltages. The FAN7346 feeds back drain voltage to control minimum drain voltage at 1V.

If minimum drain voltage is higher than 1V, FB is pulled LOW. If minimum drain voltage is lower than 1V, FB is pulled HIGH.

Feedback response can be controlled by adding a resistor and capacitor to the CMP pin.

3. Analog Dimming
In the FAN7346, LED current can be modified by changing ADIM voltage.

LED current is controlled by the FBx pin voltage. FBx means any of the FB1 / FB2 / FB3 / FB4 pins. External current balance switch is operating in the saturation region to control LED current. Sensed voltage on the FBx pin is compared with internal reference voltage and the controller supplies a gate / base signal for the external current balance switch.

Internal reference voltage is decided by ADIM voltage. The formula for LED current calculation is:

$$I_{LED} = \frac{V_{ADIM}}{10 \times R_{SENSE}} \quad (1)$$

ADIM voltage is clamped internally from 0.5V to 4V. If ADIM voltage is lower than 0.5V, it is clamped as 0.5V. If ADIM voltage is higher than 4V, it is clamped as 4V.

4. PWM Dimming

The FAN7346 has four PWM dimming signal pins. Each PWM dimming pin controls an LED string.

If PWM dimming voltage is higher than 2V, an external balance switch is turned on and conducts constant current operation. If PWM dimming voltage is lower than 0.8V, an external balance switch is turned off and blocks LED current.

During PWM dimming off, open-LED protection and short-LED protection is disabled.

CHx drain voltage is sampled during PWM dimming on and held during PWM dimming off to maintain drain voltage regardless of dimming on/off signal.

5. Short-LED Protection (SLP)

To sense a short-LED condition, the FAN7346 uses the drain voltage of external balance switch. If some LEDs are shorted, its LED forward voltage is lower than other LED strings, so the drain voltage of the external balance switch is higher than other drain voltage.

SLP threshold voltage can be programmed by SLPR (Short-LED Protection Reference) voltage. Internal SLP threshold voltage is calculated as:

$$V_{SLP\_TH} = 10 * V_{SLPR} \quad (2)$$

Minimum SLP threshold voltage is 0V and maximum SLP threshold voltage is 45V.

SLP is a channel-individual protection. If any string is in SLP condition, the SLP strings is turned off and other string operate normally.

If the sensed-drain voltage (CHx voltage) is higher than the programmed threshold voltage for 20µs, CHx goes into short-LED protection, which forces the corresponding channel to turn off. To increase reliability, the SLP channel is restarted in the next PWM dimming signal rising timing. After restarting, the FAN7346 checks the drain voltage. If the drain voltage is higher than the SLP threshold voltage for 20µs, the switch is turned off. If drain voltage is lower, the channel is restored to normal operation. Shorted LED channel operation is minimum duty PWM dimming with a 20µs dimming on period. During 100% full duty PWM dimming, auto restart is not activated.

Figure 28 shows the SLP operation. As soon as SLPR*10 (blue line) is lower than CHx voltage, CHx is forced into minimum duty dimming operation.

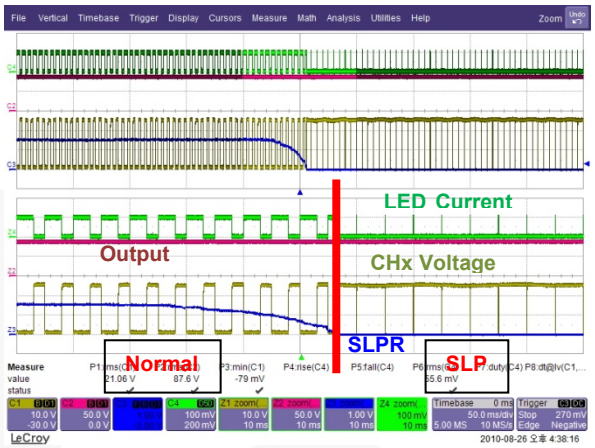

Figure 28. Short-LED Protection Operation

6. Open LED Protection (OLP)

To sensing open-LED condition, the FAN7346 use the drain voltage of an external balance switch. If an LED string is open, the drain voltage of external balance switch is grounded, and the FAN7346 can detect open-LED condition. OLP threshold voltage is 0.3V.

If CHx voltage is lower than 0.3V for 20µs, its drain-voltage feedback is pulled up to 5V. This means the open LED string is eliminated from minimum drain voltage feedback loop. Without OLP, if minimum drain voltage is 0V, drain voltage feedback forces the FB signal to increase output power. This can cause SLP or thermal stress in other channels.

OLP is an auto-recovery protection. As soon as drain voltage is higher than 0.3V, OLP is finished and the drain voltage feedback system is restored.

Figure 29 shows the OLP operation. Before open CH2, CH2 is the headroom channel. (CH2 drain voltage is minimum voltage – 1V.) As soon as open CH2, its drain voltage is 0V, OLP is activated, and CH2 is removed from headroom feedback control loop. CH1 is selected as minimum drain voltage channel, so its drain voltage is controlled as 1V. Reconnecting CH2 string, restores normal operation.

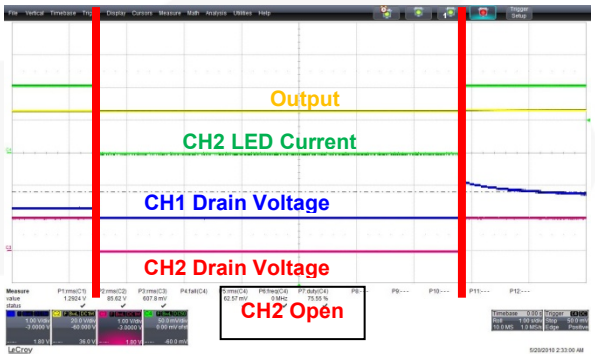

Figure 29. Open-LED Protection Operation

7. Over-Voltage Regulation (OVR)
To prevent LED driving voltage from exceeding the withstanding voltage of system components, the FAN7346 controls LED driving voltage with OVR pin voltage. The FAN7346 senses output LED driving voltage through the OVR pin voltage. Resistor divided output voltage is applied to the OVR pin voltage.

In FAN7346, OVR voltage uses two kinds of feedback and control: and regulating output voltage during enable off and clamping output voltage during enable on.

When ENA pin is LOW, the FAN7346 controls FB voltage to maintain OVR voltage as 1.0V. Through this output voltage control during ENA off, the FAN7346 reaches adequate LED driving voltage before turning ENA on.

After ENA pin is HIGH, OVR pin voltage is used for over-voltage regulation. If OVR pin voltage is lower than 1.42V, the FB pin voltage follows headroom control to maintain minimum voltage of drain voltages as 1V. If OVR pin voltage is higher than 1.42V, the FAN7346 controls FB (FB is pulled LOW). Through feedback regulation, OVR pin voltage cannot exceed 1.42V.

8. Over-Current Protection (OCP)
Through over-current protection, the FAN7346 can protect external balance switches from shorted over-current damage. To sense over-current condition, the FAN7346 monitors FBx (FB1~FB4) pin voltage.

If FBx voltage is higher than 1V for 20μs, CHx is considered an over-current condition. After sensing OCP condition, CHx dimming switch is turned off.

OCP is channel individual and latched protection. If one channel is in OCP condition, other channels keep operating. OCP channel is restarted after UVOL is reset.

9. Error Flag (FO)
To make error flag signal, the FAN7346 uses the FO pin. FO pin is open-drain type.

During normal operation, the FO pin is open. If using an external pull-up resistor, this signal is HIGH.

If used OLP / OCP / SLP protection, the FO pin is connected to ground. If using an external pull-up resistor, this signal is LOW.

If a single channel is in protection condition, error-flag signal is detected. Only if all channels are operating normally is the FO pin pulled HIGH.

Short Lamp Protection

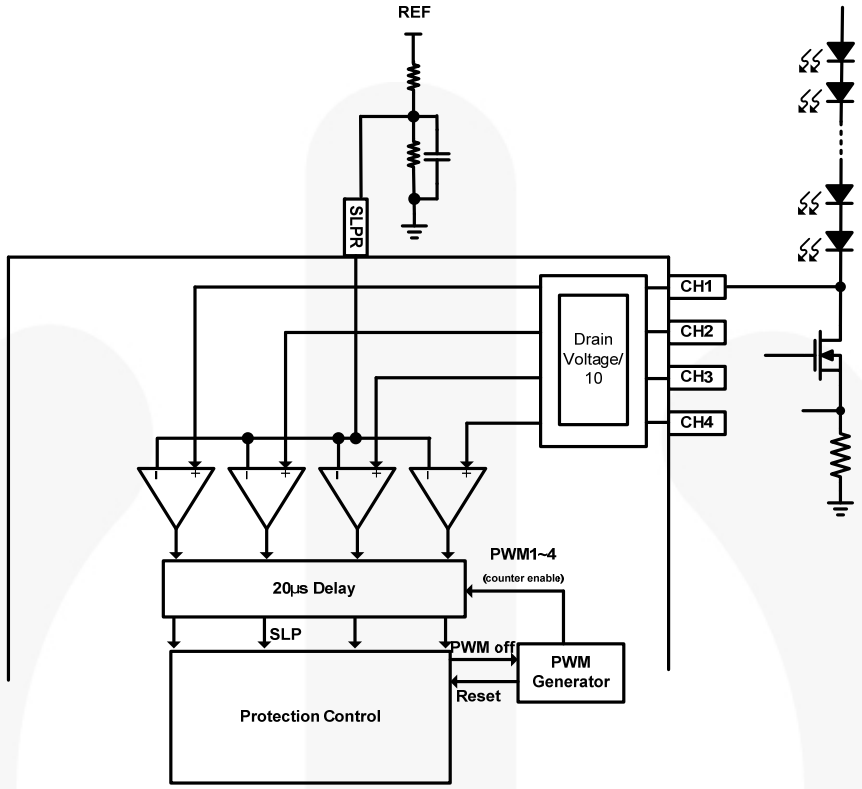

Figure 30. Block Diagram of Short LED Protection

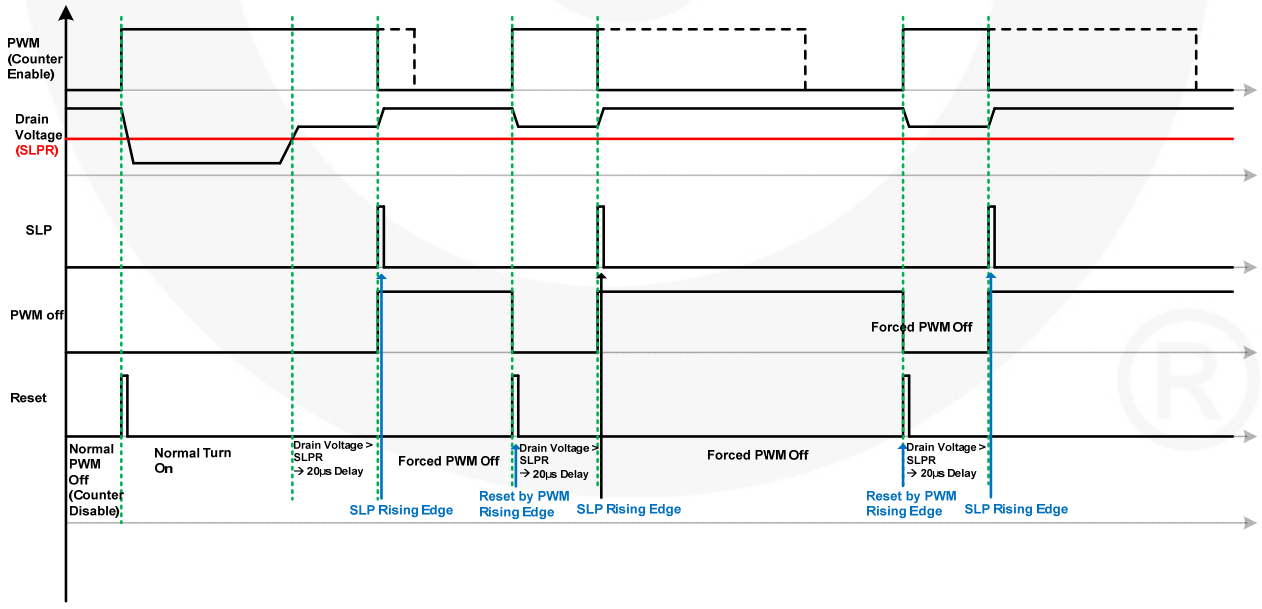

Figure 31. Timing Diagram of Short LED Protection

Typical Application Circuit (Backlight)

Application	Device	Input Voltage Range	LED String
32~46 Inch LED TV	FAN7346	380V	8-String / 90V / 100mA

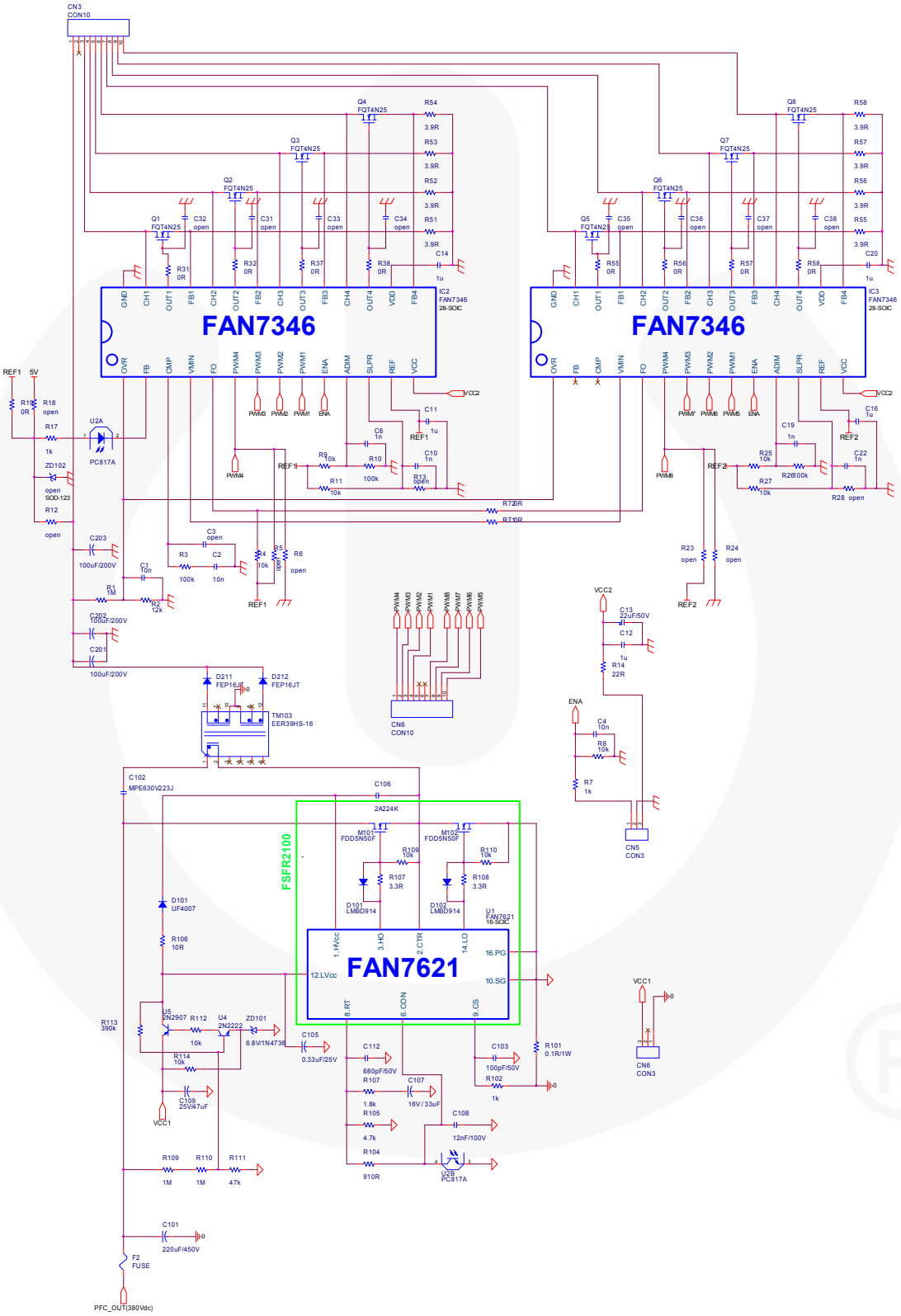

Figure 32. LCD Backlight Driver

Typical Application Circuit (Lighting) (Continued)

Application	Device	Input Voltage Range	LED String
LED Lighting	FAN7346	380V	4-String

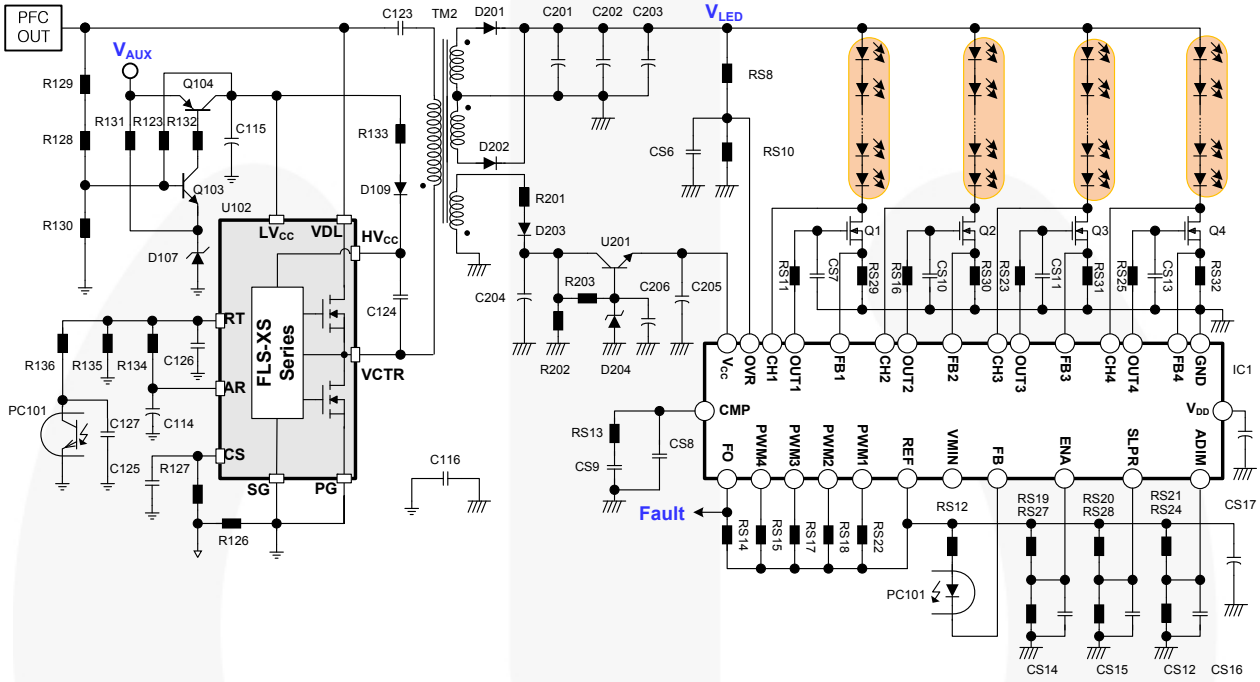

Figure 33. LED Lighting Driver

Typical Application Circuit (Continued)

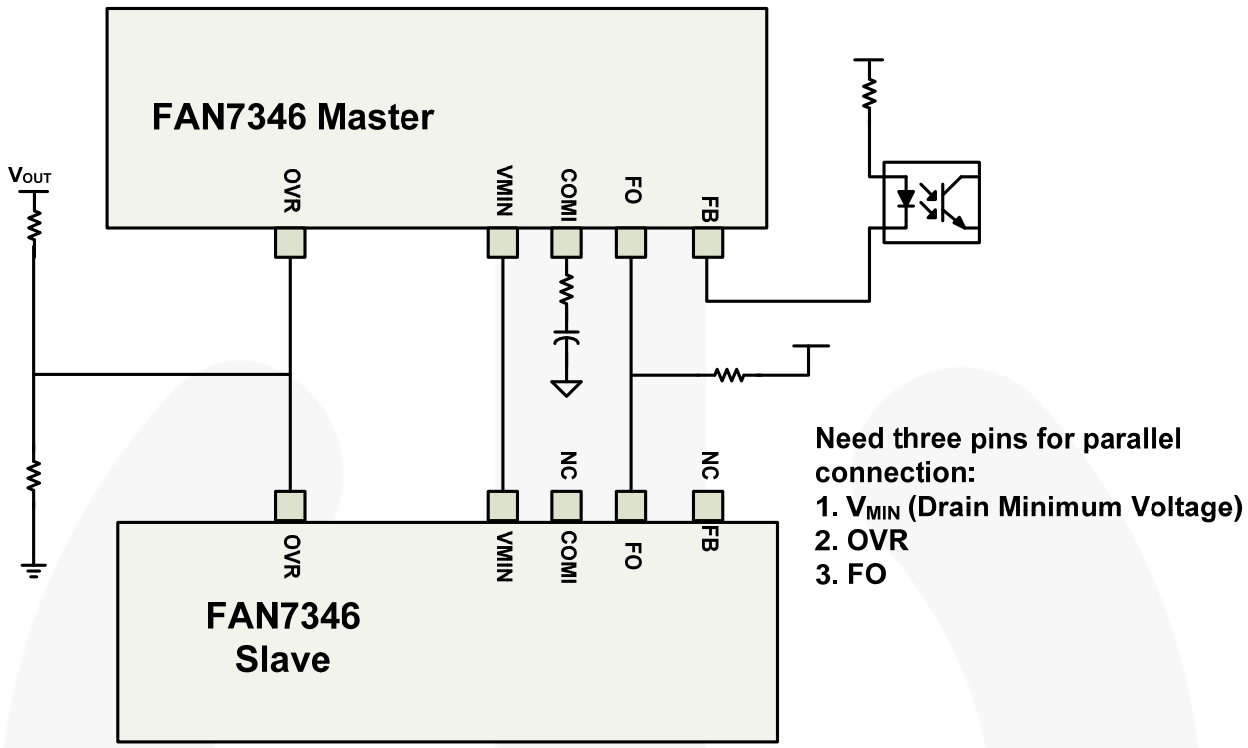

Figure 34. Multiple Controller Driving

Physical Dimensions

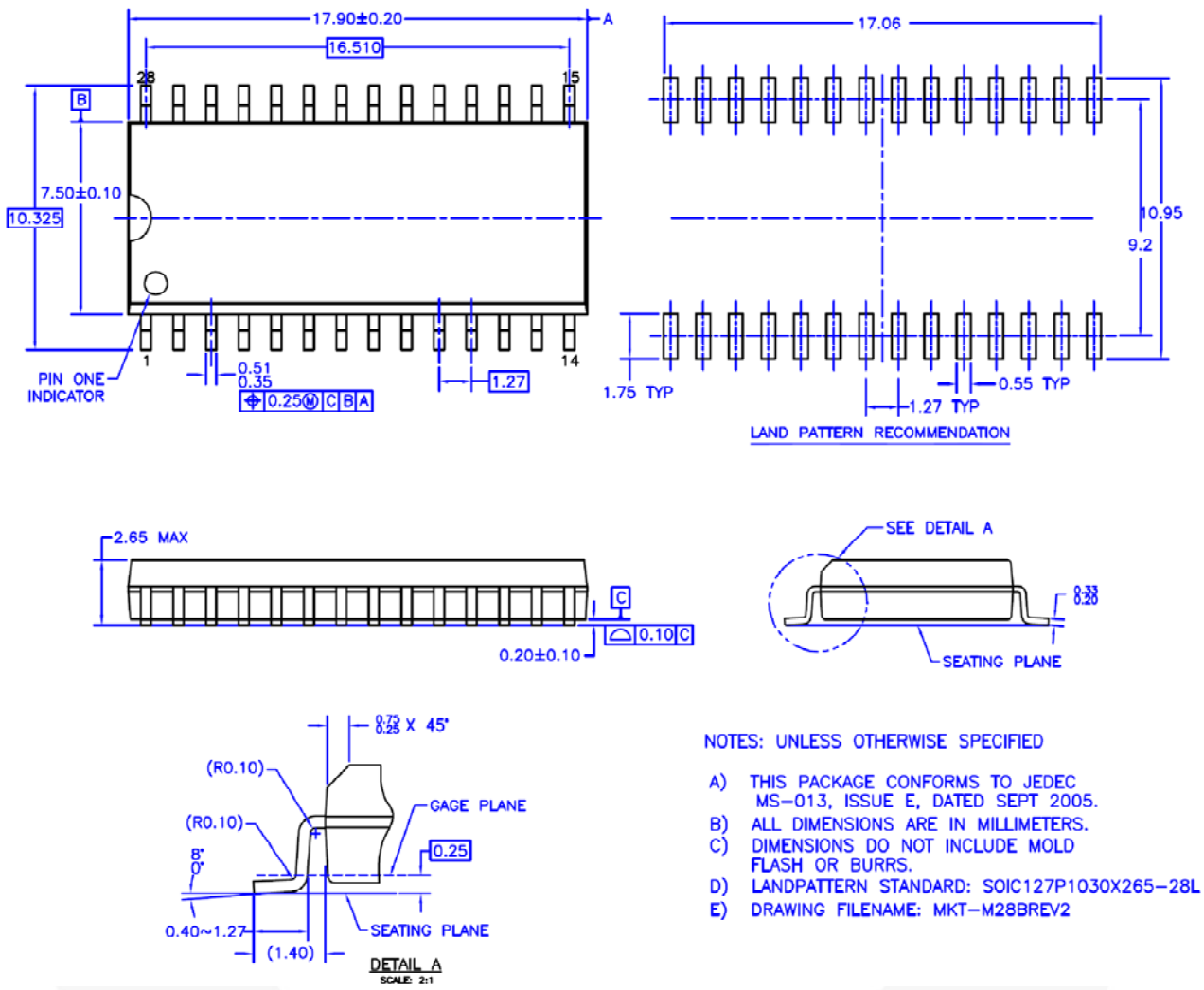

Figure 35. 28-Lead, Small-Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300-Inch, Wide Body

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