



FDB0260N1007L

N-Channel PowerTrench[®] MOSFET

100 V, 200 A, 2.6 mΩ

Features

- Max $r_{DS(on)} = 2.6\text{ m}\Omega$ at $V_{GS} = 10\text{ V}$, $I_D = 27\text{ A}$
- Fast Switching Speed
- Low Gate Charge
- High Performance Trench Technology for Extremely Low $R_{DS(on)}$
- High Power and Current Handling Capability
- RoHS Compliant

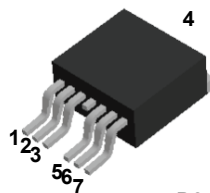


General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advance PowerTrench[®] process that has been especially tailored to minimize the on-state resistance while maintaining superior ruggedness and switching performance for industrial applications.

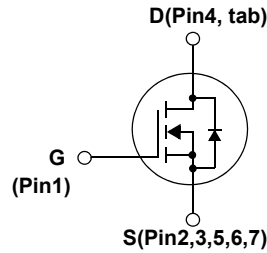
Applications

- Industrial Motor Drive
- Industrial Power Supply
- Industrial Automation
- Battery Operated tools
- Battery Protection
- Solar Inverters
- UPS and Energy Inverters
- Energy Storage
- Load Switch



1. Gate
2. Source/Kelvin Sense
3. Source/Kelvin Sense
4. Drain
5. Source
6. Source
7. Source

D2-PAK
(TO263)



MOSFET Maximum Ratings $T_C = 25\text{ }^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	100	V
V_{GS}	Gate to Source Voltage	± 20	V
I_D	Drain Current -Continuous	$T_C = 25\text{ }^\circ\text{C}$ (Note 5)	200
	-Continuous	$T_C = 100\text{ }^\circ\text{C}$ (Note 5)	140
	-Pulsed	(Note 4)	1100
E_{AS}	Single Pulse Avalanche Energy	(Note 3)	912 mJ
P_D	Power Dissipation	$T_C = 25\text{ }^\circ\text{C}$	250
	Power Dissipation	$T_A = 25\text{ }^\circ\text{C}$ (Note 1a)	3.8
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +175	$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	(Note 1)	0.6	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	40	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDB0260N1007L	FDB0260N1007L	D2-PAK-7L	330 mm	24 mm	800 units

Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}, V_{GS} = 0\text{ V}$	100			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$		53		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 80\text{ V}, V_{GS} = 0\text{ V}$			1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$			± 100	nA

On Characteristics (Note 2)

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\text{ }\mu\text{A}$	2	2.8	4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$		-13		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 27\text{ A}$ $V_{GS} = 10\text{ V}, I_D = 27\text{ A}, T_J = 150\text{ }^\circ\text{C}$		2.3 4.5	2.6 6.6	m Ω
g_{FS}	Forward Transconductance	$V_{DS} = 10\text{ V}, I_D = 27\text{ A}$		59		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 50\text{ V}, V_{GS} = 0\text{ V},$ $f = 1\text{ MHz}$		6101	8545	pF
C_{oss}	Output Capacitance			1343	1885	pF
C_{rss}	Reverse Transfer Capacitance			46	65	pF
R_g	Gate Resistance			2.7		Ω

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 50\text{ V}, I_D = 27\text{ A},$ $V_{GS} = 10\text{ V}, R_{GEN} = 6\text{ }\Omega$		30	48	ns
t_r	Rise Time			29	46	ns
$t_{d(off)}$	Turn-Off Delay Time			51	81	ns
t_f	Fall Time			19	34	ns
Q_g	Total Gate Charge			84	118	nC
Q_{gs}	Gate to Source Gate Charge	$V_{DD} = 50\text{ V}, I_D = 27\text{ A},$ $V_{GS} = 10\text{ V}$		25		nC
Q_{gd}	Gate to Drain "Miller" Charge			17		nC

Drain-Source Diode Characteristics

I_S	Maximum Continuous Drain to Source Diode Forward Current			200	A	
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current			1100	A	
V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 27\text{ A}$ (Note 2)		0.8	1.2	V
t_{rr}	Reverse Recovery Time	$I_F = 27\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		75	120	ns
Q_{rr}	Reverse Recovery Charge			97	155	nC

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

- a) $40\text{ }^\circ\text{C/W}$ when mounted on a 1 in^2 pad of 2 oz copper.
- b) $62.5\text{ }^\circ\text{C/W}$ when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < $300\text{ }\mu\text{s}$, Duty cycle < 2.0 %.

3. E_{AS} of 912 is based on starting $T_J = 25\text{ }^\circ\text{C}$, $L = 0.3\text{ mH}$, $I_{AS} = 78\text{ A}$, $V_{DD} = 10\text{ V}$, $V_{GS} = 90\text{ V}$. 100% test at $L = 0.1\text{ mH}$, $I_{AS} = 113\text{ A}$.

4. Pulsed I_d please refer to Figure "Forward Bias Safe Operating Area" for more details.

5. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted.

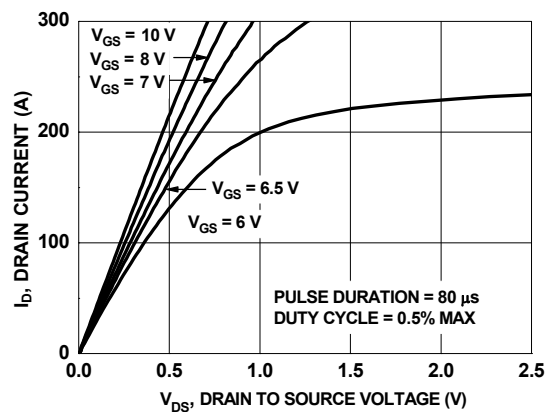


Figure 1. On Region Characteristics

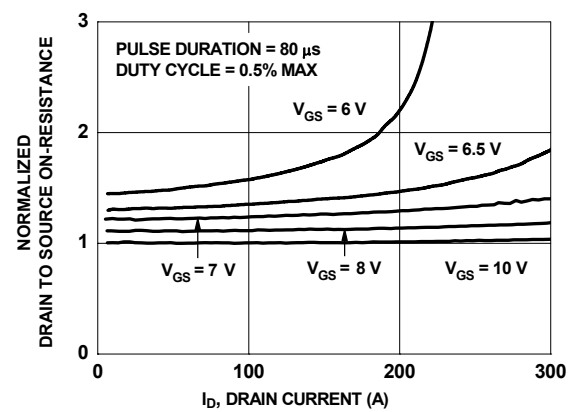


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

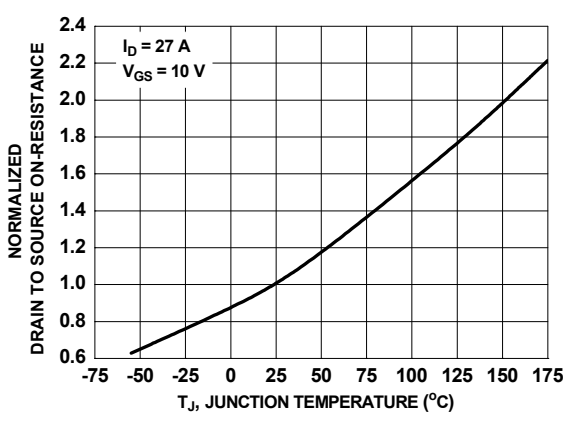


Figure 3. Normalized On Resistance vs. Junction Temperature

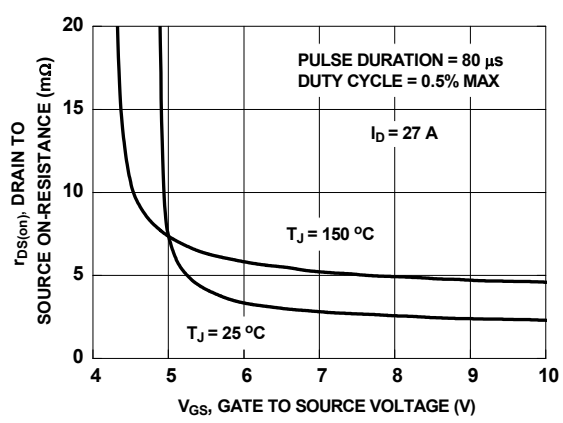


Figure 4. On-Resistance vs. Gate to Source Voltage

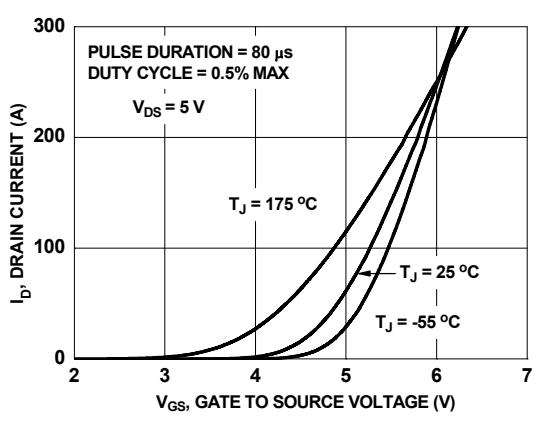


Figure 5. Transfer Characteristics

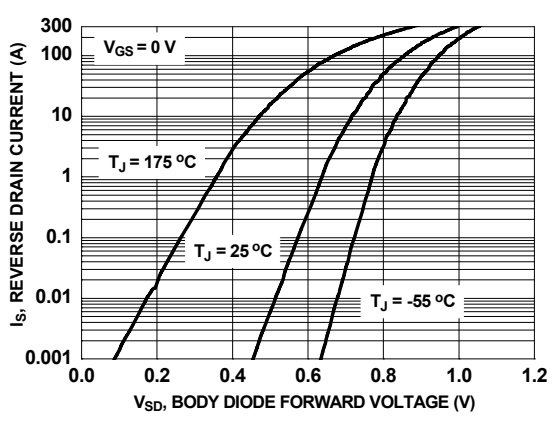


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted.

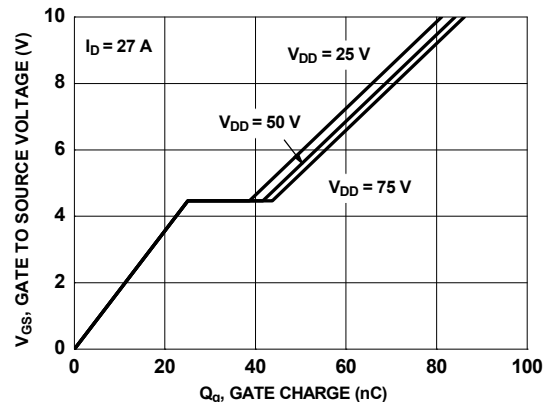


Figure 7. Gate Charge Characteristics

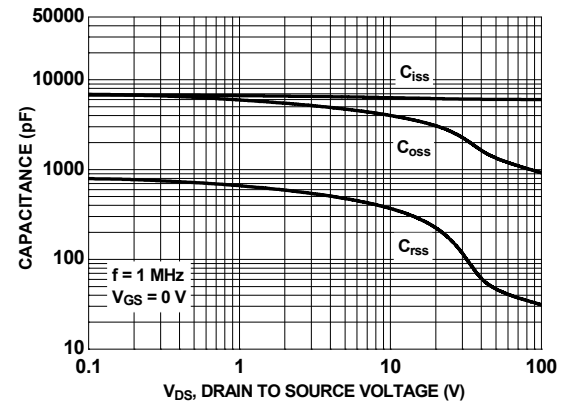


Figure 8. Capacitance vs. Drain to Source Voltage

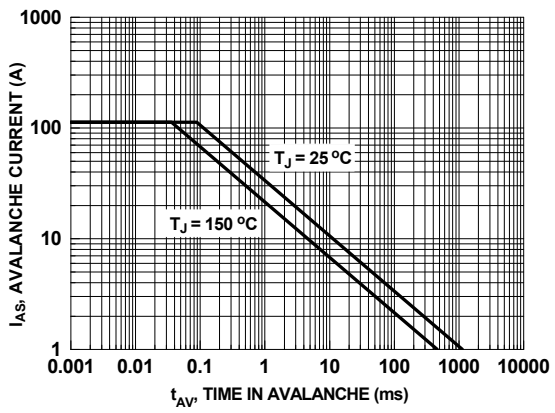


Figure 9. Unclamped Inductive Switching Capability

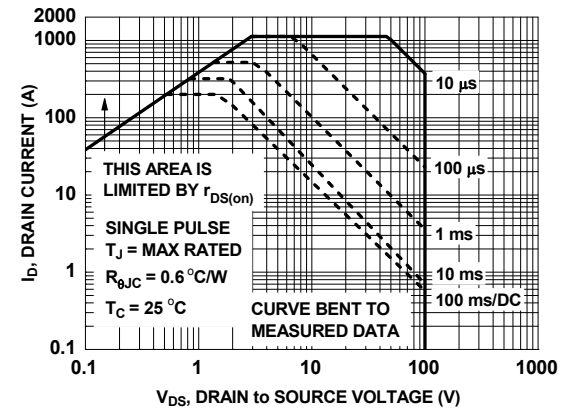


Figure 10. Forward Bias Safe Operating Area

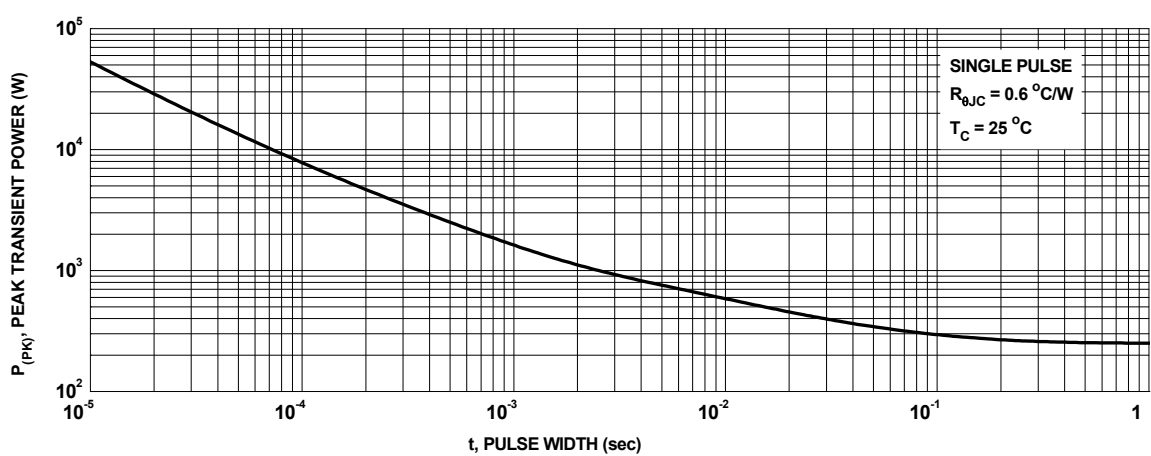


Figure 11. Single Pulse Maximum Power Dissipation

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted.

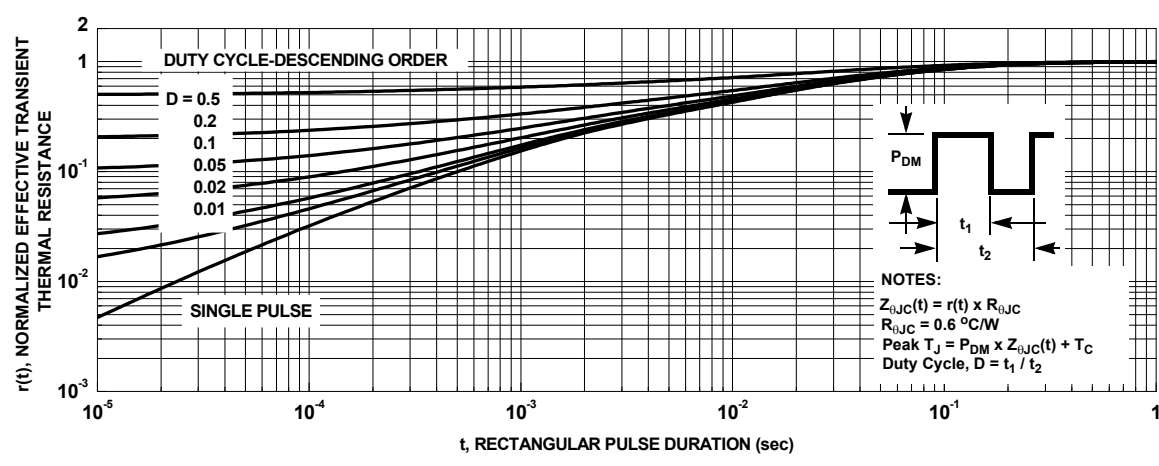
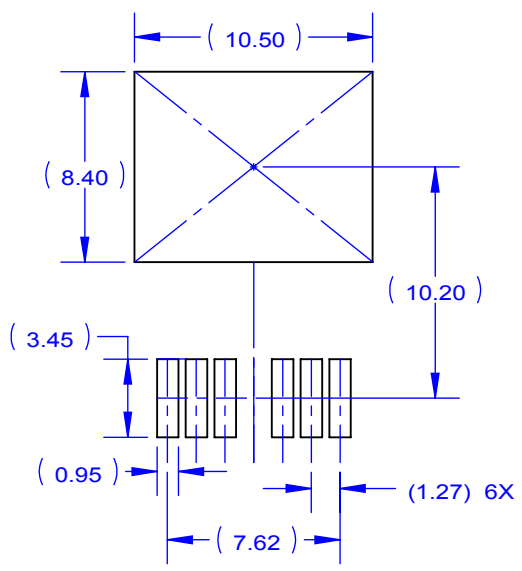
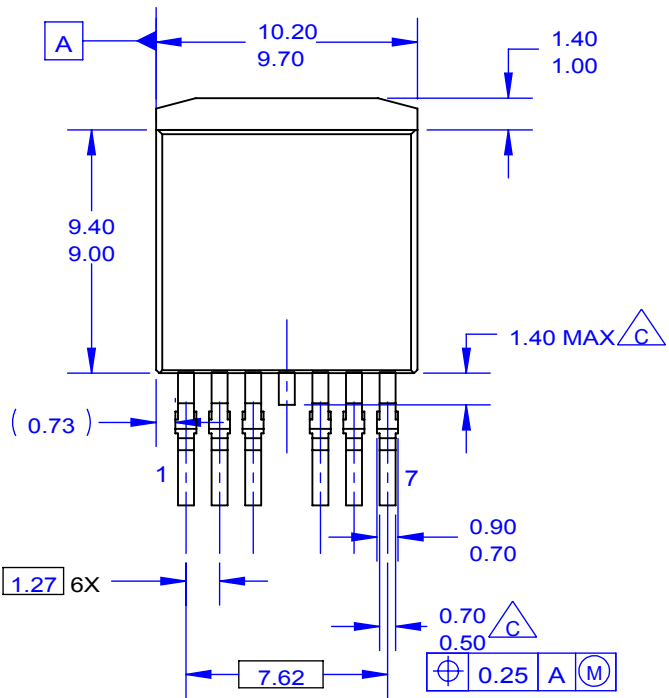
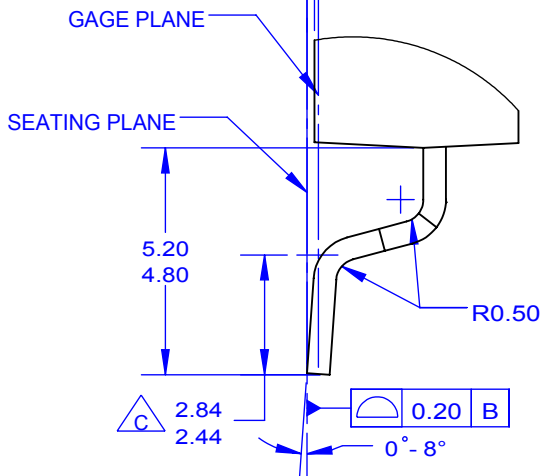
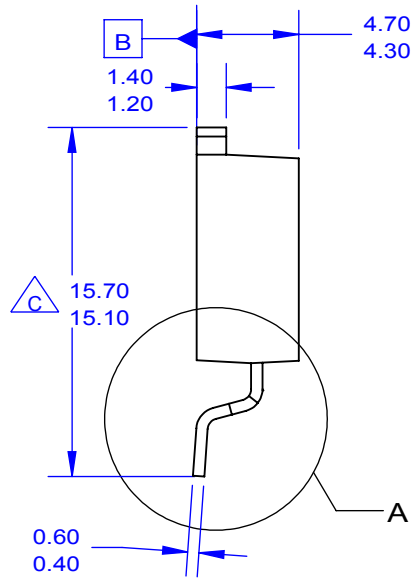
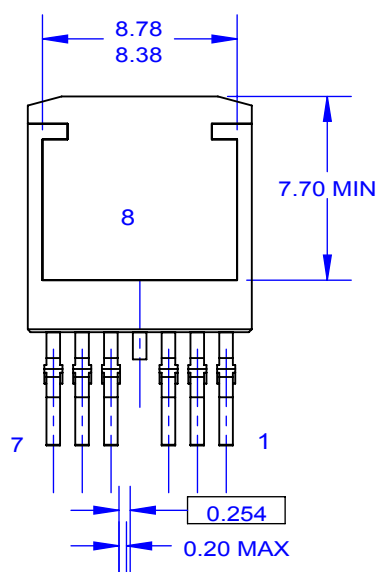


Figure 12. Junction-to-Case Transient Thermal Response Curve



LAND PATTERN RECOMMENDATION



DETAIL A
SCALE 2:1

NOTES:

- A. PACKAGE CONFORMS TO JEDEC TO-263 VARIATION CB EXCEPT WHERE NOTED.
- B. ALL DIMENSIONS ARE IN MILLIMETERS.
- $\triangle C$ OUT OF JEDEC STANDARD VALUE.
- D. DIMENSION AND TOLERANCE AS PER ASME Y14.5-1994.
- E. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
- F. LAND PATTERN RECOMMENDATION PER IPC TO127P1524X465-8N.
- G. DRAWING FILE NAME: TO263A07REV5.



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Datasheet Identification	Product Status	Definition
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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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