

# FDH3632 / FDP3632 / FDB3632

## N-Channel PowerTrench® MOSFET

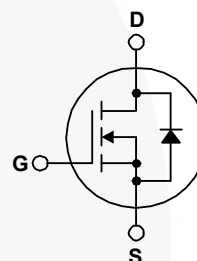
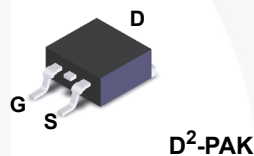
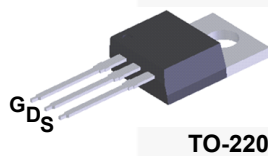
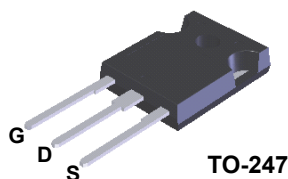
100 V, 80 A, 9 mΩ

### Features

- $R_{DS(ON)} = 7.5 \text{ m}\Omega$  (Typ.),  $V_{GS} = 10 \text{ V}$ ,  $I_D = 80 \text{ A}$
- $Q_g(\text{tot}) = 84 \text{ nC}$  (Typ.),  $V_{GS} = 10 \text{ V}$
- Low Miller Charge
- Low  $Q_{rr}$  Body Diode
- UIS Capability (Single Pulse and Repetitive Pulse)
- RoHS Compliant

### Applications

- Synchronous Rectification
- Battery Protection Circuit
- Motor Drives and Uninterruptible Power Supplies
- Micro Solar Inverter



### MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	FDH3632 / FDP3632 / FDB3632	Unit
$V_{DSS}$	Drain to Source Voltage	100	V
$V_{GS}$	Gate to Source Voltage	$\pm 20$	V
$I_D$	Drain Current	80	A
	Continuous ( $T_C < 111^\circ\text{C}$ , $V_{GS} = 10\text{V}$ )		
	Continuous ( $T_{amb} = 25^\circ\text{C}$ , $V_{GS} = 10\text{V}$ , $R_{\theta JA} = 43^\circ\text{C/W}$ )		
	Pulsed	Figure 4	A
$E_{AS}$	Single Pulse Avalanche Energy (Note 1)	337	mJ
$P_D$	Power dissipation	310	W
	Derate above $25^\circ\text{C}$	2.07	W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature	-55 to 175	$^\circ\text{C}$

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance Junction to Case, Max. TO-220, D²-PAK, TO-247	0.48	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient, Max. TO-220 (Note 2)	62	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient D²-PAK, Max. 1in² copper pad area	43	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient, Max. TO-247 (Note 2)	30	$^\circ\text{C/W}$

## Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDB3632	FDB3632	D <sup>2</sup> -PAK	330 mm	24 mm	800 units
FDP3632	FDP3632	TO-220	Tube	N/A	50 units
FDH3632	FDH3632	TO-247	Tube	N/A	30 units

## Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$B_{VDSS}$	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}$ , $V_{GS} = 0\text{V}$	100	-	-	V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 80\text{V}$ $V_{GS} = 0\text{V}$ $T_C = 150^\circ\text{C}$	-	-	1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{V}$	-	-	$\pm 100$	nA

### On Characteristics

$V_{GS(TH)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250\mu\text{A}$	2	-	4	V
$r_{DS(ON)}$	Drain to Source On Resistance	$I_D = 80\text{A}$ , $V_{GS} = 10\text{V}$	-	0.0075	0.009	$\Omega$
		$I_D = 40\text{A}$ , $V_{GS} = 6\text{V}$ ,	-	0.009	0.015	
		$I_D = 80\text{A}$ , $V_{GS} = 10\text{V}$ , $T_C = 175^\circ\text{C}$	-	0.018	0.022	

### Dynamic Characteristics

$C_{ISS}$	Input Capacitance	$V_{DS} = 25\text{V}$ , $V_{GS} = 0\text{V}$ , $f = 1\text{MHz}$	-	6000	-	pF
$C_{OSS}$	Output Capacitance		-	820	-	pF
$C_{RSS}$	Reverse Transfer Capacitance		-	200	-	pF
$Q_{g(TOT)}$	Total Gate Charge at 10V	$V_{GS} = 0\text{V}$ to 10V	-	84	110	nC
$Q_{g(TH)}$	Threshold Gate Charge	$V_{GS} = 0\text{V}$ to 2V	-	11	14	nC
$Q_{gs}$	Gate to Source Gate Charge	$V_{DD} = 50\text{V}$ $I_D = 80\text{A}$ $I_g = 1.0\text{mA}$	-	30	-	nC
$Q_{gs2}$	Gate Charge Threshold to Plateau		-	20	-	nC
$Q_{gd}$	Gate to Drain "Miller" Charge		-	20	-	nC

### Resistive Switching Characteristics ( $V_{GS} = 10\text{V}$ )

$t_{ON}$	Turn-On Time	$V_{DD} = 50\text{V}$ , $I_D = 80\text{A}$ $V_{GS} = 10\text{V}$ , $R_{GS} = 3.6\Omega$	-	-	102	ns
$t_{d(ON)}$	Turn-On Delay Time		-	30	-	ns
$t_r$	Rise Time		-	39	-	ns
$t_{d(OFF)}$	Turn-Off Delay Time		-	96	-	ns
$t_f$	Fall Time		-	46	-	ns
$t_{OFF}$	Turn-Off Time		-	-	213	ns

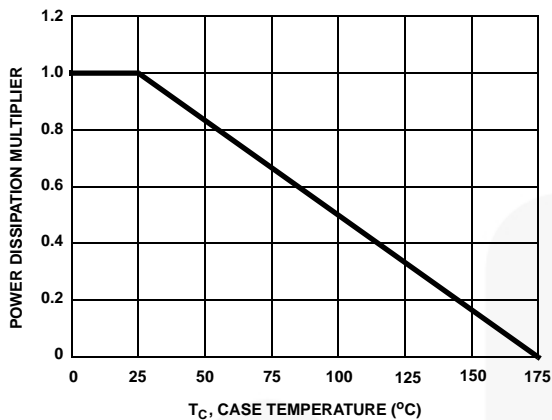
### Drain-Source Diode Characteristics

$V_{SD}$	Source to Drain Diode Voltage	$I_{SD} = 80\text{A}$	-	-	1.25	V
		$I_{SD} = 40\text{A}$	-	-	1.0	V
$t_{rr}$	Reverse Recovery Time	$I_{SD} = 75\text{A}$ , $di_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	64	ns
$Q_{RR}$	Reverse Recovered Charge	$I_{SD} = 75\text{A}$ , $di_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	120	nC

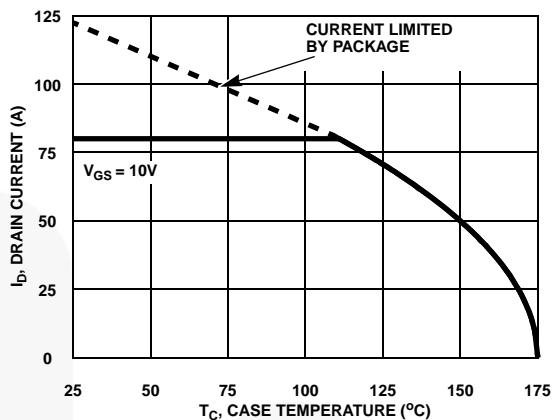
#### Notes:

- Starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.12\text{mH}$ ,  $I_{AS} = 75\text{A}$ ,  $V_{DD} = 80\text{V}$ .
- Pulse Width = 100s

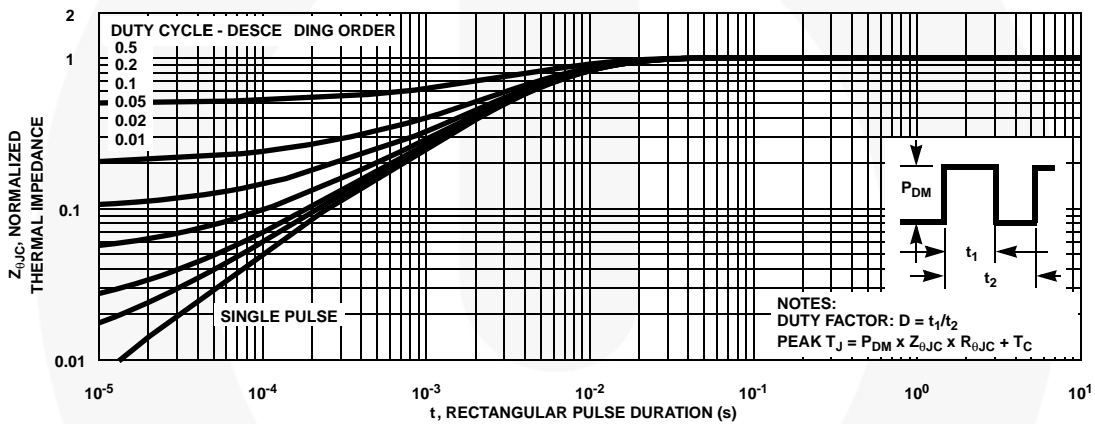
**Typical Characteristics**  $T_C = 25^\circ\text{C}$  unless otherwise noted



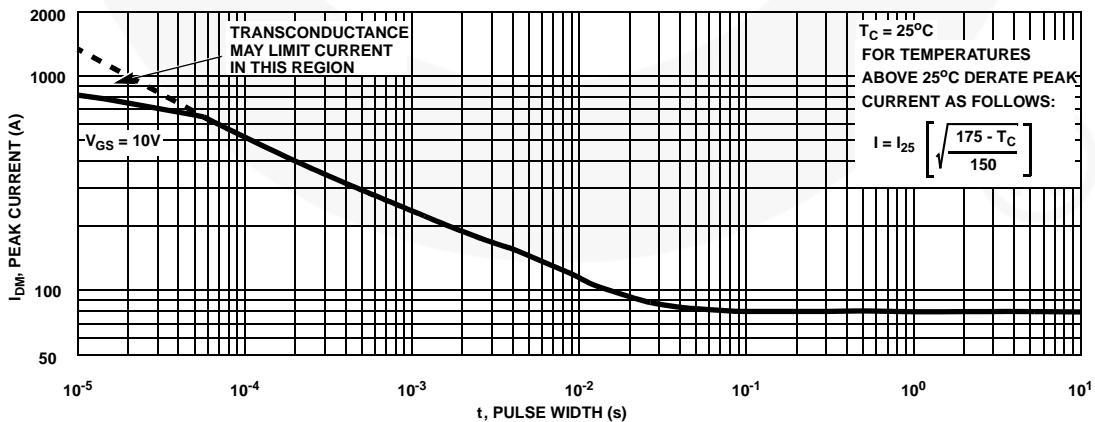
**Figure 1. Normalized Power Dissipation vs Ambient Temperature**



**Figure 2. Maximum Continuous Drain Current vs Case Temperature**

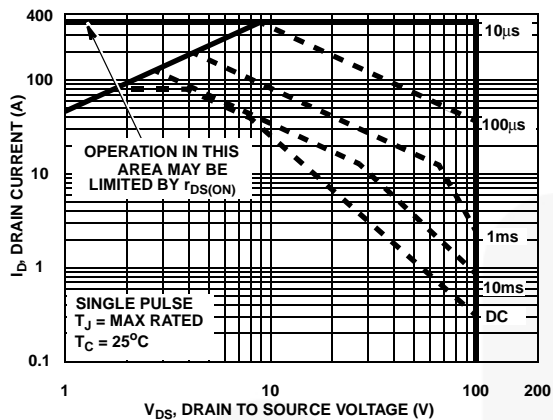


**Figure 3. Normalized Maximum Transient Thermal Impedance**

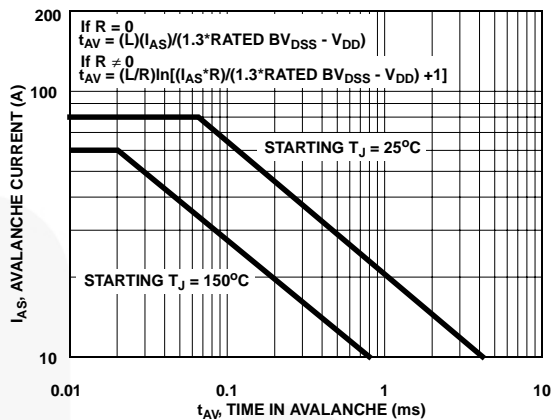


**Figure 4. Peak Current Capability**

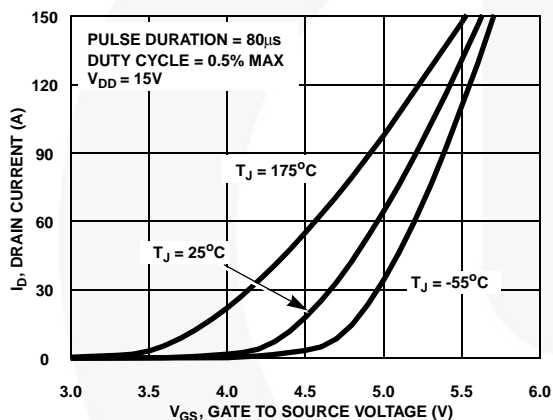
**Typical Characteristics**  $T_C = 25^\circ\text{C}$  unless otherwise noted



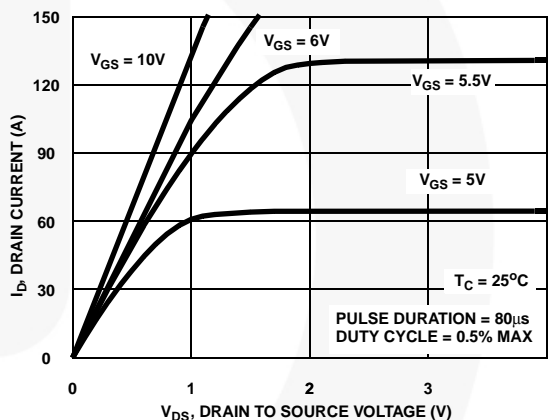
**Figure 5. Forward Bias Safe Operating Area**



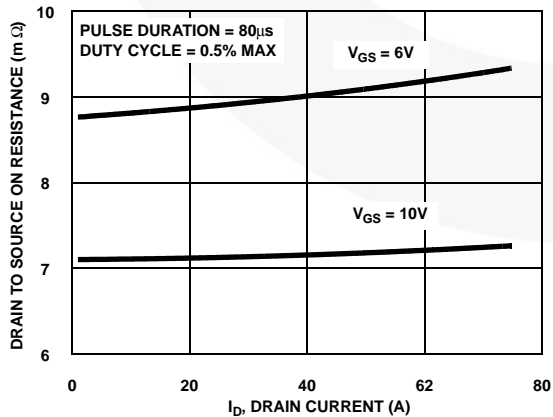
NOTE: Refer to Fairchild Application Notes AN7514 and AN7515  
**Figure 6. Unclamped Inductive Switching Capability**



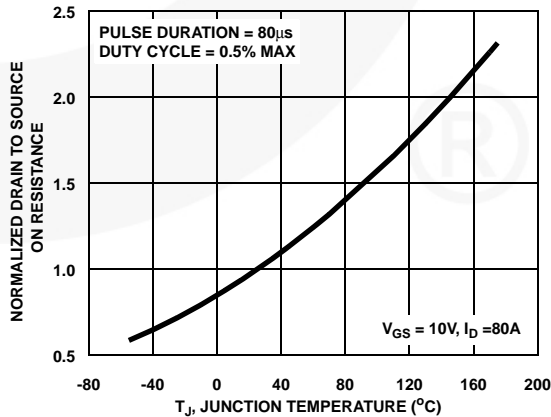
**Figure 7. Transfer Characteristics**



**Figure 8. Saturation Characteristics**

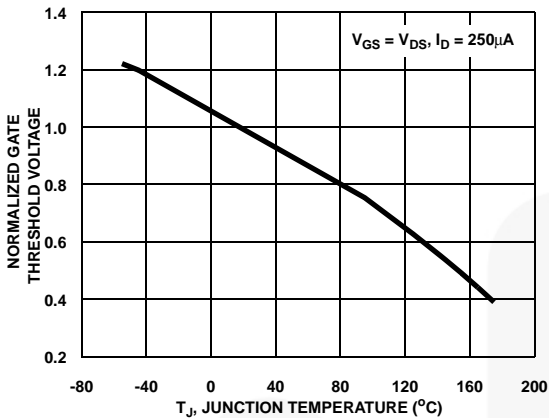


**Figure 9. Drain to Source On Resistance vs Drain Current**

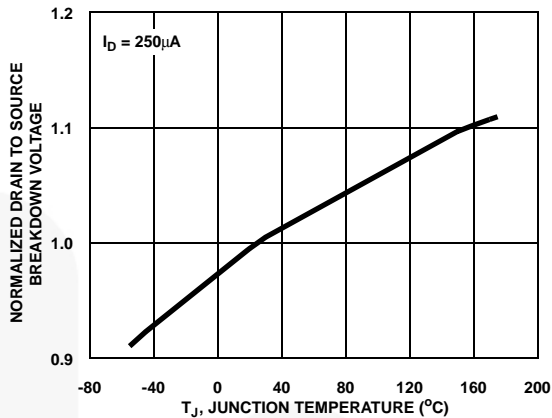


**Figure 10. Normalized Drain to Source On Resistance vs Junction Temperature**

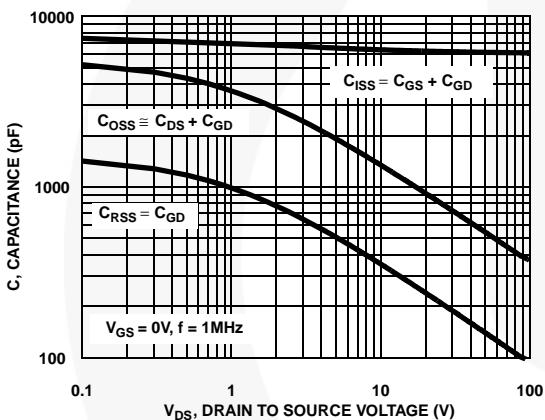
**Typical Characteristics**  $T_C = 25^\circ\text{C}$  unless otherwise noted



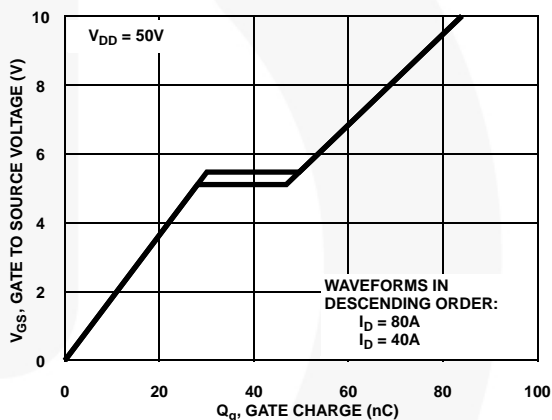
**Figure 11. Normalized Gate Threshold Voltage vs Junction Temperature**



**Figure 12. Normalized Drain to Source Breakdown Voltage vs Junction Temperature**



**Figure 13. Capacitance vs Drain to Source Voltage**



**Figure 14. Gate Charge Waveforms for Constant Gate Currents**

### Test Circuits and Waveforms

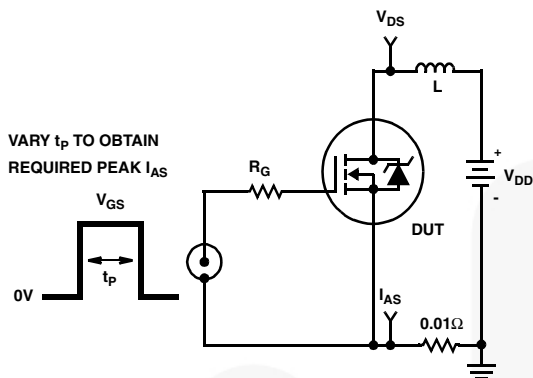


Figure 15. Unclamped Energy Test Circuit

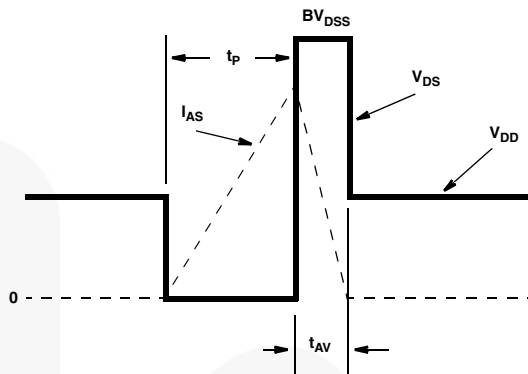


Figure 16. Unclamped Energy Waveforms

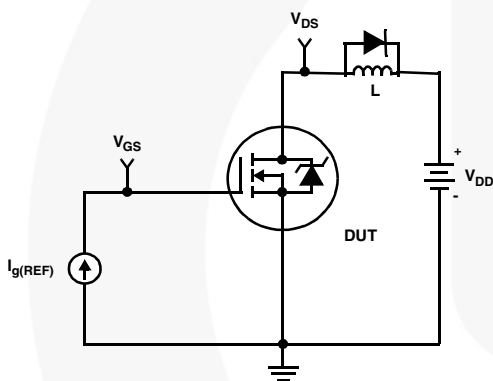


Figure 17. Gate Charge Test Circuit

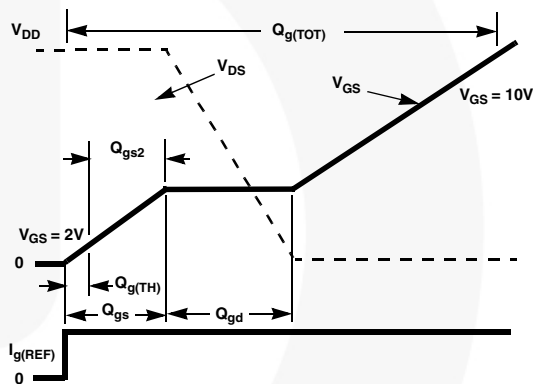


Figure 18. Gate Charge Waveforms

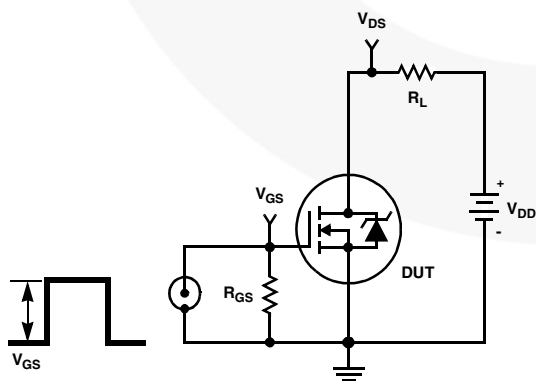


Figure 19. Switching Time Test Circuit

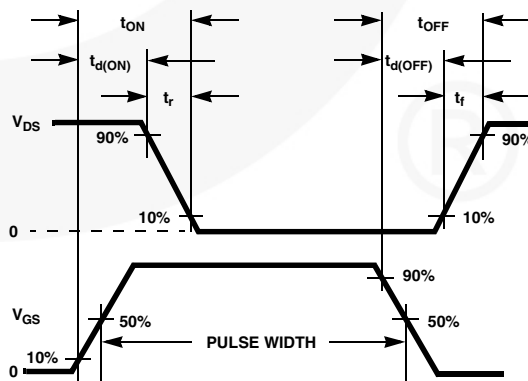


Figure 20. Switching Time Waveforms

### Thermal Resistance vs. Mounting Pad Area

The maximum rated junction temperature,  $T_{JM}$ , and the thermal resistance of the heat dissipating path determines the maximum allowable device power dissipation,  $P_{DM}$ , in an application. Therefore the application's ambient temperature,  $T_A$  ( $^{\circ}C$ ), and thermal resistance  $R_{\theta JA}$  ( $^{\circ}C/W$ ) must be reviewed to ensure that  $T_{JM}$  is never exceeded. Equation 1 mathematically represents the relationship and serves as the basis for establishing the rating of the part.

$$P_{DM} = \frac{(T_{JM} - T_A)}{R_{\theta JA}} \quad (\text{EQ. 1})$$

In using surface mount devices such as the TO-263 package, the environment in which it is applied will have a significant influence on the part's current and maximum power dissipation ratings. Precise determination of  $P_{DM}$  is complex and influenced by many factors:

1. Mounting pad area onto which the device is attached and whether there is copper on one side or both sides of the board.
2. The number of copper layers and the thickness of the board.
3. The use of external heat sinks.
4. The use of thermal vias.
5. Air flow and board orientation.
6. For non steady state applications, the pulse width, the duty cycle and the transient thermal response of the part, the board and the environment they are in.

Fairchild provides thermal information to assist the designer's preliminary application evaluation. Figure 21 defines the  $R_{\theta JA}$  for the device as a function of the top copper (component side) area. This is for a horizontally positioned FR-4 board with 1oz copper after 1000 seconds of steady state power with no air flow. This graph provides the necessary information for calculation of the steady state junction temperature or power dissipation. Pulse applications can be evaluated using the Fairchild device Spice thermal model or manually utilizing the normalized maximum transient thermal impedance curve.

Thermal resistances corresponding to other copper areas can be obtained from Figure 21 or by calculation using Equation 2 or 3. Equation 2 is used for copper area defined in inches square and equation 3 is for area in centimeter square. The area, in square inches or square centimeters is the top copper area including the gate and source pads.

$$R_{\theta JA} = 26.51 + \frac{19.84}{(0.262 + Area)} \quad (\text{EQ. 2})$$

Area in Inches Squared

$$R_{\theta JA} = 26.51 + \frac{128}{(1.69 + Area)} \quad (\text{EQ. 3})$$

Area in Centimeter Squared

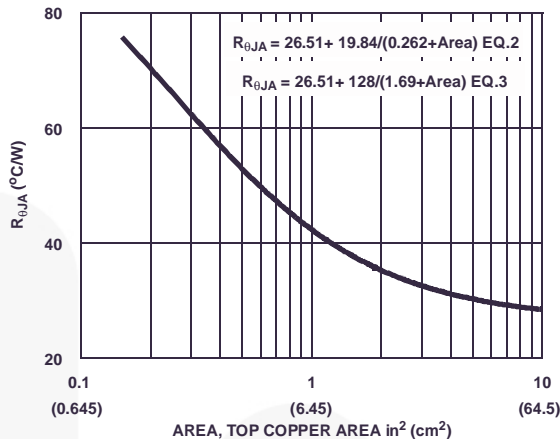


Figure 21. Thermal Resistance vs Mounting Pad Area





### SABER Electrical Model

REV May 2002  
 template FDB3632 n2,n1,n3  
 electrical n2,n1,n3

```

{
var i iscl
dp..model dbodymod = (isl=5.9e-11,ni=1.07,rs=2.3e-3,trs1=3.0e-3,trs2=1.0e-6,cjo=4e-9,m=0.58,tt=4.8e-8,xti=4.2)
dp..model dbreakmod = (rs=0.17,trs1=3.0e-3,trs2=-8.9e-6)
dp..model dplcapmod = (cjo=15e-10,isl=10.0e-30,ni=10,m=0.6)
m..model mstrongmod = (type=_n,vto=4.1,kp=200,is=1e-30,tox=1)
m..model mmedmod = (type=_n,vto=3.4,kp=10.0,is=1e-30,tox=1)
m..model mweakmod = (type=_n,vto=2.75,kp=0.05,is=1e-30,tox=1,rs=0.1)
sw_vcsp..model s1amod = (ron=1e-5,roff=0.1,von=-4,voff=-2)
sw_vcsp..model s1bmod = (ron=1e-5,roff=0.1,von=-2,voff=-4)
sw_vcsp..model s2amod = (ron=1e-5,roff=0.1,von=-0.8,voff=0.4)
sw_vcsp..model s2bmod = (ron=1e-5,roff=0.1,von=0.4,voff=-0.8)
c.ca n12 n8 = 1.7e-9
c.cb n15 n14 = 2.5e-9
c.cin n6 n8 = 6.0e-9
    
```

```

dp.dbody n7 n5 = model=dbodymod
dp.dbreak n5 n11 = model=dbreakmod
dp.dplcap n10 n5 = model=dplcapmod
    
```

```

spe.ebreak n11 n7 n17 n18 = 102.5
spe.eds n14 n8 n5 n8 = 1
spe.egs n13 n8 n6 n8 = 1
spe.esg n6 n10 n6 n8 = 1
spe.evthres n6 n21 n19 n8 = 1
spe.evtemp n20 n6 n18 n22 = 1
    
```

```

i.it n8 n17 = 1
    
```

```

l.lgate n1 n9 = 5.61e-9
l.ldrain n2 n5 = 1.0e-9
l.lsource n3 n7 = 2.7e-9
    
```

```

res.rlgate n1 n9 = 56.1
res.rldrain n2 n5 = 10
res.rlsource n3 n7 = 27
    
```

```

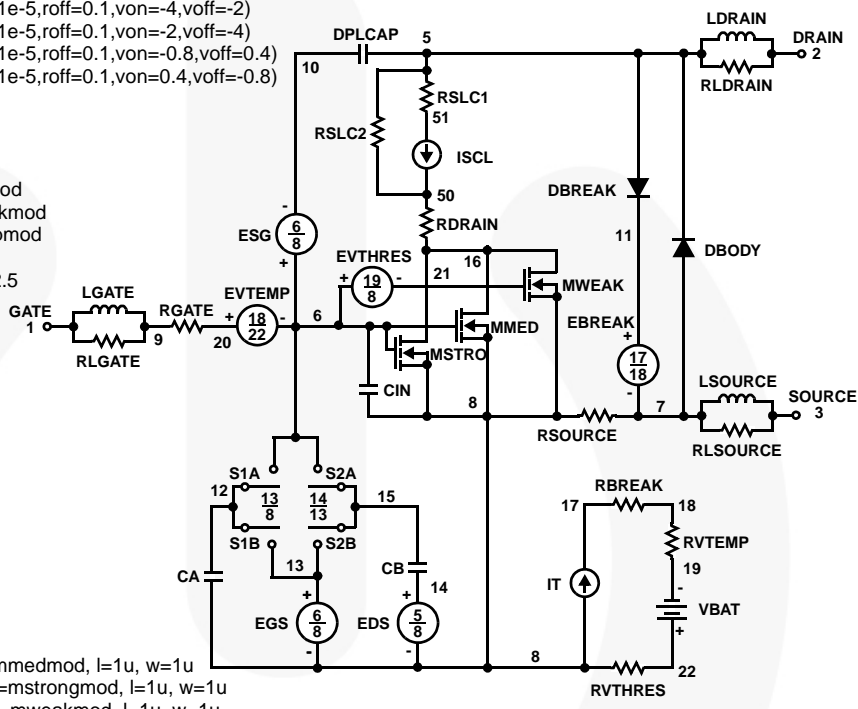
m.mmed n16 n6 n8 n8 = model=mmedmod, l=1u, w=1u
m.mstrong n16 n6 n8 n8 = model=mstrongmod, l=1u, w=1u
m.mweak n16 n21 n8 n8 = model=mweakmod, l=1u, w=1u
    
```

```

res.rbreak n17 n18 = 1, tc1=1.0e-3,tc2=-1.7e-6
res.rdrain n5 n16 = 3.8e-3, tc1=8.5e-3,tc2=2.8e-5
res.rgate n9 n20 = 1.1
res.rslc1 n5 n51 = 1.0e-6, tc1=2.0e-3,tc2=2.0e-6
res.rslc2 n5 n50 = 1.0e3
res.rsource n8 n7 = 2.5e-3, tc1=4e-3,tc2=1e-6
res.rvthres n22 n8 = 1, tc1=-4.0e-3,tc2=-1.8e-5
res.rvtemp n18 n19 = 1, tc1=-4.4e-3,tc2=2.2e-6
sw_vcsp.s1a n6 n12 n13 n8 = model=s1amod
sw_vcsp.s1b n13 n12 n13 n8 = model=s1bmod
sw_vcsp.s2a n6 n15 n14 n13 = model=s2amod
sw_vcsp.s2b n13 n15 n14 n13 = model=s2bmod
    
```

```

v.vbat n22 n19 = dc=1
equations {
i (n51->n50) +=iscl
iscl: v(n51,n50) = ((v(n5,n51))/(1e-9+abs(v(n5,n51))))*((abs(v(n5,n51))*1e6/350)** 3))
}
}
    
```



### SPICE Thermal Model

REV May 2002

FDB3632

```

CTHERM1 TH 6 7.5e-3
CTHERM2 6 5 8.0e-3
CTHERM3 5 4 9.0e-3
CTHERM4 4 3 2.4e-2
CTHERM5 3 2 3.4e-2
CTHERM6 2 TL 6.5e-2
    
```

```

RTHERM1 TH 6 3.1e-4
RTHERM2 6 5 2.5e-3
RTHERM3 5 4 2.2e-2
RTHERM4 4 3 8.1e-2
RTHERM5 3 2 1.35e-1
RTHERM6 2 TL 1.5e-1
    
```

### SABER Thermal Model

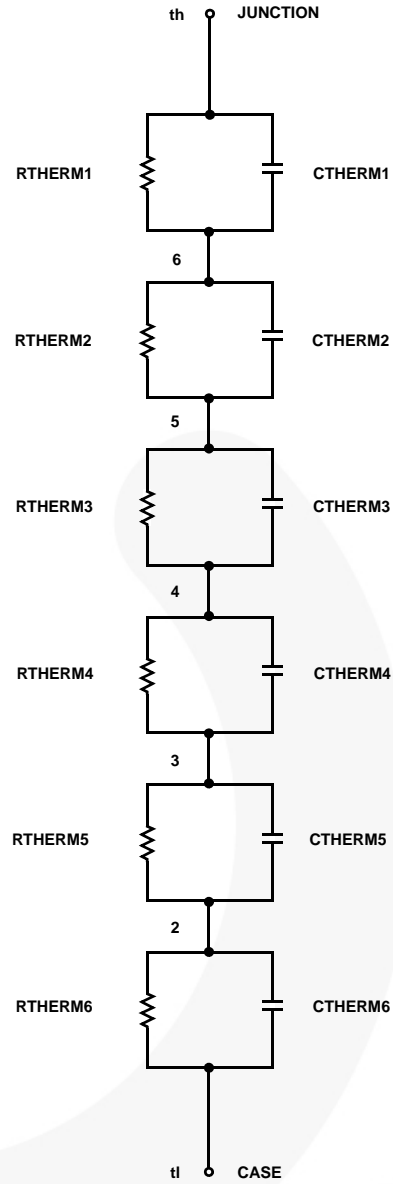
SABER thermal model FDB3632  
 template thermal\_model th tl  
 thermal\_c th, tl

```

{
ctherm.ctherm1 th 6 =7.5e-3
ctherm.ctherm2 6 5 =8.0e-3
ctherm.ctherm3 5 4 =9.0e-3
ctherm.ctherm4 4 3 =2.4e-2
ctherm.ctherm5 3 2 =3.4e-2
ctherm.ctherm6 2 tl =6.5e-2
    
```

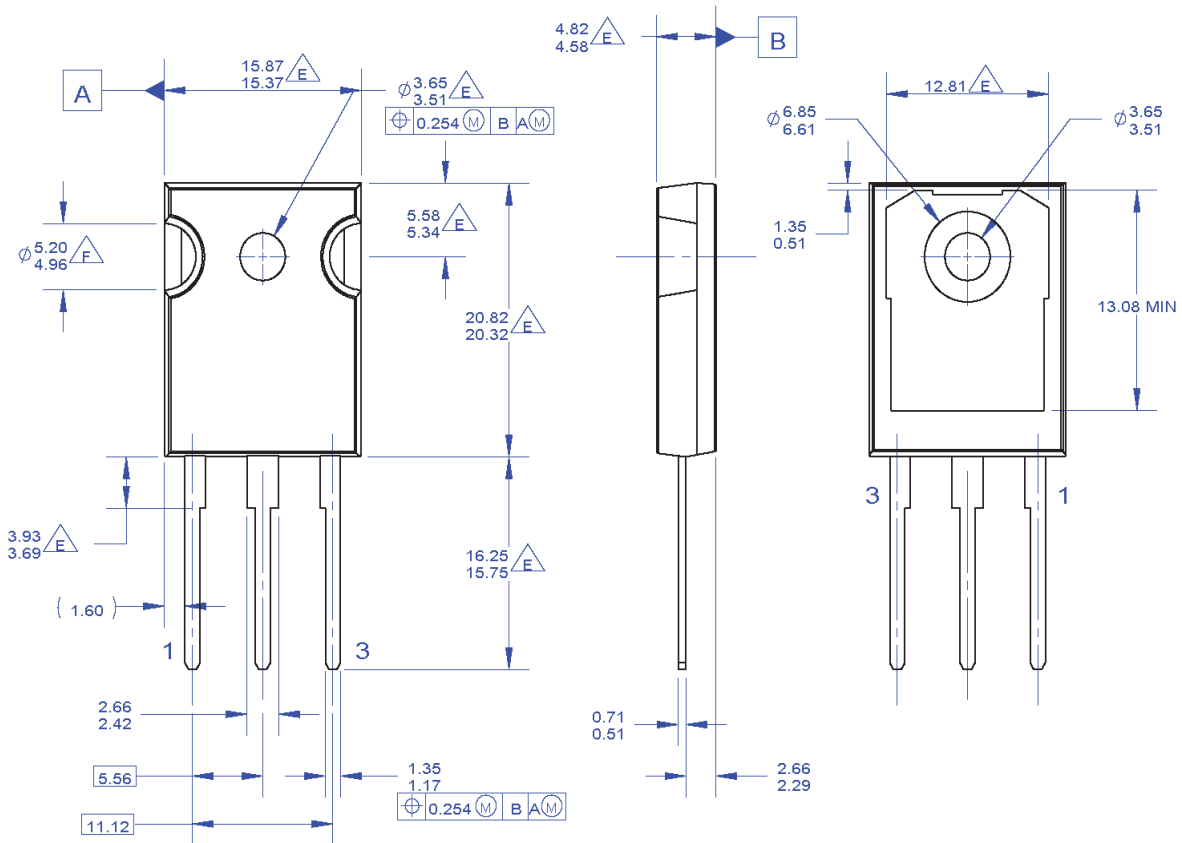
```

rtherm.rtherm1 th 6 =3.1e-4
rtherm.rtherm2 6 5 =2.5e-3
rtherm.rtherm3 5 4 =2.2e-2
rtherm.rtherm4 4 3 =8.1e-2
rtherm.rtherm5 3 2 =1.35e-1
rtherm.rtherm6 2 tl =1.5e-1
}
    
```



## Mechanical Dimensions

### TO-247 3L



NOTES: UNLESS OTHERWISE SPECIFIED.

- A. PACKAGE REFERENCE: JEDEC TO-247, ISSUE E, VARIATION AB, DATED JUNE, 2004.
- B. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- C. ALL DIMENSIONS ARE IN MILLIMETERS.
- D. DRAWING CONFORMS TO ASME Y14.5 - 1994

$\triangle E$  DOES NOT COMPLY JEDEC STANDARD VALUE

$\triangle F$  NOTCH MAY BE SQUARE

G. DRAWING FILENAME: MKT-TO247A03\_REV03

**Figure 22. TO-247, Molded, 3 Lead, Jeced Variation AB**

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

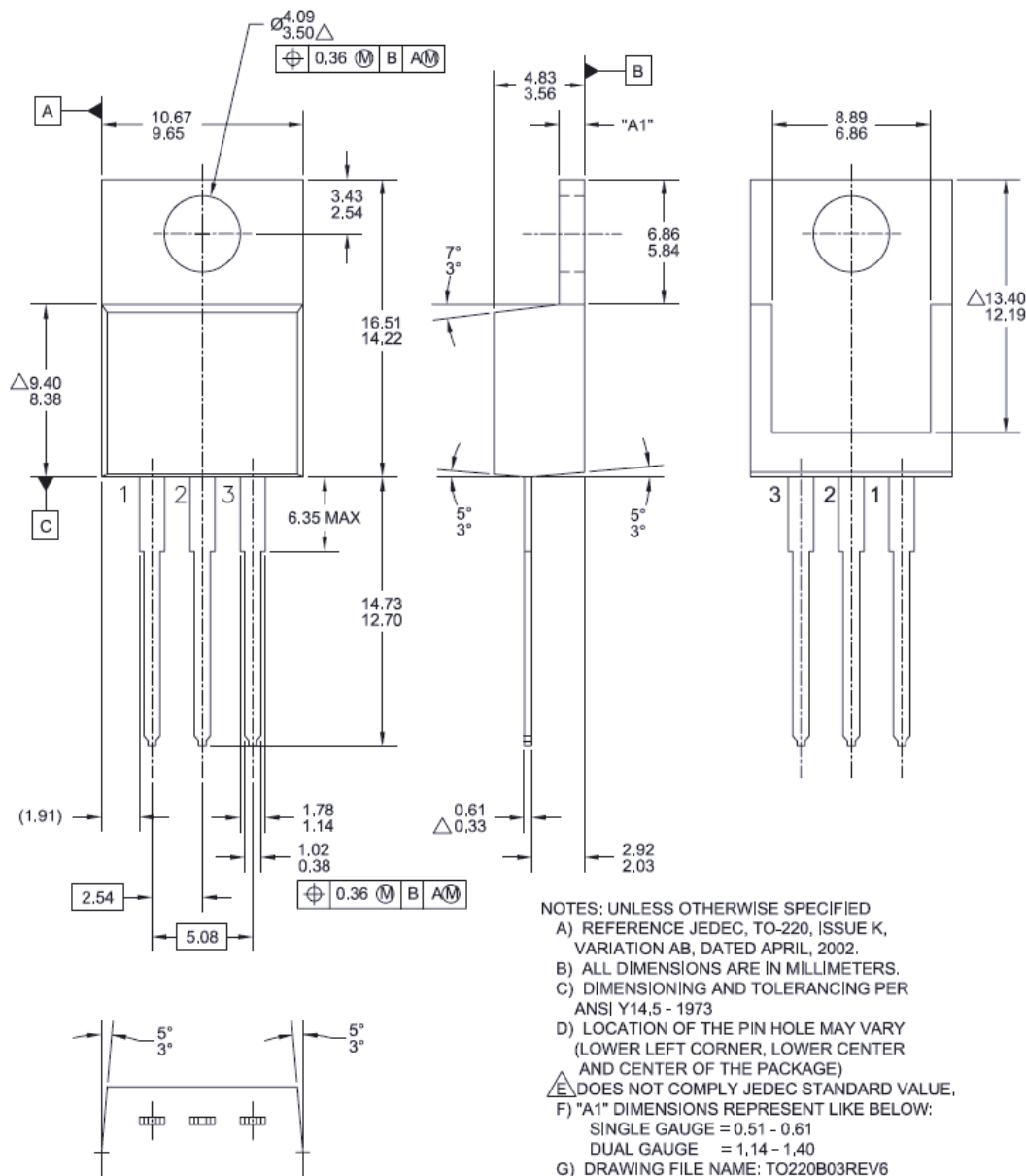
Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:

[http://www.fairchildsemi.com/package/packageDetails.html?id=PN\\_TO247-003](http://www.fairchildsemi.com/package/packageDetails.html?id=PN_TO247-003)

Dimension in Millimeters

## Mechanical Dimensions

### TO-220 3L



**Figure 23. TO-220, Molded, 3Lead, Jedec Variation AB**

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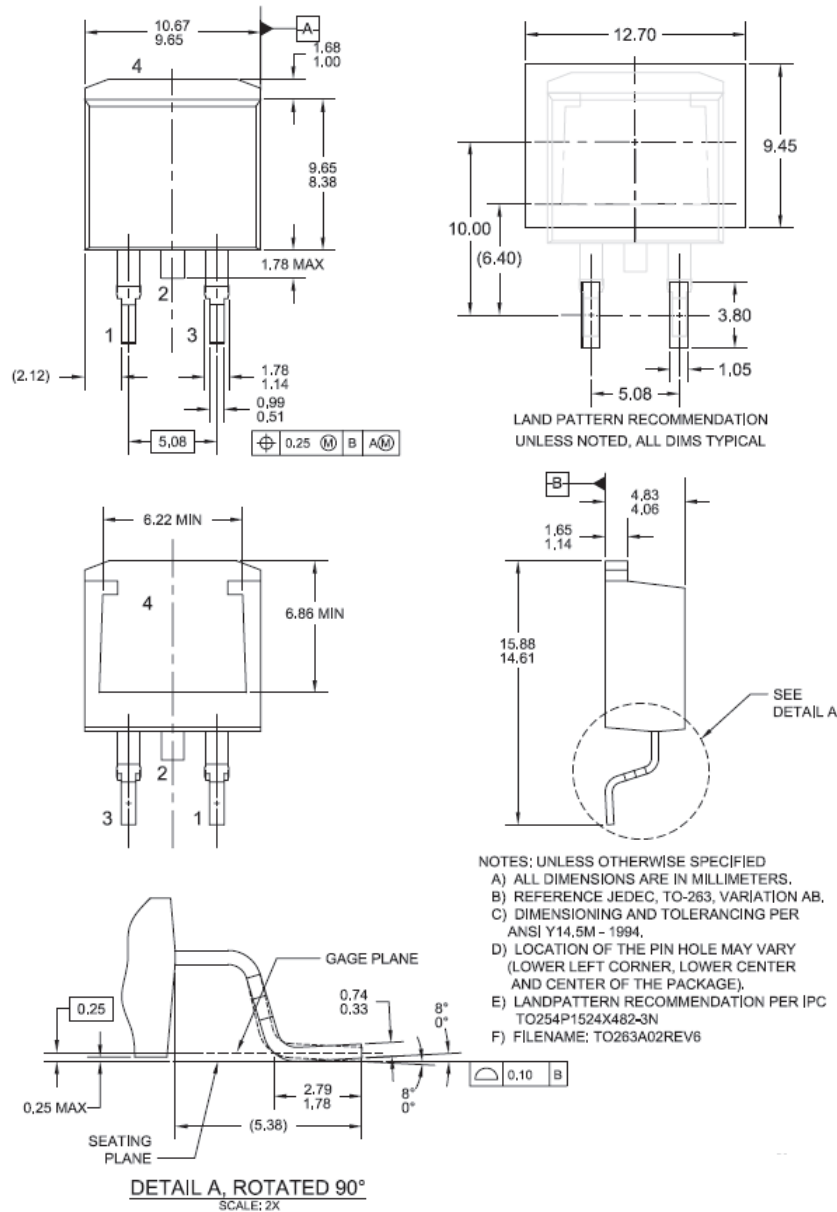
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[http://www.fairchildsemi.com/package/packageDetails.html?id=PN\\_TT220-003](http://www.fairchildsemi.com/package/packageDetails.html?id=PN_TT220-003)

Dimension in Millimeters

## Mechanical Dimensions

### TO-263 2L (D<sup>2</sup>PAK)



**Figure 24. 2LD, TO263, Surface Mount**

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Dimension in Millimeters



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