



# FDS9958\_F085

## Dual P-Channel PowerTrench<sup>®</sup> MOSFET -60V, -2.9A, 105mΩ

### Features

- Max  $r_{DS(on)}$  = 105mΩ at  $V_{GS} = -10V, I_D = -2.9A$
- Max  $r_{DS(on)}$  = 135mΩ at  $V_{GS} = -4.5V, I_D = -2.5A$
- Qualified to AEC Q101
- RoHS Compliant



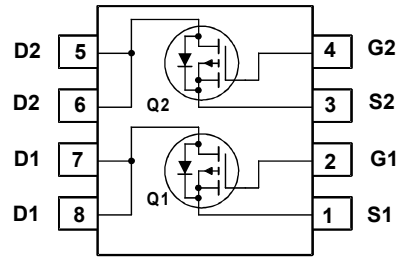
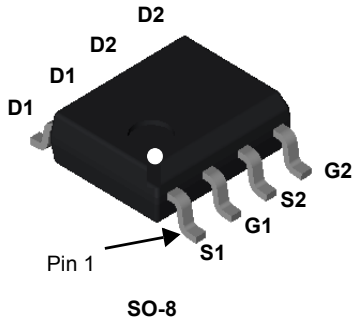
### General Description

These P-channel logic level specified MOSFETs are produced using Fairchild Semiconductor's advanced PowerTrench<sup>®</sup> process that has been especially tailored to minimize the on-state resistance and yet maintain low gate charge for superior switching performance.

These devices are well suited for portable electronics applications: load switching and power management, battery charging and protection circuits.

### Applications

- Load Switch
- Power Management



### MOSFET Maximum Ratings $T_A = 25^\circ C$ unless otherwise noted

| Symbol         | Parameter  | Ratings     | Units      |
|----------------|--|-------------|------------|
| $V_{DS}$       | Drain to Source Voltage                          | -60         | V          |
| $V_{GS}$       | Gate to Source Voltage                           | $\pm 20$    | V          |
| $I_D$          | Drain Current -Continuous (Note 1a)              | -2.9        | A          |
|                | -Pulsed  | -12         |            |
| $E_{AS}$       | Single Pulse Avalanche Energy (Note 3)           | 54          | mJ         |
| $P_D$          | Power Dissipation for Dual Operation             | 2           | W          |
|                | Power Dissipation (Note 1a)                      | 1.6         |            |
|                | Power Dissipation (Note 1b)                      | 0.9         |            |
| $T_J, T_{STG}$ | Operating and Storage Junction Temperature Range | -55 to +150 | $^\circ C$ |

### Thermal Characteristics

|                 |   |    |              |
|-----------------|---|----|--------------|
| $R_{\theta JC}$ | Thermal Resistance, Junction to Case              | 40 | $^\circ C/W$ |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient (Note 1a) | 78 |              |

### Package Marking and Ordering Information

| Device Marking | Device       | Package | Reel Size | Tape Width | Quantity  |
|----------------|--------------|---------|-----------|------------|-----------|
| FDS9958        | FDS9958_F085 | SO-8    | 330mm     | 12mm       | 2500units |

FDS9958\_F085 Dual P-Channel PowerTrench<sup>®</sup> MOSFET

## Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|--------|-----------|-----------------|-----|-----|-----|-------|
|--------|-----------|-----------------|-----|-----|-----|-------|

### Off Characteristics

|                                      |   |   |     |     |           |                      |
|--------------------------------------|---|---|-----|-----|-----------|----------------------|
| $BV_{DSS}$                           | Drain to Source Breakdown Voltage         | $I_D = -250\mu\text{A}, V_{GS} = 0\text{V}$                         | -60 |     |           | V                    |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D = -250\mu\text{A}$ , referenced to $25^\circ\text{C}$          |     | -52 |           | mV/ $^\circ\text{C}$ |
| $I_{DSS}$                            | Zero Gate Voltage Drain Current           | $V_{DS} = -48\text{V}, V_{GS} = 0\text{V}, T_J = 125^\circ\text{C}$ |     |     | -1        | $\mu\text{A}$        |
| $I_{GSS}$                            | Gate to Source Leakage Current            | $V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$                       |     |     | $\pm 100$ | nA                   |

### On Characteristics

|  |  |   |      |      |      |                      |
|--|--|---|------|------|------|----------------------|
| $V_{GS(th)}$                           | Gate to Source Threshold Voltage                         | $V_{GS} = V_{DS}, I_D = -250\mu\text{A}$                            | -1.0 | -1.6 | -3.0 | V                    |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate to Source Threshold Voltage Temperature Coefficient | $I_D = -250\mu\text{A}$ , referenced to $25^\circ\text{C}$          |      | 4    |      | mV/ $^\circ\text{C}$ |
| $r_{DS(on)}$                           | Static Drain to Source On Resistance                     | $V_{GS} = -10\text{V}, I_D = -2.9\text{A}$                          |      | 82   | 105  | m $\Omega$           |
|  |  | $V_{GS} = -4.5\text{V}, I_D = -2.5\text{A}$                         |      | 103  | 135  |                      |
|  |  | $V_{GS} = -10\text{V}, I_D = -2.9\text{A}, T_J = 125^\circ\text{C}$ |      | 131  | 190  |                      |
| $g_{FS}$                               | Forward Transconductance                                 | $V_{DD} = -5\text{V}, I_D = -2.9\text{A}$                           |      | 7.7  |      | S                    |

### Dynamic Characteristics

|           |                              |   |  |     |      |    |
|-----------|------------------------------|---|--|-----|------|----|
| $C_{iss}$ | Input Capacitance            | $V_{DS} = -30\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$ |  | 765 | 1020 | pF |
| $C_{oss}$ | Output Capacitance           |   |  | 90  | 120  | pF |
| $C_{rss}$ | Reverse Transfer Capacitance |   |  | 40  | 65   | pF |

### Switching Characteristics

|              |                               |   |  |    |    |    |
|--------------|-------------------------------|---|--|----|----|----|
| $t_{d(on)}$  | Turn-On Delay Time            | $V_{DD} = -30\text{V}, I_D = -2.9\text{A}, V_{GS} = -10\text{V}, R_{GEN} = 6\Omega$ |  | 6  | 12 | ns |
| $t_r$        | Rise Time                     |   |  | 3  | 10 | ns |
| $t_{d(off)}$ | Turn-Off Delay Time           |   |  | 27 | 43 | ns |
| $t_f$        | Fall Time                     |   |  | 6  | 12 | ns |
| $Q_g$        | Total Gate Charge             |   | $V_{GS} = 0\text{V to } -10\text{V}$       |    | 16 | 23 |
| $Q_g$        | Total Gate Charge             | $V_{GS} = 0\text{V to } -4.5\text{V}$   | $V_{DD} = -30\text{V}, I_D = -2.9\text{A}$ | 8  | 12 | nC |
| $Q_{gs}$     | Gate to Source Charge         |   |  | 2  |    | nC |
| $Q_{gd}$     | Gate to Drain "Miller" Charge |   |  | 3  |    | nC |

### Drain-Source Diode Characteristics

|          |                                       |   |  |      |      |    |
|----------|---------------------------------------|---|--|------|------|----|
| $V_{SD}$ | Source to Drain Diode Forward Voltage | $V_{GS} = 0\text{V}, I_S = -1.3\text{A}$ (Note 2)     |  | -0.8 | -1.2 | V  |
| $t_{rr}$ | Reverse Recovery Time                 | $I_F = -2.9\text{A}, di/dt = 100\text{A}/\mu\text{s}$ |  | 26   | 42   | ns |
| $Q_{rr}$ | Reverse Recovery Charge               |   |  | 21   | 35   | nC |

#### NOTES:

- $R_{\theta JA}$  is determined with the device mounted on a  $1\text{in}^2$  pad 2 oz copper pad on a  $1.5 \times 1.5\text{in.}$  board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a)  $78^\circ\text{C/W}$  when mounted on a  $1\text{in}^2$  pad of 2 oz copper

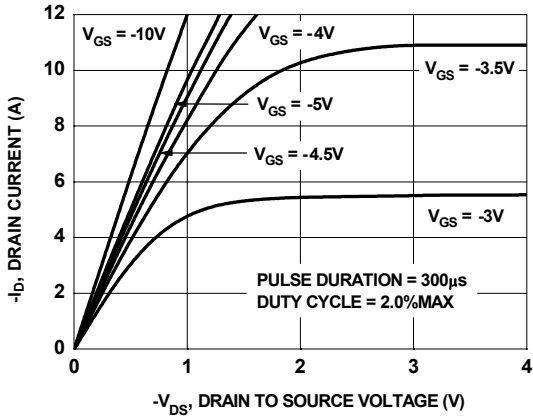


b)  $135^\circ\text{C/W}$  when mounted on a minimum pad

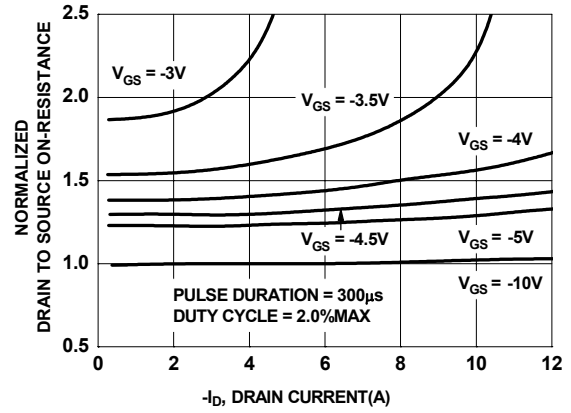
- Pulse Test: Pulse Width  $< 300\mu\text{s}$ , Duty cycle  $< 2.0\%$ .

- UIL condition: Starting  $T_J = 25^\circ\text{C}$ ,  $L = 3\text{mH}$ ,  $I_{AS} = 6\text{A}$ ,  $V_{DD} = 60\text{V}$ ,  $V_{GS} = 10\text{V}$ .

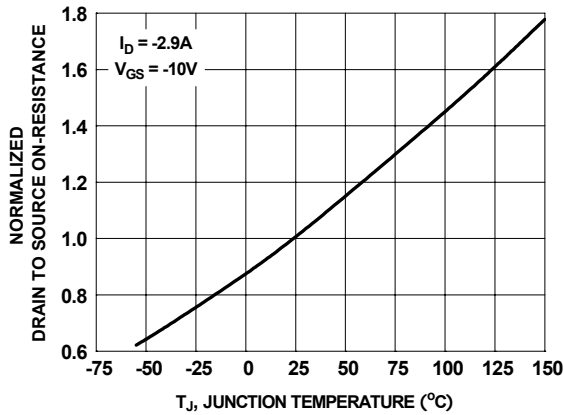
**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted



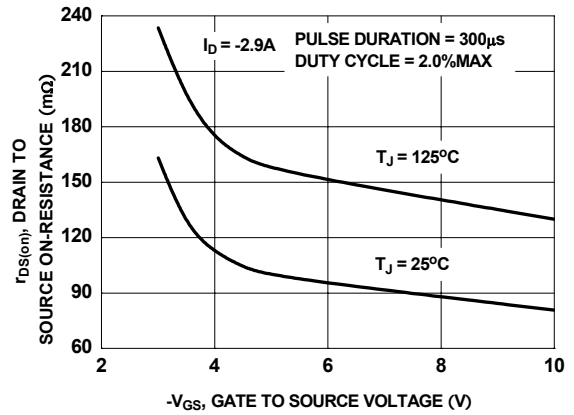
**Figure 1. On-Region Characteristics**



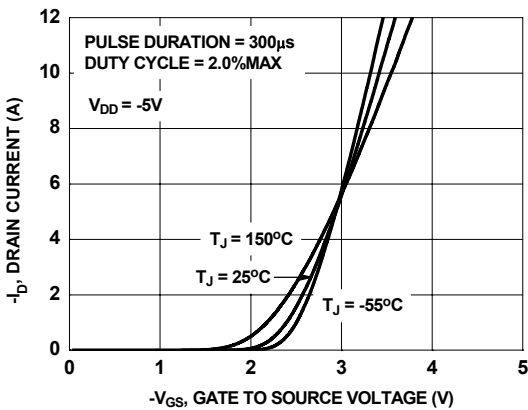
**Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage**



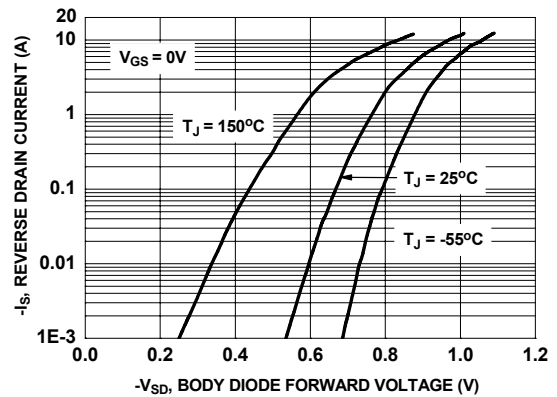
**Figure 3. Normalized On-Resistance vs Junction Temperature**



**Figure 4. On-Resistance vs Gate to Source Voltage**

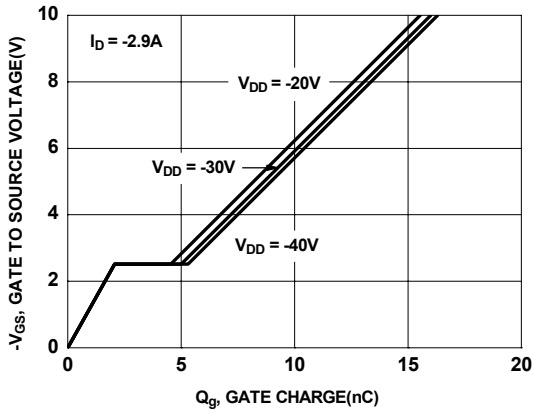


**Figure 5. Transfer Characteristics**

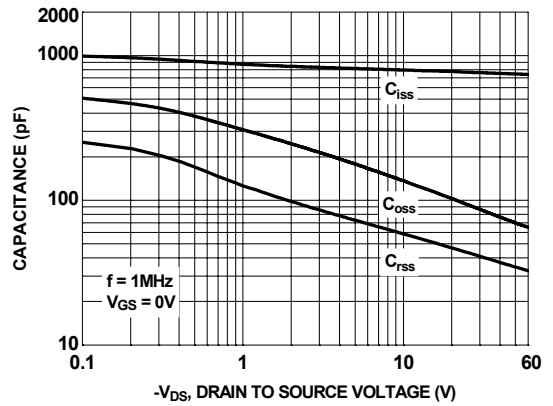


**Figure 6. Source to Drain Diode Forward Voltage vs Source Current**

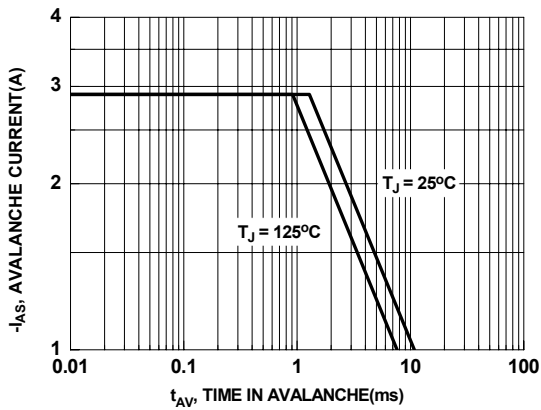
**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted



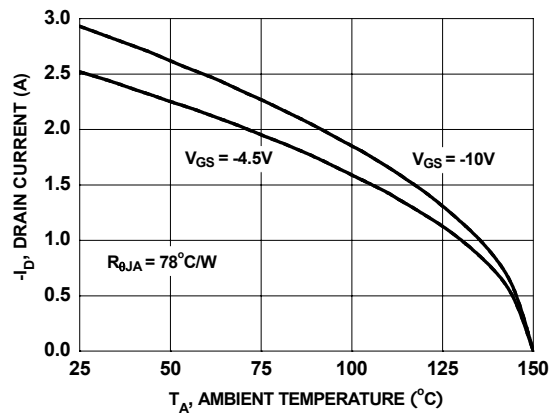
**Figure 7. Gate Charge Characteristics**



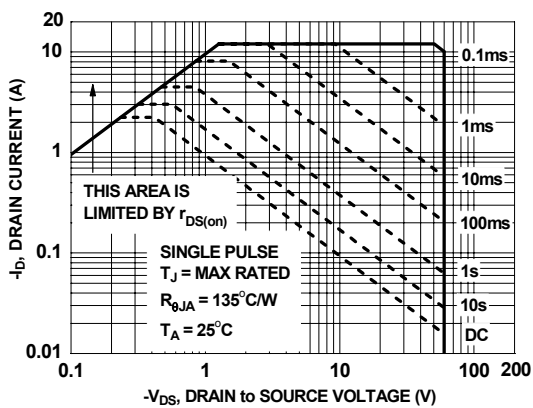
**Figure 8. Capacitance vs Drain to Source Voltage**



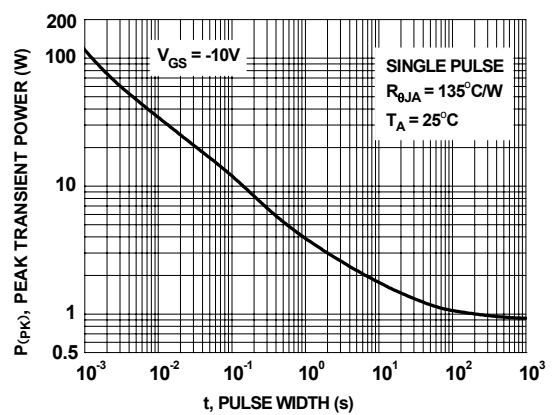
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Maximum Continuous Drain Current vs Ambient Temperature**

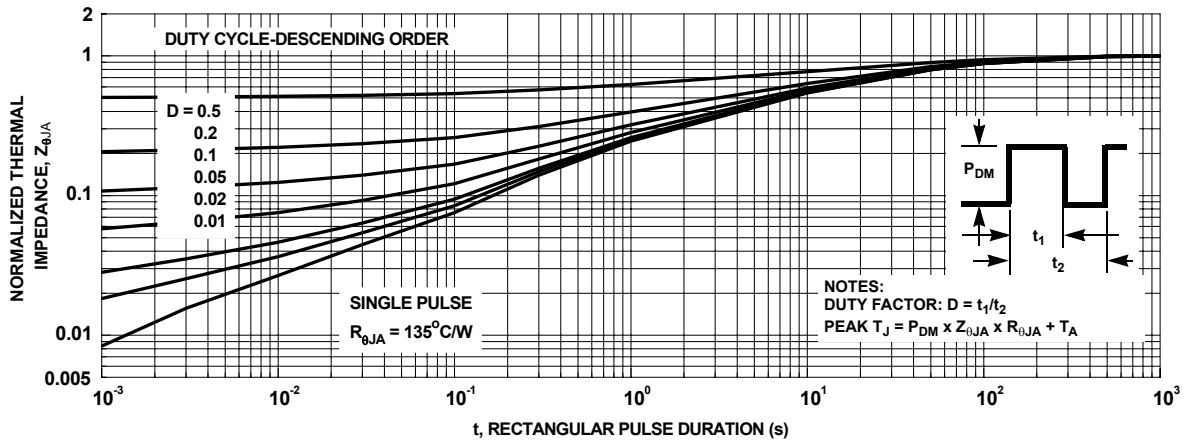


**Figure 11. Forward Bias Safe Operating Area**

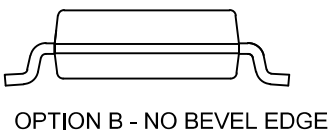
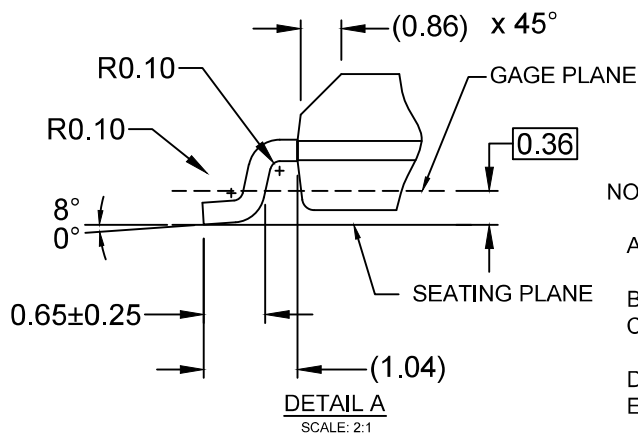
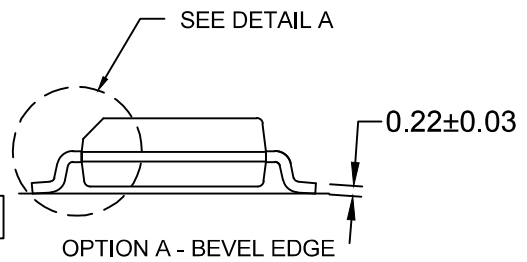
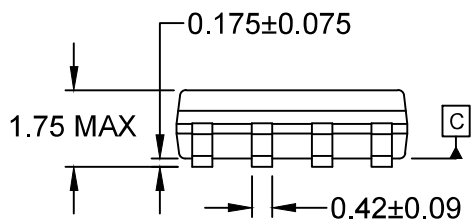
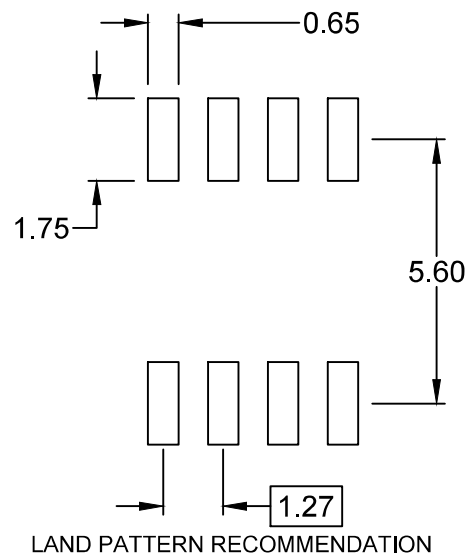
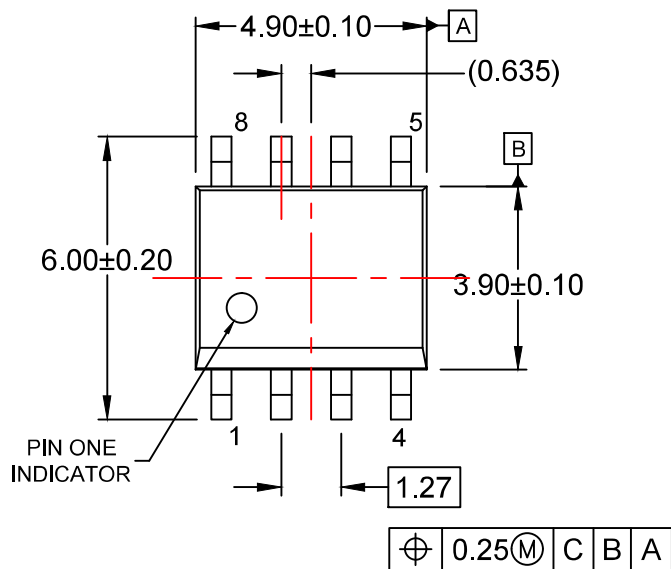


**Figure 12. Single Pulse Maximum Power Dissipation**

**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted



**Figure 13. Transient Thermal Response Curve**



NOTES:

- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
- D) LANDPATTERN STANDARD: SOIC127P600X175-8M
- E) DRAWING FILENAME: M08Arev16





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