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June 2013

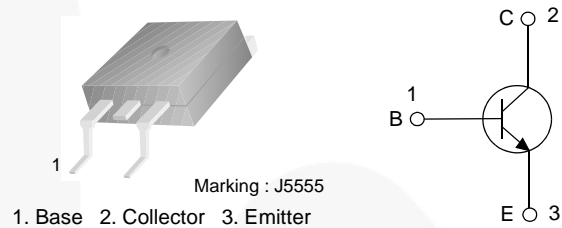
# FJD5555 NPN Silicon Transistor

## Features

- Fast Speed Switching
- Wide Safe Operating Area
- High Voltage Capability

## Application

- Electronic Ballast
- Switch Mode Power Supplies



## Ordering Information

Part Number	Marking	Package	Packing Method
FJD5555TM	J5555	D-PAK	Tape & Reel

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Values are at  $T_A = 25^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter	Value	Units
$BV_{CBO}$	Collector-Base Voltage	1050	V
$BV_{CEO}$	Collector-Emitter Voltage	400	V
$BV_{EBO}$	Emitter-Base Voltage	14	V
$I_C$	Collector Current (DC)	5	A
$I_{CP}$	Collector Current (Pulse)	10	A
$I_B$	Base Current (DC)	2	A
$I_{BP}$	Base Current (Pulse)	4	A
$T_J$	Junction Temperature	150	$^\circ\text{C}$
$T_{STG}$	Storage Junction Temperature Range	- 55 to +150	$^\circ\text{C}$

## Thermal Characteristics

Values are at  $T_A = 25^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter	Value	Units	
$P_D$	Total Device Dissipation	$T_A = 25^\circ\text{C}$	1.34	W
		$T_C = 25^\circ\text{C}$	100	W
$R_{\theta ja}^{(1)}$	Thermal Resistance, Junction to Ambient	95	$^\circ\text{C}/\text{W}$	
$R_{\theta jc}^{(2)}$	Thermal Resistance, Junction to Case	1.25	$^\circ\text{C}/\text{W}$	

### Notes:

1.  $R_{\theta ja}$  test board and fixture under natural convection; JESD51-3 recommended thermal test board.
2.  $R_{\theta jc}$  test fixture under infinite cooling condition.

**Electrical Characteristics<sup>(3)</sup>**Values are at  $T_A = 25^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$BV_{CBO}$	Collector-Base Breakdown Voltage	$I_C = 500 \mu\text{A}, I_E = 0$	1050			V
$BV_{CEO}$	Collector-Emitter Breakdown Voltage	$I_C = 5 \text{ mA}, I_B = 0$	400			V
$BV_{EBO}$	Emitter-Base Breakdown Voltage	$I_E = 500 \mu\text{A}, I_C = 0$	14			V
$h_{FE}$	DC Current Gain	$V_{CE} = 5 \text{ V}, I_C = 10 \text{ mA}$	10			
		$V_{CE} = 3 \text{ V}, I_C = 0.8 \text{ A}$	20		40	
$V_{CE}(\text{sat})$	Collector-Emitter Saturation Voltage	$I_C = 1 \text{ A}, I_B = 0.2 \text{ A}$		0.17	0.50	V
		$I_C = 3.5 \text{ A}, I_B = 1.0 \text{ A}$			1.5	V
$V_{BE}(\text{sat})$	Base-Emitter Saturation Voltage	$I_C = 3.5 \text{ A}, I_B = 1.0 \text{ A}$			1.2	V
$C_{ob}$	Output Capacitance	$V_{CB} = 10 \text{ V}, f = 1 \text{ MHz}$		45		pF
$t_{ON}$	Turn-On Time	$V_{CC} = 125 \text{ V}, I_C = 0.5 \text{ A},$ $I_{B1} = 45 \text{ mA}, I_{B2} = -0.5 \text{ A},$ $R_L = 250 \Omega$			1.0	$\mu\text{s}$
$t_{STG}$	Storage Time				1.2	$\mu\text{s}$
$t_F$	Fall Time			0.3		$\mu\text{s}$
$t_{ON}$	Turn-On Time	$V_{CC} = 250 \text{ V}, I_C = 2.5 \text{ A},$ $I_{B1} = 0.5 \text{ A}, I_{B2} = -1.0 \text{ A},$ $R_L = 100 \Omega$			2.0	$\mu\text{s}$
$t_{STG}$	Storage Time				2.5	$\mu\text{s}$
$t_F$	Fall Time				0.3	$\mu\text{s}$
EAS	Avalanche Energy	$L = 2 \text{ mH}$	6			mJ

**Note:**3. Pulse test: pulse width  $\leq 300 \mu\text{s}$ , duty cycle  $\leq 2\%$ .

## Typical Performance Characteristics

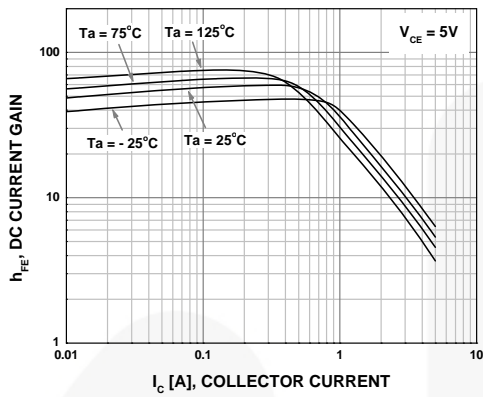


Figure 1. DC Current Gain

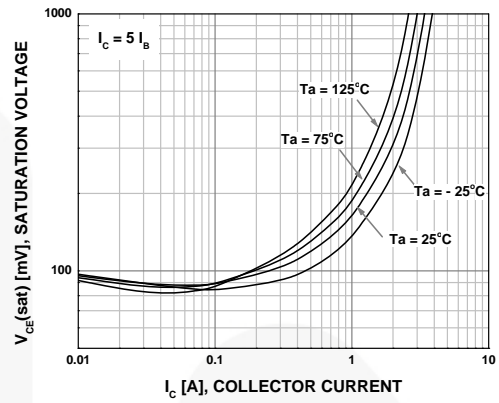


Figure 2. Saturation Voltage

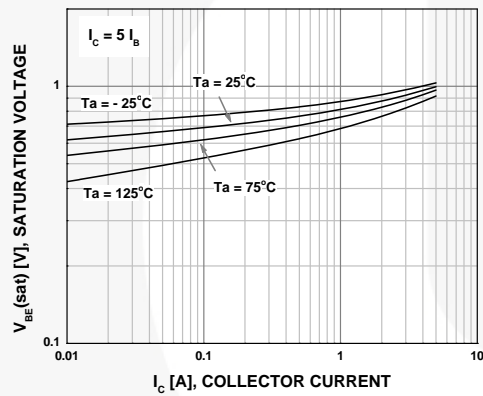


Figure 3. Saturation Voltage

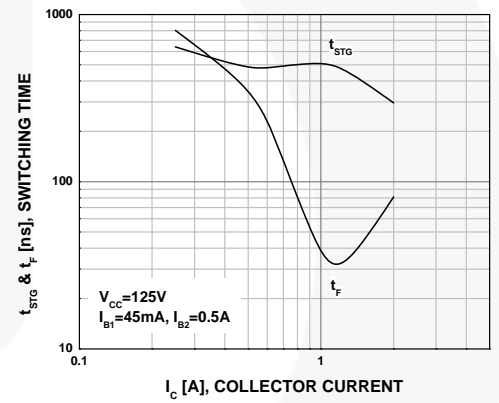


Figure 4. Resistive Load Switching

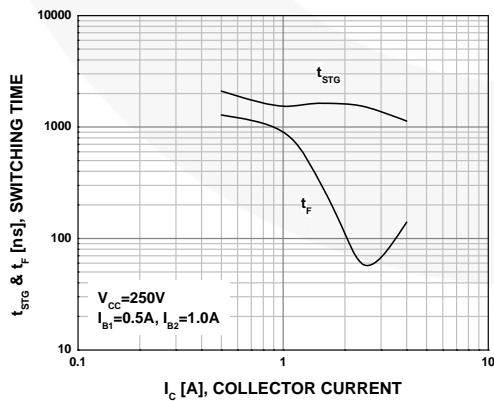


Figure 5. Resistive Load Switching

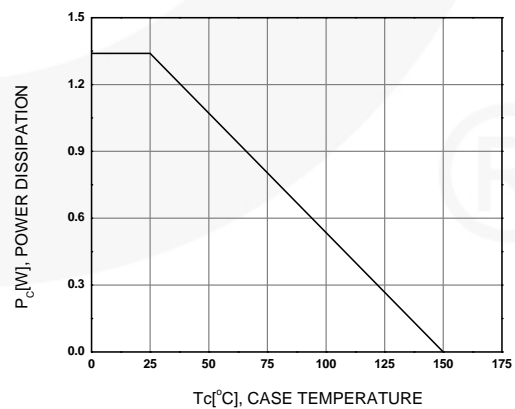


Figure 6. Power Derating

Typical Performance Characteristics (Continued)

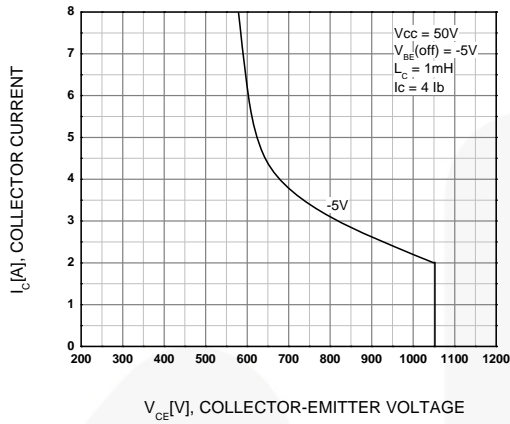


Figure 7. Reverse Bias Safe Operating

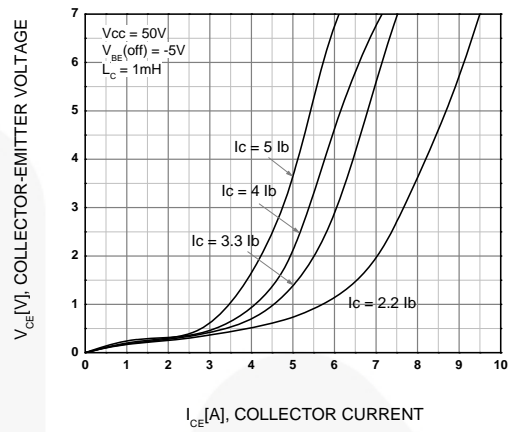
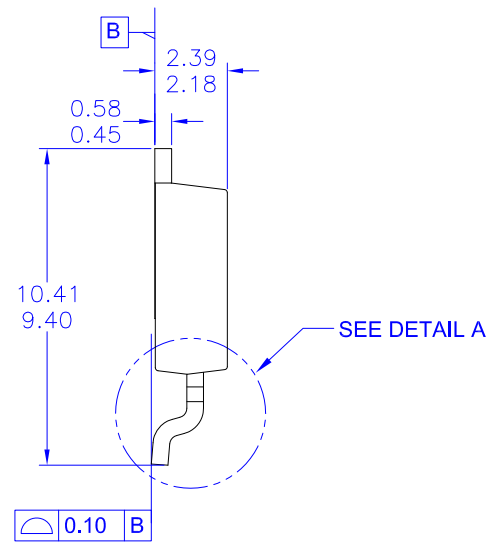
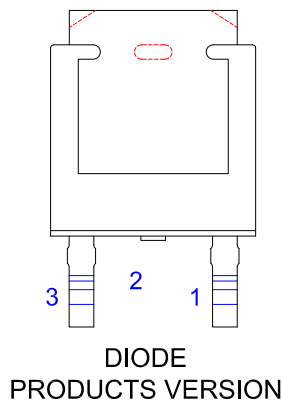
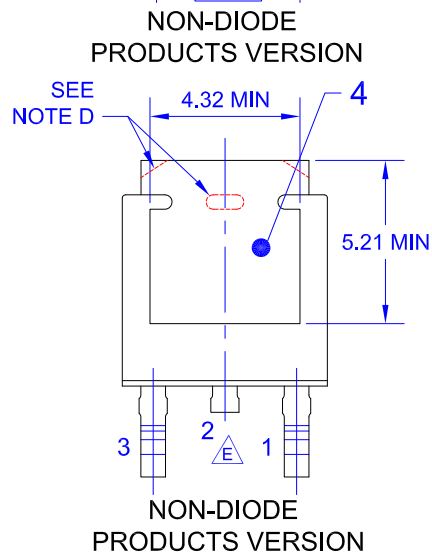
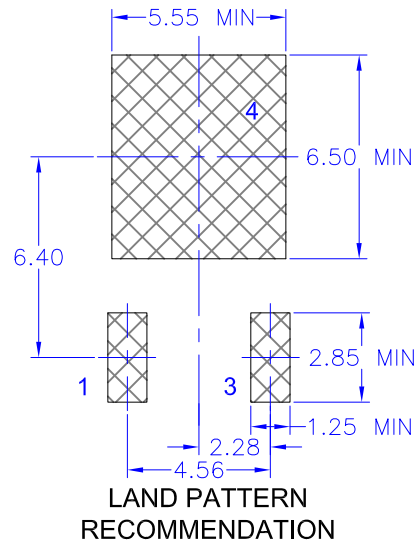
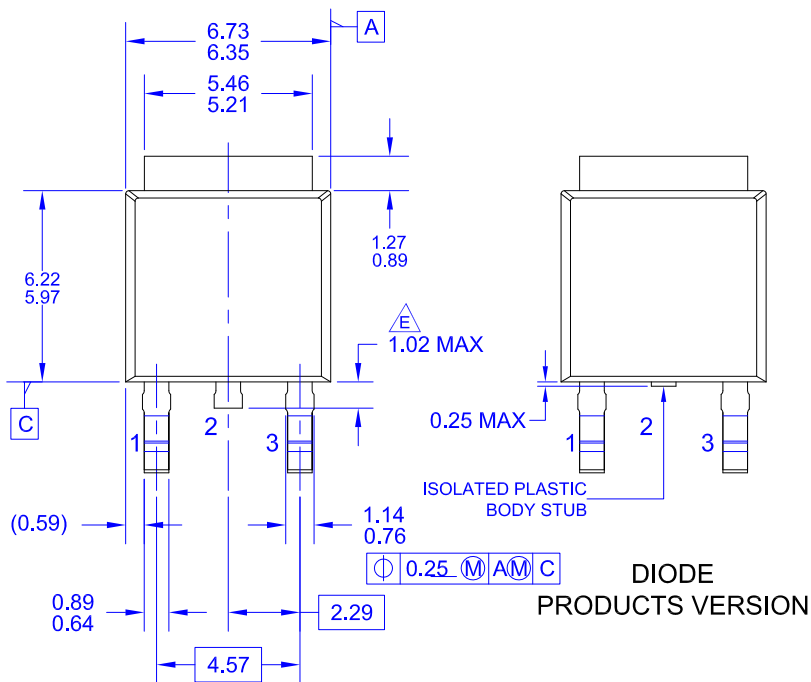
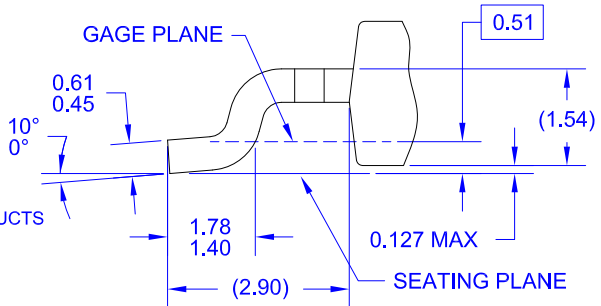


Figure 8.  $V_{CE}$  Saturation vs.  $h_{FE}$



**NOTES: UNLESS OTHERWISE SPECIFIED**

- A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
- D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
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- G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.
- H) DRAWING NUMBER AND REVISION: MKT-TO252A03REV11



**DETAIL A**  
(ROTATED -90°)  
SCALE: 12X





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