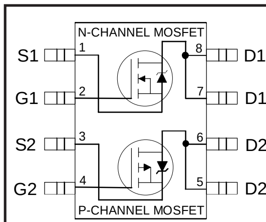
PD - 94372C

International
IOR Rectifier

IRF7338

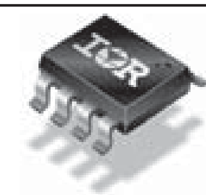
HEXFET® Power MOSFET

- Ultra Low On-Resistance
- Dual N and P Channel MOSFET
- Surface Mount
- Available in Tape & Reel



Top View

	N-Ch	P-Ch
V_{DSS}	12V	-12V
$R_{DS(on)}$	0.034Ω	0.150Ω



SO-8

Description

These N and P channel MOSFETs from International Rectifier utilize advanced processing techniques to achieve the extremely low on-resistance per silicon area. This benefit provides the designer with an extremely efficient device for use in battery and load management applications.

This Dual SO-8 has been modified through a customized leadframe for enhanced thermal characteristics and multiple-die capability making it ideal in a variety of power applications. With these improvements, multiple devices can be used in an application with dramatically reduced board space. The package is designed for vapor phase, infrared, or wave soldering techniques.

Absolute Maximum Ratings

	Parameter	Max. N-Channel	Max. P-Channel	Units
V_{DS}	Drain-to-Source Voltage	12	-12	
I_D @ T_A = 25°C	Continuous Drain Current, V_{GS} @ 4.5V	6.3	-3.0	A
I_D @ T_A = 70°C	Continuous Drain Current, V_{GS} @ 4.5V	5.2	-2.5	
I_{DM}	Pulsed Drain Current ①	26	-13	
P_D @T_A = 25°C	Power Dissipation ③	2.0		W
P_D @T_A = 70°C	Power Dissipation ③	1.3		
	Linear Derating Factor	16		mW/°C
V_{GS}	Gate-to-Source Voltage	±12 ④	± 8.0	V
T_J, T_{STG}	Junction and Storage Temperature Range	-55 to + 150		°C

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JL}$	Junction-to-Drain Lead	——	20	
$R_{\theta JA}$	Junction-to-Ambient ③	——	62.5	°C/W

6/2/03

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter		Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	N-Ch	12	—	—	V	V_{GS} = 0V, I_D = 250µA
		P-Ch	-12	—	—		V_{GS} = 0V, I_D = -250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	N-Ch	—	0.01	—	V/°C	Reference to 25°C, I_D = 1mA
		P-Ch	—	-0.01	—		Reference to 25°C, I_D = -1mA
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance	N-Ch	—	—	0.034	Ω	V_{GS} = 4.5V, I_D = 6.0A ②
			—	—	0.060		V_{GS} = 3.0V, I_D = 2.0A ②
		P-Ch	—	—	0.150		V_{GS} = -4.5V, I_D = -2.9A ②
			—	—	0.200		V_{GS} = -2.7V, I_D = -1.5A ②
$V_{GS(th)}$	Gate Threshold Voltage	N-Ch	0.6	—	1.5	V	V_{DS} = V_{GS}, I_D = 250µA
		P-Ch	-0.40	—	-1.0		V_{DS} = V_{GS}, I_D = -250µA
g_{fs}	Forward Transconductance	N-Ch	9.2	—	—	S	V_{DS} = 6.0V, I_D = 6.0A ②
		P-Ch	3.5	—	—		V_{DS} = -6.0V, I_D = -1.5A ②
I_{DSS}	Drain-to-Source Leakage Current	N-Ch	—	—	20	µA	V_{DS} = 9.6V, V_{GS} = 0V
		P-Ch	—	—	-1.0		V_{DS} = -9.6 V, V_{GS} = 0V
		N-Ch	—	—	50		V_{DS} = 9.6V, V_{GS} = 0V, T_J = 55°C
		P-Ch	—	—	-25		V_{DS} = -9.6V, V_{GS} = 0V, T_J = 55°C
I_{GSS}	Gate-to-Source Forward Leakage	N-Ch	—	—	±100	nA	V_{GS} = ± 12V
		P-Ch	—	—	±100		V_{GS} = ± 8.0V
Q_g	Total Gate Charge	N-Ch	—	—	8.6	nC	N-Channel I_D = 6.0A, V_{DS} = 6.0V, V_{GS} = 4.5V P-Channel I_D = -2.9A, V_{DS} = -9.6V, V_{GS} = -4.5 V
		P-Ch	—	—	6.6		
Q_{gs}	Gate-to-Source Charge	N-Ch	—	—	1.9		
		P-Ch	—	—	1.3		
Q_{gd}	Gate-to-Drain ("Miller") Charge	N-Ch	—	—	3.9		
		P-Ch	—	—	1.6		
$t_{d(on)}$	Turn-On Delay Time	N-Ch	—	6.0	—	ns	N-Channel V_{DD} = 6.0V, I_D = 1.0A, R_G = 6.0Ω, V_{GS} = 4.5V ② P-Channel V_{DD} = -6.0V, I_D = -2.9A, R_G = 6.0Ω, V_{GS} = -4.5V
		P-Ch	—	9.6	—		
t_r	Rise Time	N-Ch	—	7.6	—		
		P-Ch	—	13	—		
$t_{d(off)}$	Turn-Off Delay Time	N-Ch	—	26	—		
		P-Ch	—	27	—		
t_f	Fall Time	N-Ch	—	34	—		
		P-Ch	—	25	—		
C_{iss}	Input Capacitance	N-Ch	—	640	—	pF	N-Channel V_{GS} = 0V, V_{DS} = 9.0V, ƒ = 1.0MHz P-Channel V_{GS} = 0V, V_{DS} = -9.0V, ƒ = 1.0KHz
		P-Ch	—	490	—		
C_{oss}	Output Capacitance	N-Ch	—	340	—		
		P-Ch	—	80	—		
C_{rss}	Reverse Transfer Capacitance	N-Ch	—	110	—		
		P-Ch	—	58	—		

Source-Drain Ratings and Characteristics

	Parameter		Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	N-Ch	—	—	6.3	A	
		P-Ch	—	—	-3.0		
I_{SM}	Pulsed Source Current (Body Diode) ①	N-Ch	—	—	26		
		P-Ch	—	—	-13		
V_{SD}	Diode Forward Voltage	N-Ch	—	—	1.3	V	T_J = 25°C, I_S = 1.7A, V_{GS} = 0V ②
		P-Ch	—	—	-1.2		T_J = 25°C, I_S = -2.9A, V_{GS} = 0V ②
t_{rr}	Reverse Recovery Time	N-Ch	—	51	76	ns	N-Channel T_J = 25°C, I_F = 1.7A, di/dt = 100A/µs P-Channel ② T_J = 25°C, I_F = -2.9A, di/dt = -100A/µs
		P-Ch	—	37	56		
Q_{rr}	Reverse Recovery Charge	N-Ch	—	43	64	nC	
		P-Ch	—	20	30		

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.

② Pulse width ≤ 400µs; duty cycle ≤ 2%.

③ Surface mounted on 1 in square Cu board.

④ The N-channel MOSFET can withstand 15V V_{GS} max for up to 24 hours over the life of the device.

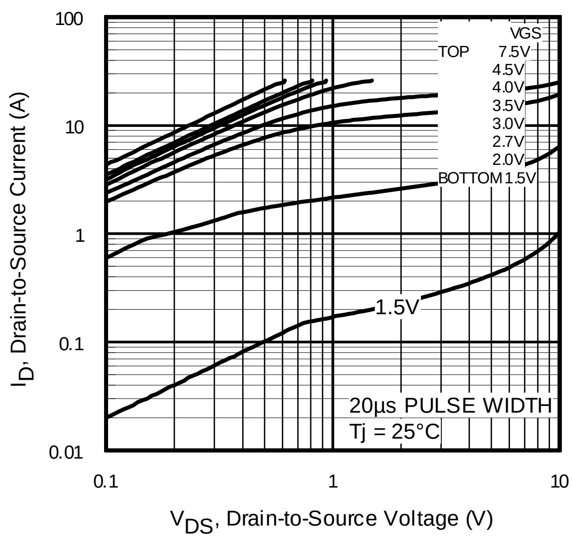


Fig 1. Typical Output Characteristics

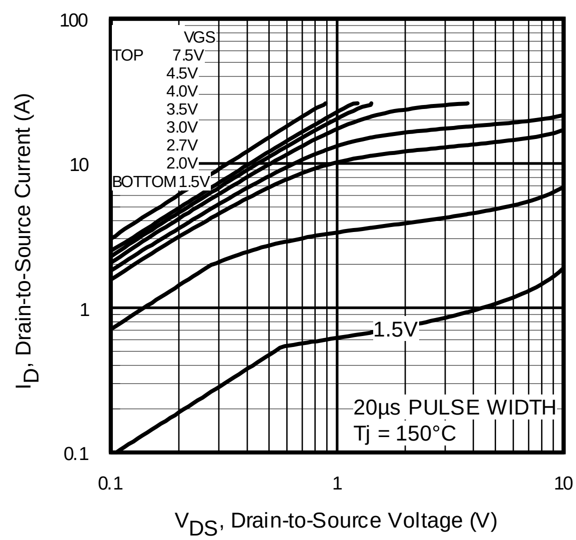


Fig 2. Typical Output Characteristics

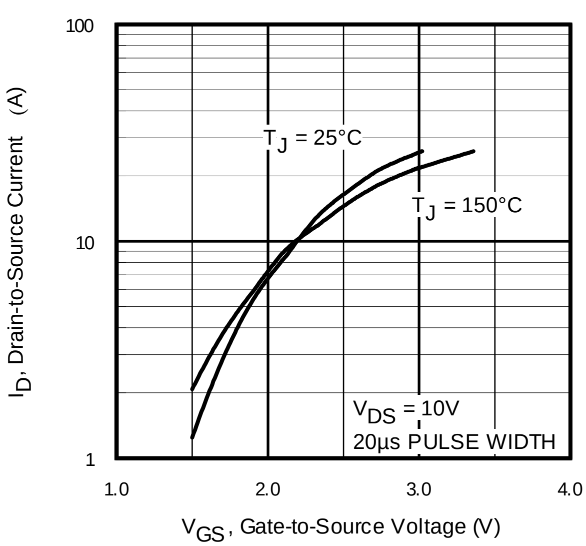


Fig 3. Typical Transfer Characteristics

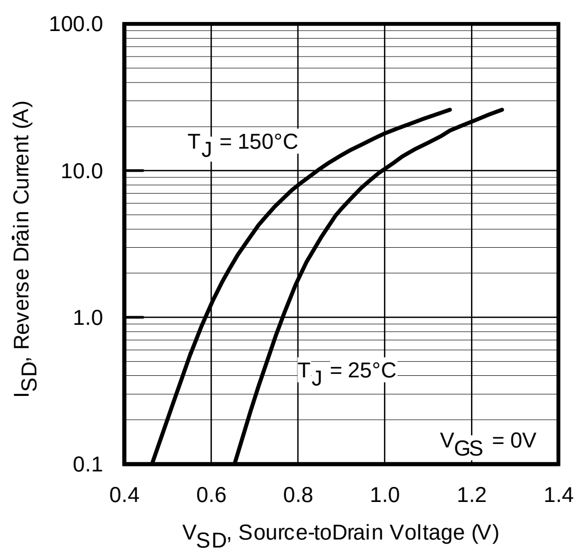


Fig 4. Typical Source-Drain Diode Forward Voltage

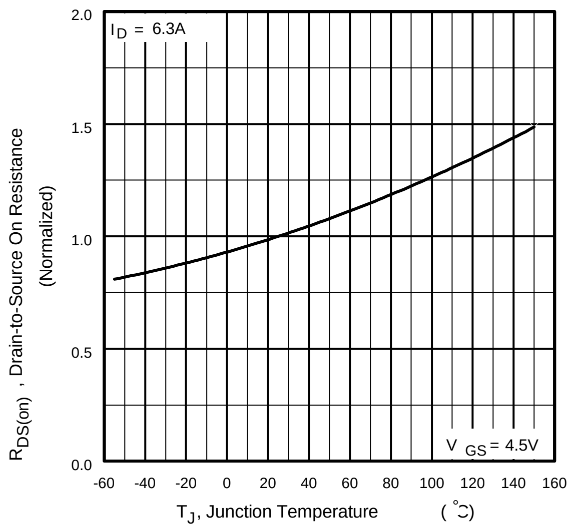


Fig 5. Normalized On-Resistance Vs. Temperature

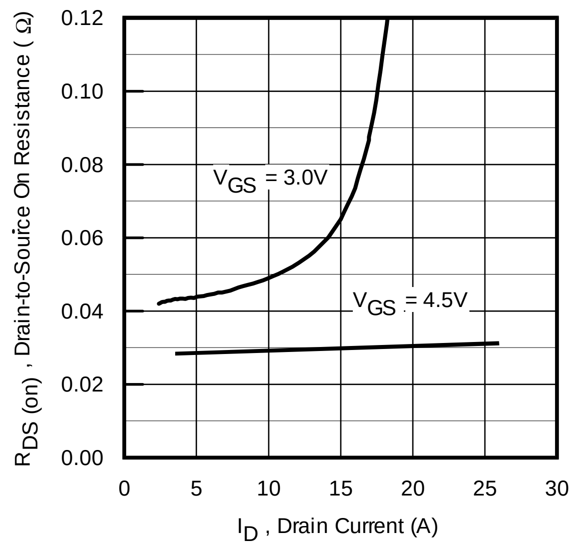


Fig 6. Typical On-Resistance Vs. Drain Current

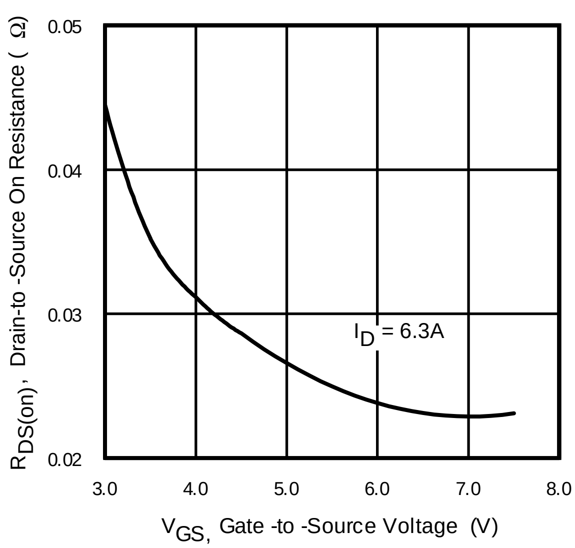


Fig 7. Typical On-Resistance Vs. Gate Voltage

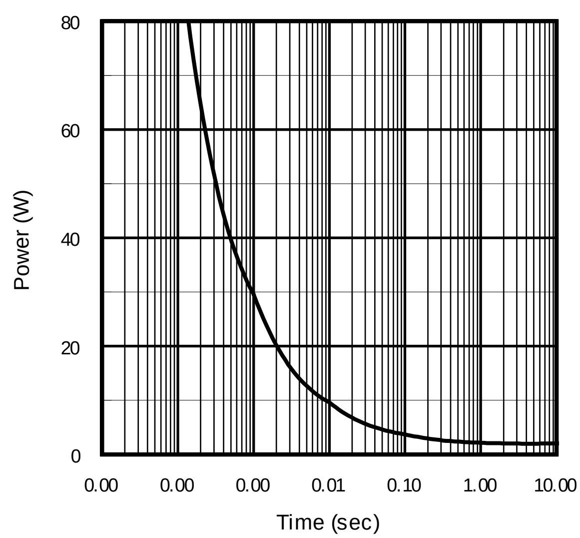


Fig 8. Typical Power Vs. Time

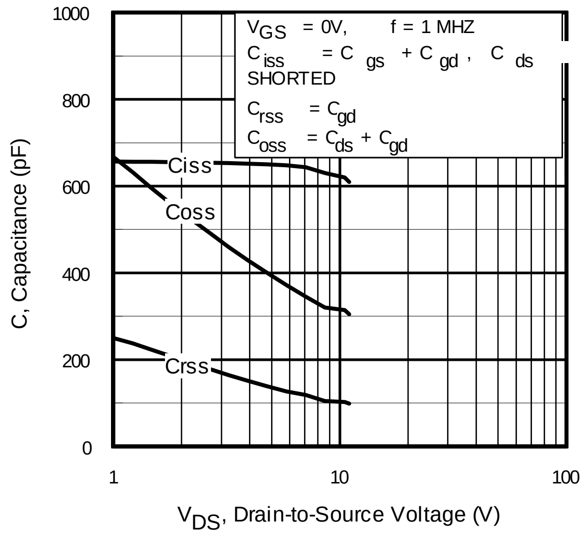


Fig 9. Typical Capacitance Vs. Drain-to-Source Voltage

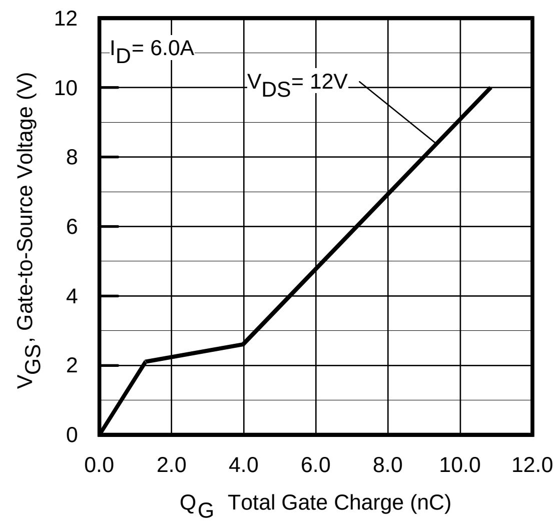


Fig 10. Typical Gate Charge Vs. Gate-to-Source Voltage

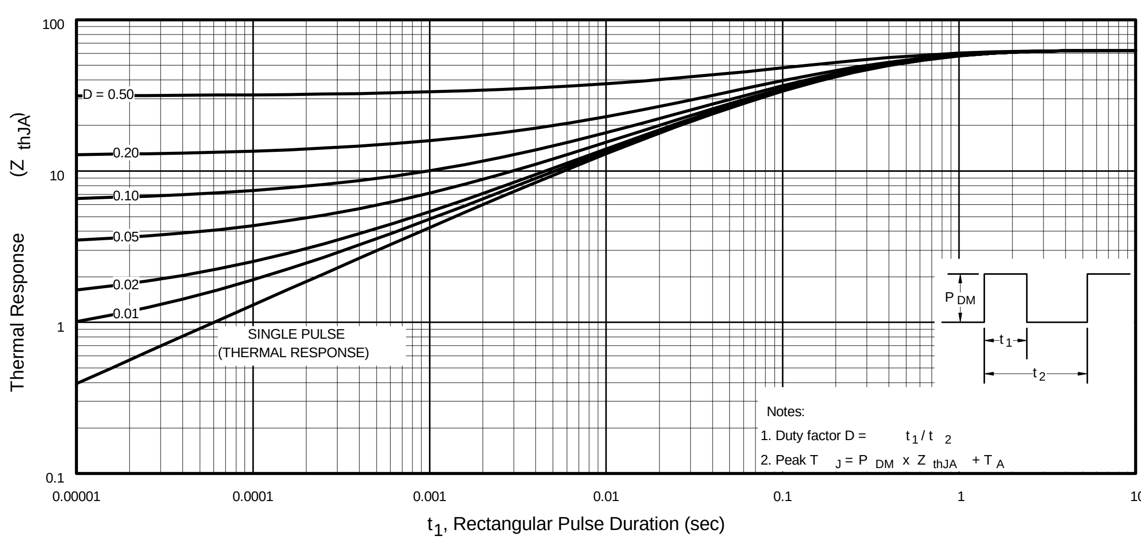


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

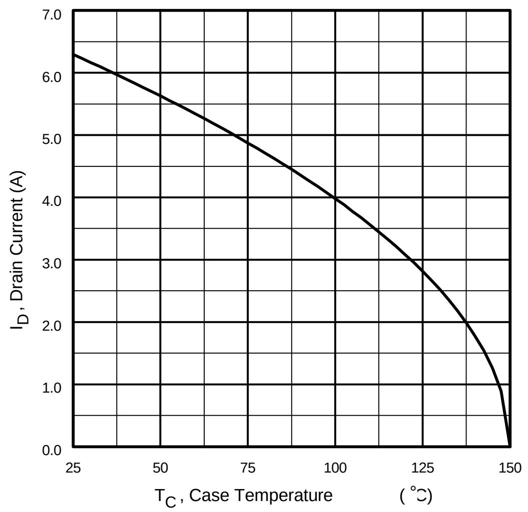


Fig 12. Maximum Drain Current Vs. Case Temperature

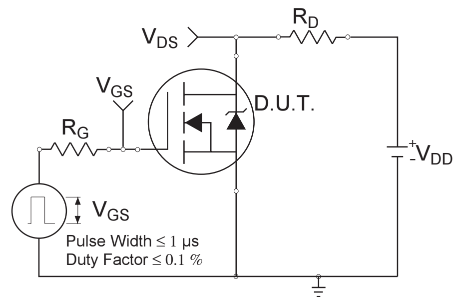


Fig 13a. Switching Time Test Circuit

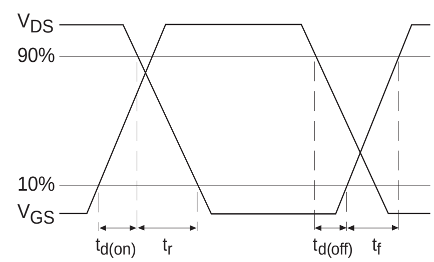


Fig 13b. Switching Time Waveforms

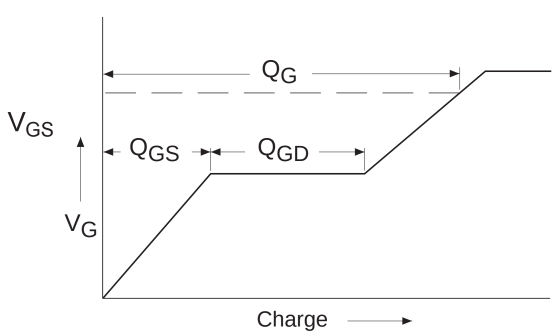


Fig 14a. Basic Gate Charge Waveform

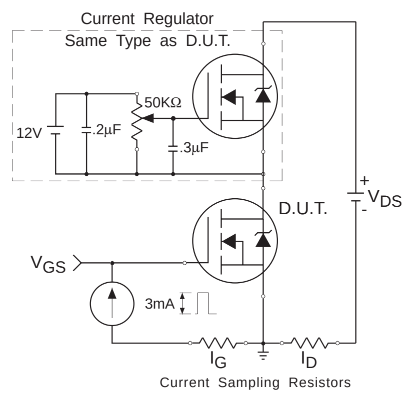


Fig 14b. Gate Charge Test Circuit

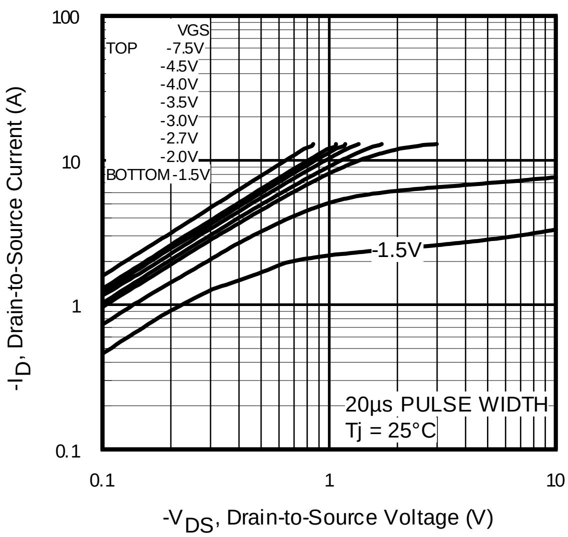


Fig 15. Typical Output Characteristics

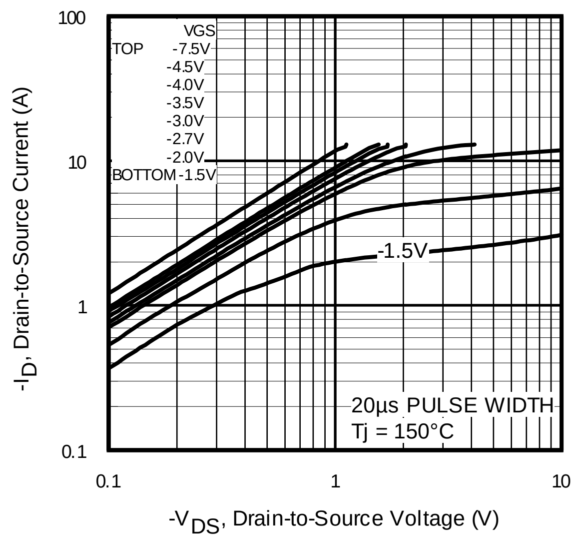


Fig 16. Typical Output Characteristics

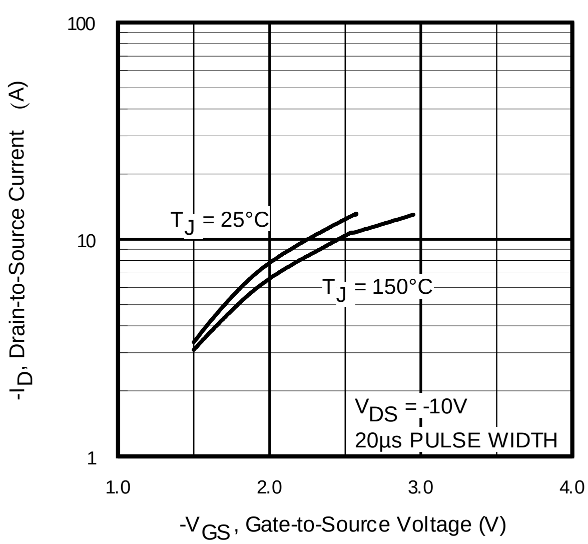


Fig 17. Typical Transfer Characteristics

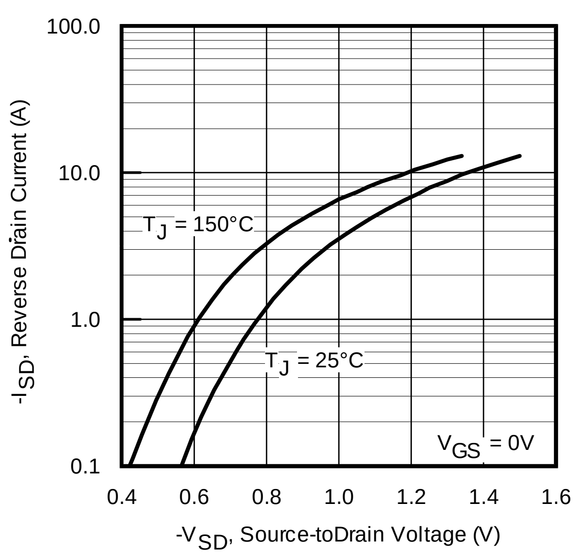


Fig 18. Typical Source-Drain Diode Forward Voltage

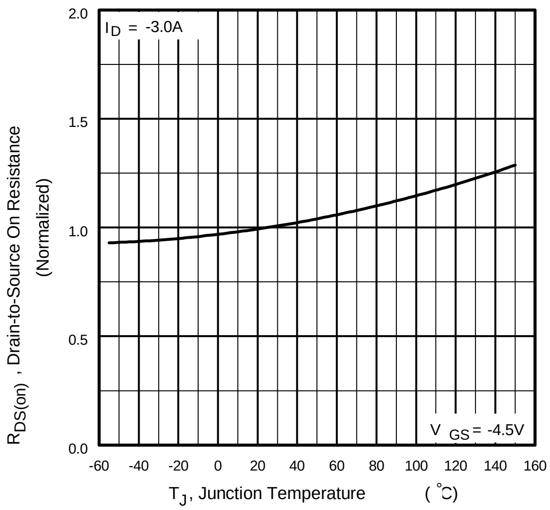


Fig 19. Normalized On-Resistance Vs. Temperature

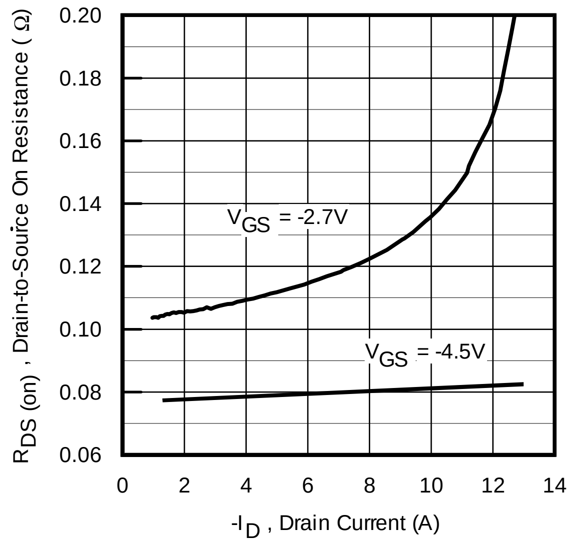


Fig 20. Typical On-Resistance Vs. Drain Current

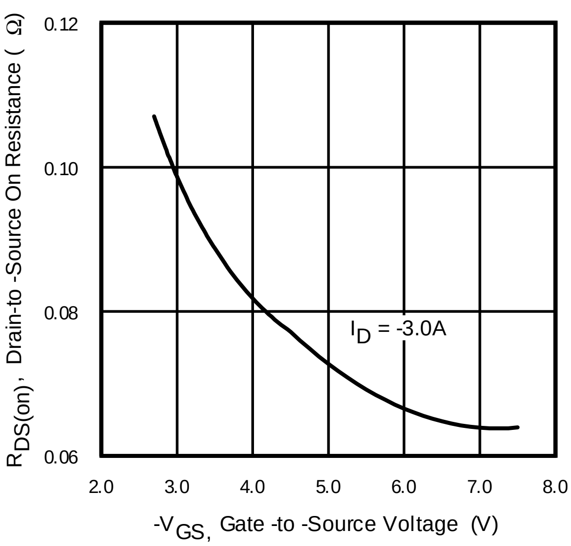


Fig 21. Typical On-Resistance Vs. Gate Voltage

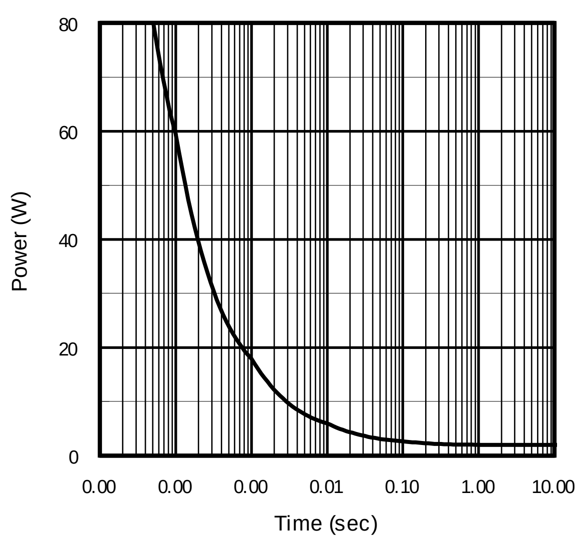


Fig 22. Maximum Avalanche Energy Vs. Drain Current

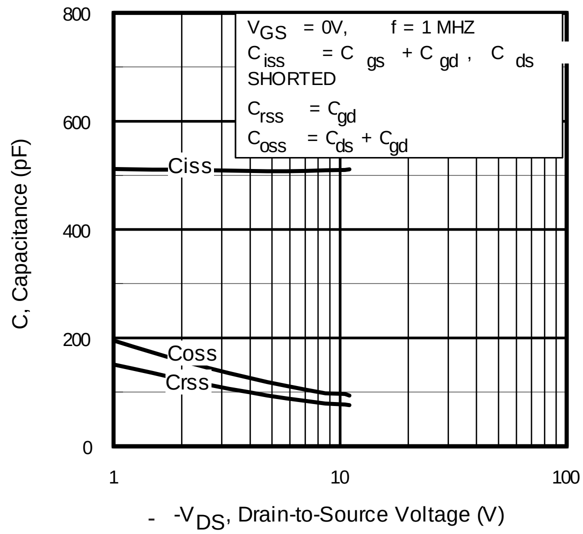


Fig 23. Typical Capacitance Vs. Drain-to-Source Voltage

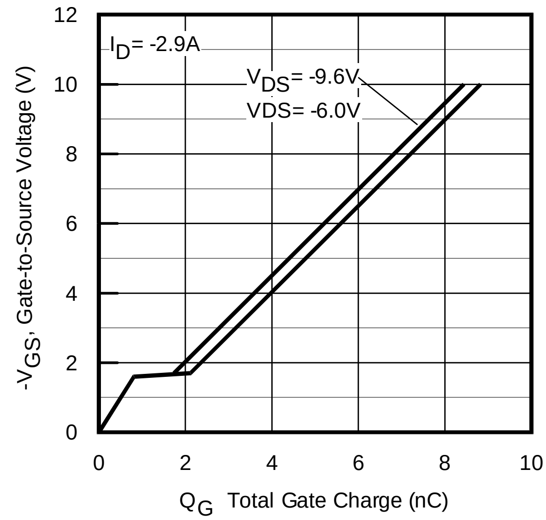


Fig 24. Typical Gate Charge Vs. Gate-to-Source Voltage

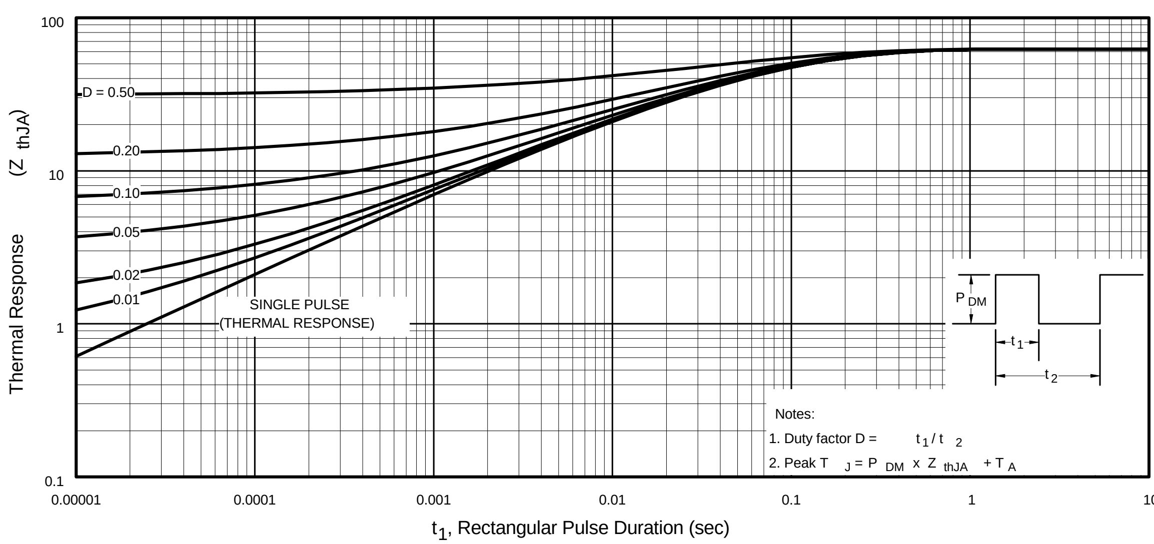


Fig 25. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

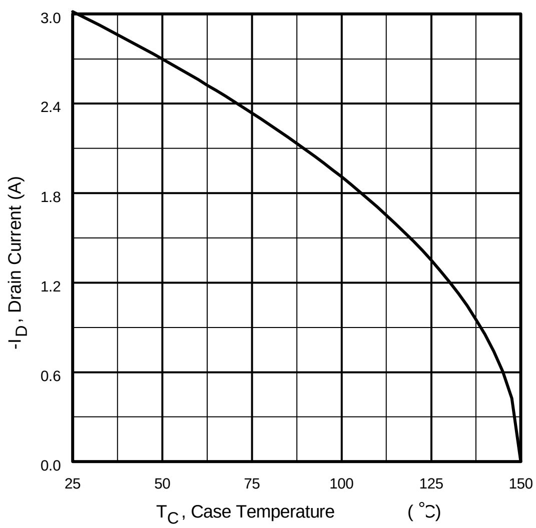


Fig 26. Maximum Drain Current Vs. Case Temperature

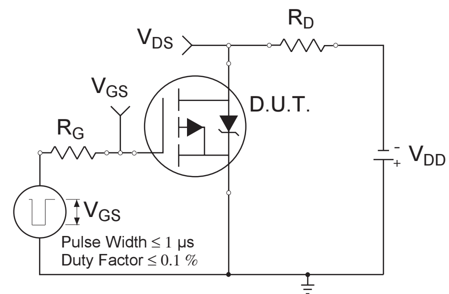


Fig 27a. Switching Time Test Circuit

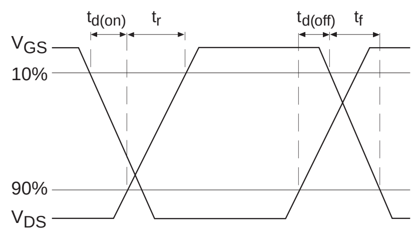


Fig 27b. Switching Time Waveforms

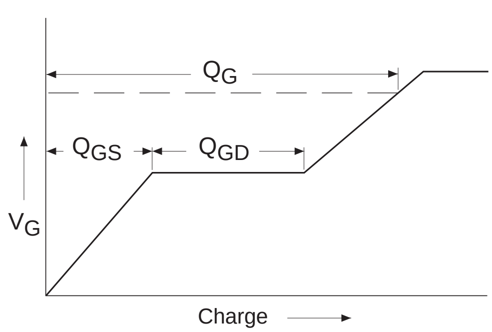


Fig 28a. Basic Gate Charge Waveform

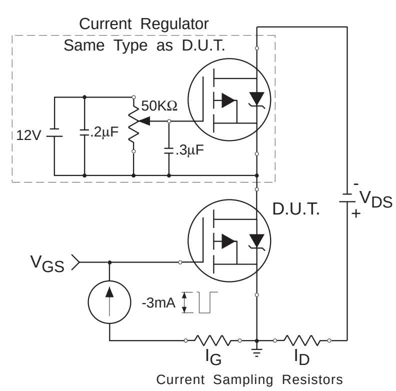
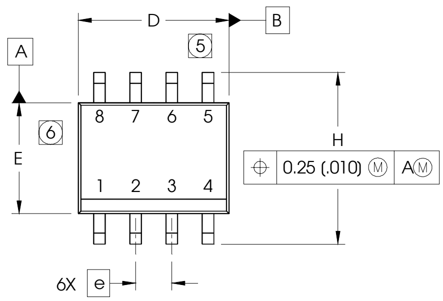
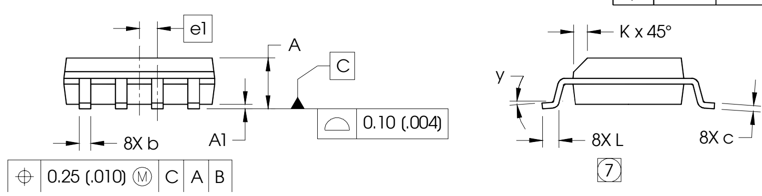


Fig 28b. Gate Charge Test Circuit

SO-8 Package Details

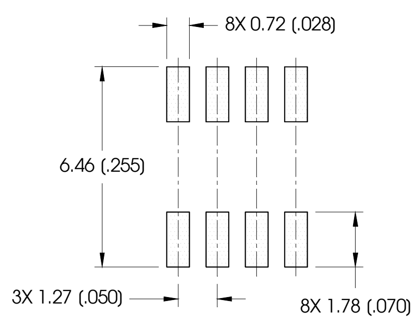


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e 1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°



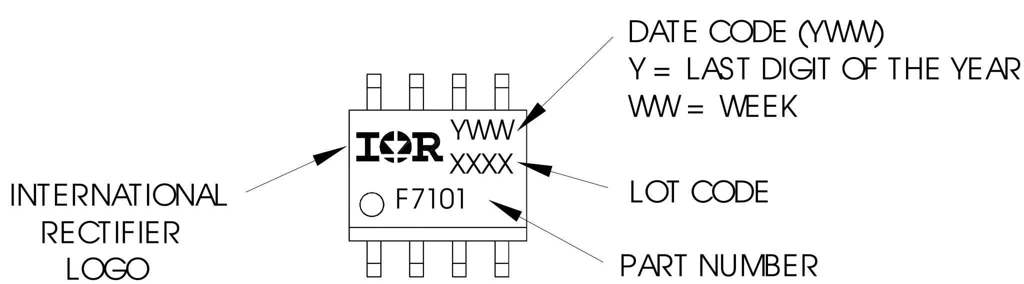
NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [.006].
6. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.010].
7. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

FOOTPRINT

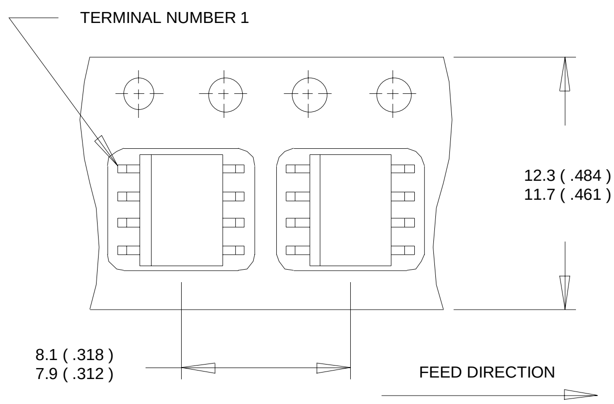


SO-8 Part Marking

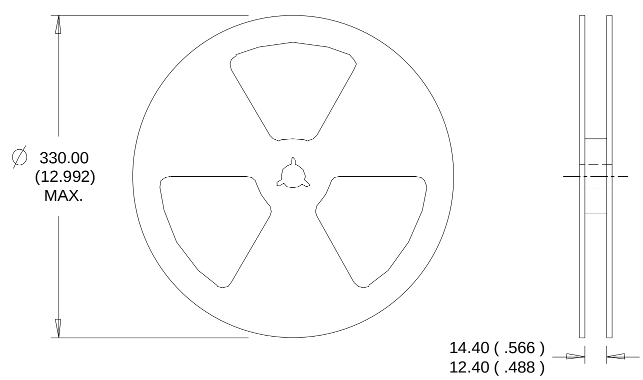
EXAMPLE: THIS IS AN IRF7101 (MOSFET)



SO-8 Tape and Reel



NOTES:
1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS(INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

Data and specifications subject to change without notice.
This product has been designed and qualified for the Consumer market.
Qualification Standards can be found on IR's Web site.

International
IOR Rectifier

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