

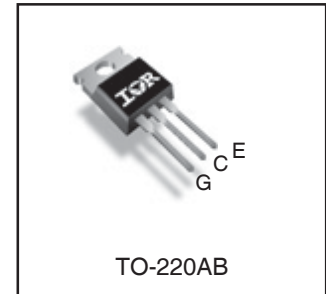
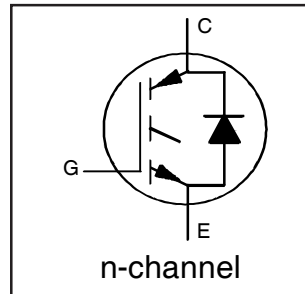
# IRG6B330UDPbF

## PDP TRENCH IGBT

### Features

- Advanced Trench IGBT Technology
- Optimized for Sustain and Energy Recovery Circuits in PDP Applications
- Low  $V_{CE(on)}$  and Energy per Pulse ( $E_{PULSE}^{TM}$ ) for Improved Panel Efficiency
- High Repetitive Peak Current Capability
- Lead Free Package

Key Parameters		
$V_{CE\ min}$	330	V
$V_{CE(on)}\ typ.\ @\ I_C = 70A$	1.69	V
$I_{RP\ max}\ @\ T_C = 25^\circ C$ ①	250	A
$T_J\ max$	150	°C



G	C	E
Gate	Collector	Emitter

### Description

This IGBT is specifically designed for applications in Plasma Display Panels. This device utilizes advanced trench IGBT technology to achieve low  $V_{CE(on)}$  and low  $E_{PULSE}^{TM}$  rating per silicon area which improve panel efficiency. Additional features are 150°C operating junction temperature and high repetitive peak current capability. These features combine to make this IGBT a highly efficient, robust and reliable device for PDP applications.

### Absolute Maximum Ratings

	Parameter	Max.	Units
$V_{GE}$	Gate-to-Emitter Voltage	±30	V
$I_C @ T_C = 25^\circ C$	Continuous Collector Current, $V_{GE} @ 15V$	70	A
$I_C @ T_C = 100^\circ C$	Continuous Collector, $V_{GE} @ 15V$	40	
$I_{RP} @ T_C = 25^\circ C$	Repetitive Peak Current ①	250	
$P_D @ T_C = 25^\circ C$	Power Dissipation	160	W
$P_D @ T_C = 100^\circ C$	Power Dissipation	63	
	Linear Derating Factor	1.3	W/°C
$T_J$	Operating Junction and	-40 to + 150	°C
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature for 10 seconds	300	
	Mounting Torque, 6-32 or M3 Screw	10lb·in (1.1N·m)	N

### Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$ (IGBT)	Thermal Resistance Junction-to-Case-(each IGBT) ②	—	0.80	°C/W
$R_{\theta JC}$ (Diode)	Thermal Resistance Junction-to-Case-(each Diode) ②	1.6	2.4	
$R_{\theta CS}$	Case-to-Sink (flat, greased surface)	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient (typical socket mount) ②	—	40	
	Weight	6.0 (0.21)	—	g (oz)

## Electrical Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV <sub>CES</sub>	Collector-to-Emitter Breakdown Voltage	330	—	—	V	V <sub>GE</sub> = 0V, I <sub>CE</sub> = 1 mA
ΔBV <sub>CES</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	—	0.34	—	V/°C	Reference to 25°C, I <sub>CE</sub> = 1mA
V <sub>CE(on)</sub>	Static Collector-to-Emitter Voltage	—	1.18	1.48	V	V <sub>GE</sub> = 15V, I <sub>CE</sub> = 25A ③
		—	1.36	1.68		V <sub>GE</sub> = 15V, I <sub>CE</sub> = 40A ③
		—	1.69	2.09		V <sub>GE</sub> = 15V, I <sub>CE</sub> = 70A ③
		—	2.26	2.76		V <sub>GE</sub> = 15V, I <sub>CE</sub> = 120A ③
		—	1.93	—		V <sub>GE</sub> = 15V, I <sub>CE</sub> = 70A, T <sub>J</sub> = 150°C
V <sub>GE(th)</sub>	Gate Threshold Voltage	2.6	—	5.0	V	V <sub>CE</sub> = V <sub>GE</sub> , I <sub>CE</sub> = 500μA
ΔV <sub>GE(th)</sub> /ΔT <sub>J</sub>	Gate Threshold Voltage Coefficient	—	-11	—	mV/°C	
I <sub>CES</sub>	Collector-to-Emitter Leakage Current	—	2.0	25	μA	V <sub>CE</sub> = 330V, V <sub>GE</sub> = 0V
		—	5.0	—		V <sub>CE</sub> = 330V, V <sub>GE</sub> = 0V, T <sub>J</sub> = 100°C
		—	100	—		V <sub>CE</sub> = 330V, V <sub>GE</sub> = 0V, T <sub>J</sub> = 150°C
I <sub>GES</sub>	Gate-to-Emitter Forward Leakage	—	—	100	nA	V <sub>GE</sub> = 30V
	Gate-to-Emitter Reverse Leakage	—	—	-100		V <sub>GE</sub> = -30V
g <sub>fe</sub>	Forward Transconductance	—	50	—	S	V <sub>CE</sub> = 25V, I <sub>CE</sub> = 25A
Q <sub>g</sub>	Total Gate Charge	—	85	—	nC	V <sub>CE</sub> = 200V, I <sub>C</sub> = 25A, V <sub>GE</sub> = 15V ③
Q <sub>gc</sub>	Gate-to-Collector Charge	—	31	—		
t <sub>d(on)</sub>	Turn-On delay time	—	47	—	ns	I <sub>C</sub> = 25A, V <sub>CC</sub> = 196V R <sub>G</sub> = 10Ω, L = 200μH, L <sub>S</sub> = 200nH T <sub>J</sub> = 25°C
t <sub>r</sub>	Rise time	—	37	—		
t <sub>d(off)</sub>	Turn-Off delay time	—	176	—		
t <sub>f</sub>	Fall time	—	99	—		
t <sub>d(on)</sub>	Turn-On delay time	—	45	—	ns	I <sub>C</sub> = 25A, V <sub>CC</sub> = 196V R <sub>G</sub> = 10Ω, L = 200μH, L <sub>S</sub> = 200nH T <sub>J</sub> = 150°C
t <sub>r</sub>	Rise time	—	38	—		
t <sub>d(off)</sub>	Turn-Off delay time	—	228	—		
t <sub>f</sub>	Fall time	—	183	—		
t <sub>st</sub>	Shoot Through Blocking Time	100	—	—	ns	V <sub>CC</sub> = 240V, V <sub>GE</sub> = 15V, R <sub>G</sub> = 5.1Ω L = 220nH, C = 0.40μF, V <sub>GE</sub> = 15V V <sub>CC</sub> = 240V, R <sub>G</sub> = 5.1Ω, T <sub>J</sub> = 25°C
E <sub>PULSE</sub>	Energy per Pulse	—	834	—	μJ	L = 220nH, C = 0.40μF, V <sub>GE</sub> = 15V V <sub>CC</sub> = 240V, R <sub>G</sub> = 5.1Ω, T <sub>J</sub> = 25°C
		—	985	—		L = 220nH, C = 0.40μF, V <sub>GE</sub> = 15V V <sub>CC</sub> = 240V, R <sub>G</sub> = 5.1Ω, T <sub>J</sub> = 100°C
C <sub>iss</sub>	Input Capacitance	—	2297	—	pF	V <sub>GE</sub> = 0V V <sub>CE</sub> = 30V f = 1.0MHz, See Fig.13
C <sub>oss</sub>	Output Capacitance	—	141	—		
C <sub>rss</sub>	Reverse Transfer Capacitance	—	74	—		
L <sub>C</sub>	Internal Collector Inductance	—	5.0	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L <sub>E</sub>	Internal Emitter Inductance	—	13	—		

## Diode Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>F(AV)</sub>	Average Forward Current at T <sub>C</sub> =155°C	—	—	8.0	A	
I <sub>FSM</sub>	Non Repetitive Peak Surge Current	—	—	100	A	T <sub>J</sub> = 155°C, PW = 6.0ms half sine wave
V <sub>F</sub>	Forward Voltage	—	1.19	1.3	V	I <sub>F</sub> = 8A
		—	0.94	1.0		I <sub>F</sub> = 8A, T <sub>J</sub> = 150°C
t <sub>rr</sub>	Reverse Recovery Time	—	35	60	ns	I <sub>F</sub> = 1A, di/dt = -50A/μs, V <sub>R</sub> = 30V
		—	43	—		T <sub>J</sub> = 25°C
		—	67	—		T <sub>J</sub> = 125°C
Q <sub>rr</sub>	Reverse Recovery Charge	—	60	—	nC	T <sub>J</sub> = 25°C
		—	210	—		T <sub>J</sub> = 125°C
I <sub>rr</sub>	Peak Recovery Current	—	2.8	—	A	T <sub>J</sub> = 25°C
		—	6.3	—		T <sub>J</sub> = 125°C

### Notes:

- ① Half sine wave with duty cycle = 0.1, ton=2μsec.  
② R<sub>θ</sub> is measured at T<sub>J</sub> of approximately 90°C.

③ Pulse width ≤ 400μs; duty cycle ≤ 2%.

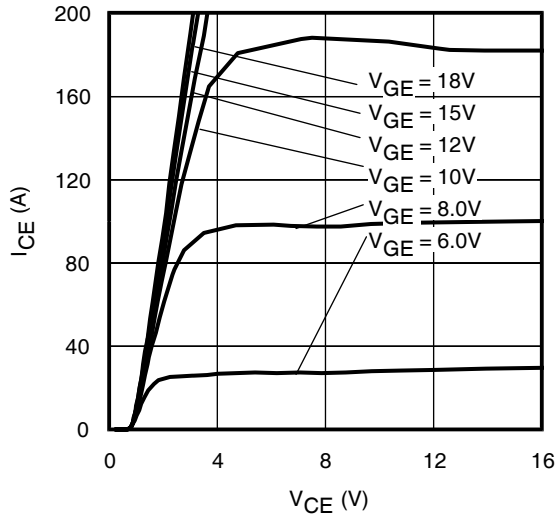


Fig 1. Typical Output Characteristics @ 25°C

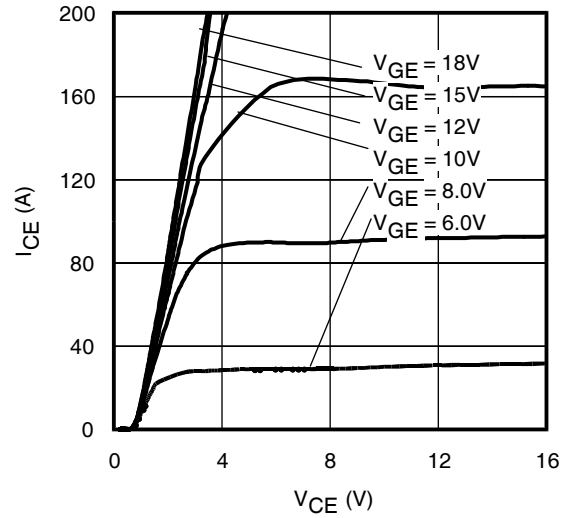


Fig 2. Typical Output Characteristics @ 75°C

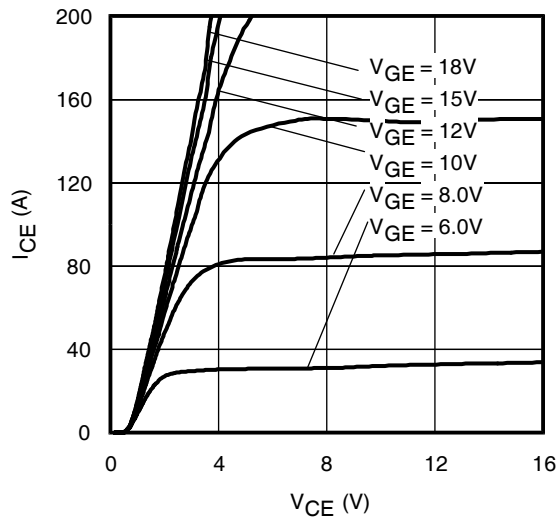


Fig 3. Typical Output Characteristics @ 125°C

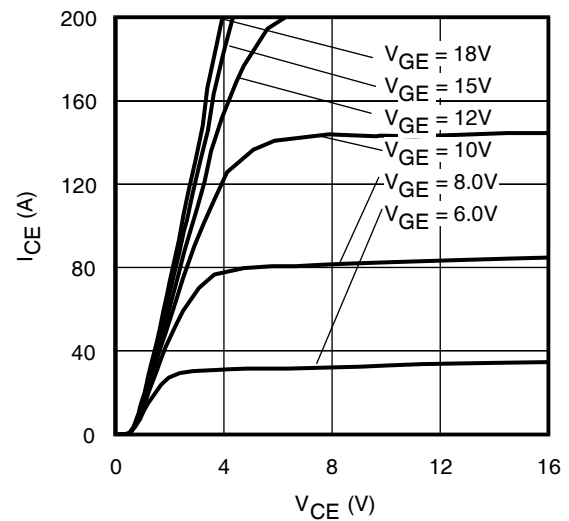


Fig 4. Typical Output Characteristics @ 150°C

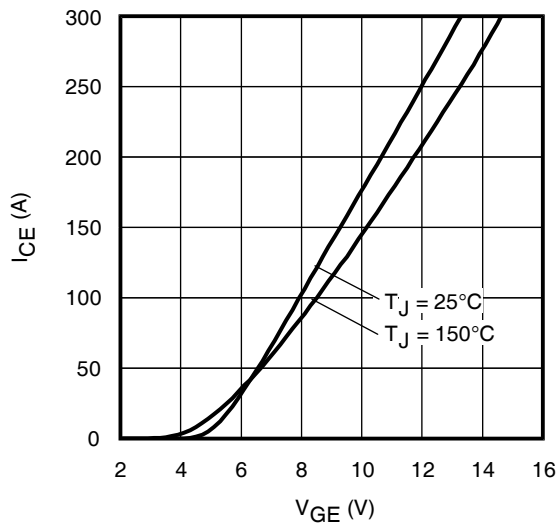


Fig 5. Typical Transfer Characteristics

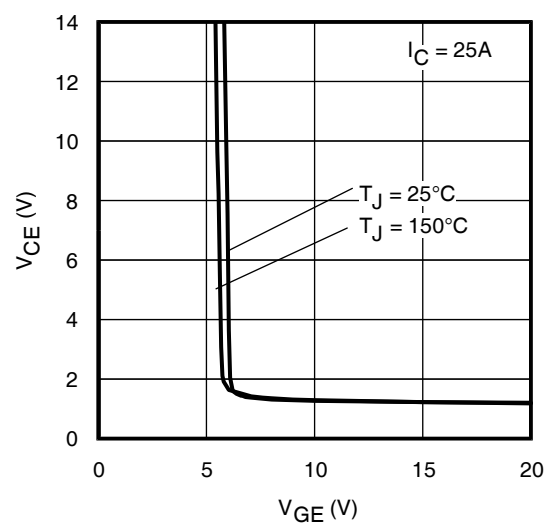


Fig 6.  $V_{CE(ON)}$  vs. Gate Voltage

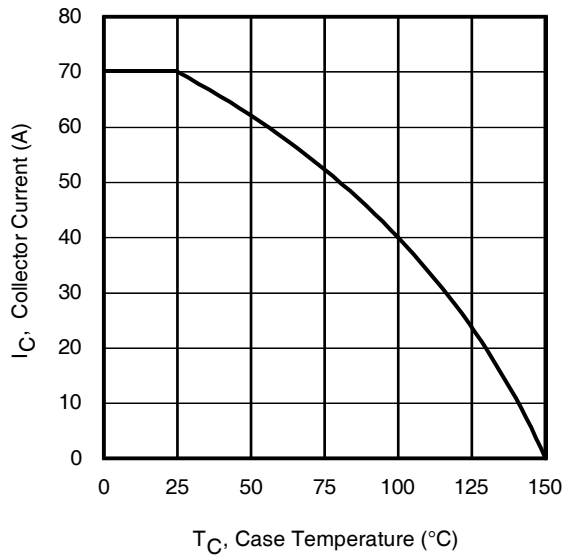


Fig 7. Maximum Collector Current vs. Case Temperature

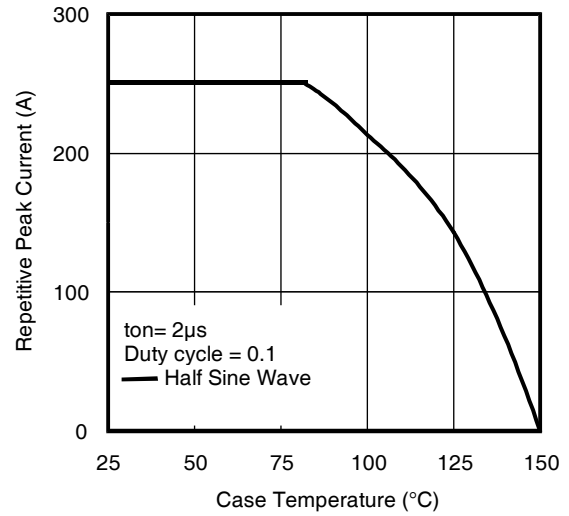


Fig 8. Typical Repetitive Peak Current vs. Case Temperature

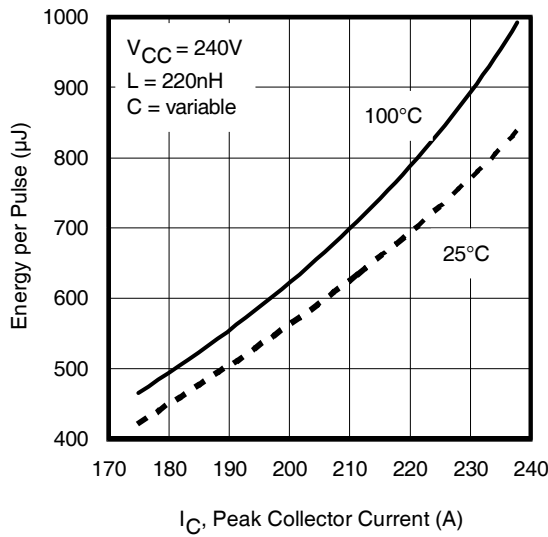


Fig 9. Typical  $E_{PULSE}$  vs. Collector Current

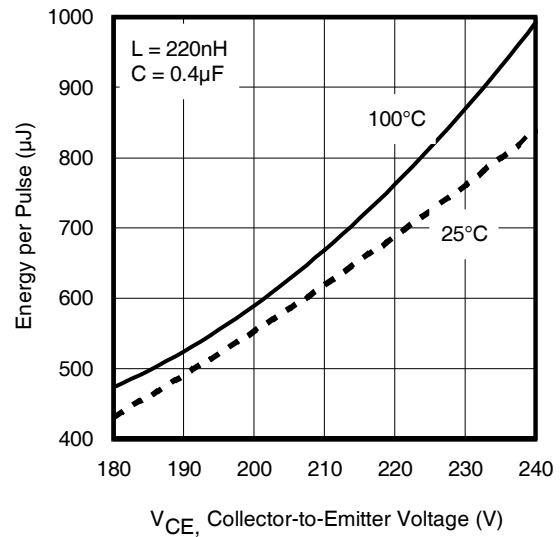


Fig 10. Typical  $E_{PULSE}$  vs. Collector-to-Emitter Voltage

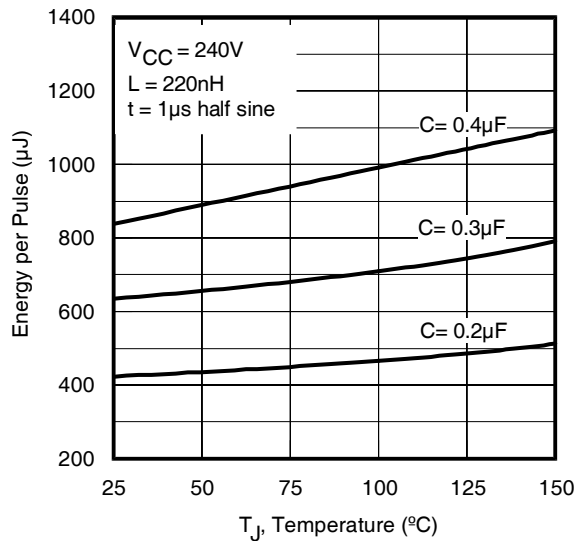


Fig 11.  $E_{PULSE}$  vs. Temperature

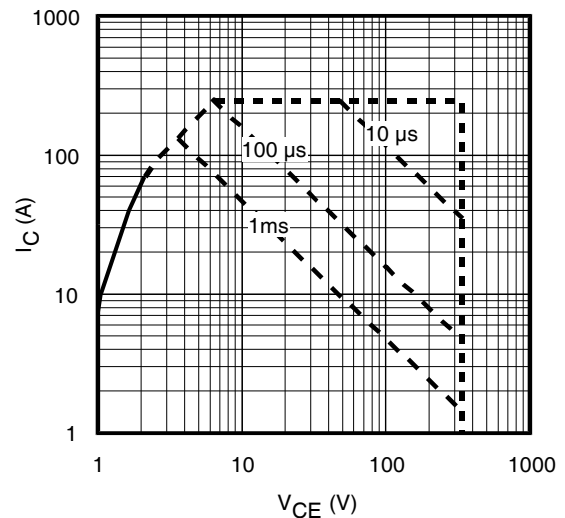


Fig 12. Forward Bias Safe Operating Area

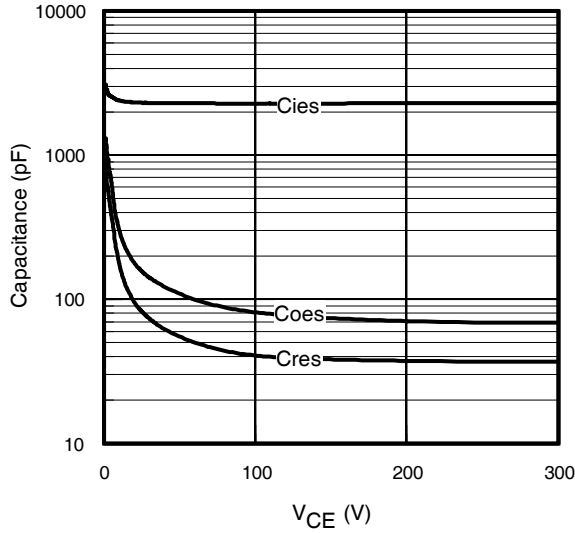


Fig 13. Typical Capacitance vs. Collector-to-Emitter Voltage

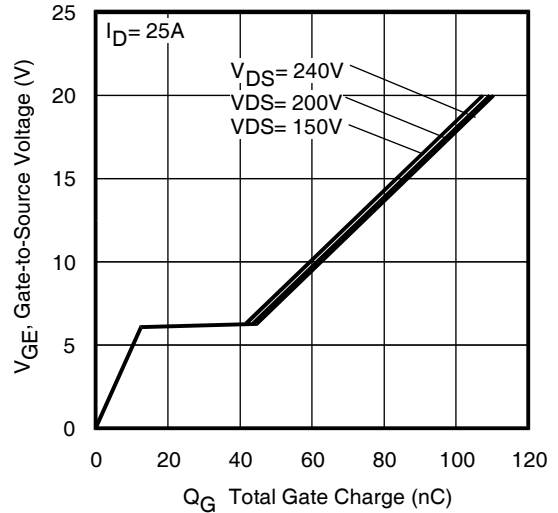


Fig 14. Typical Gate Charge vs. Gate-to-Emitter Voltage

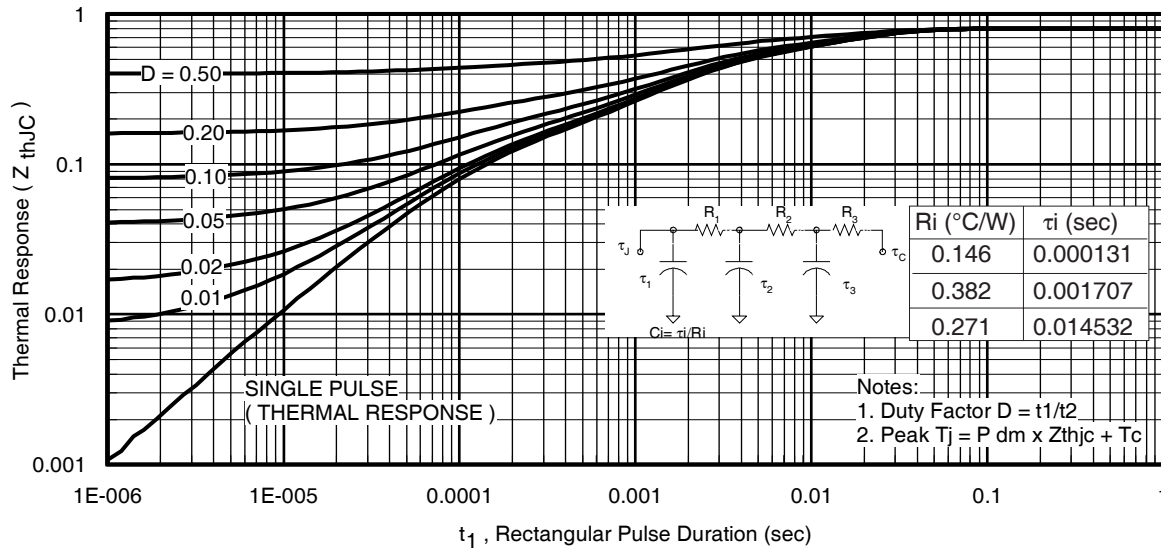


Fig 15. Maximum Effective Transient Thermal Impedance, Junction-to-Case (IGBT)

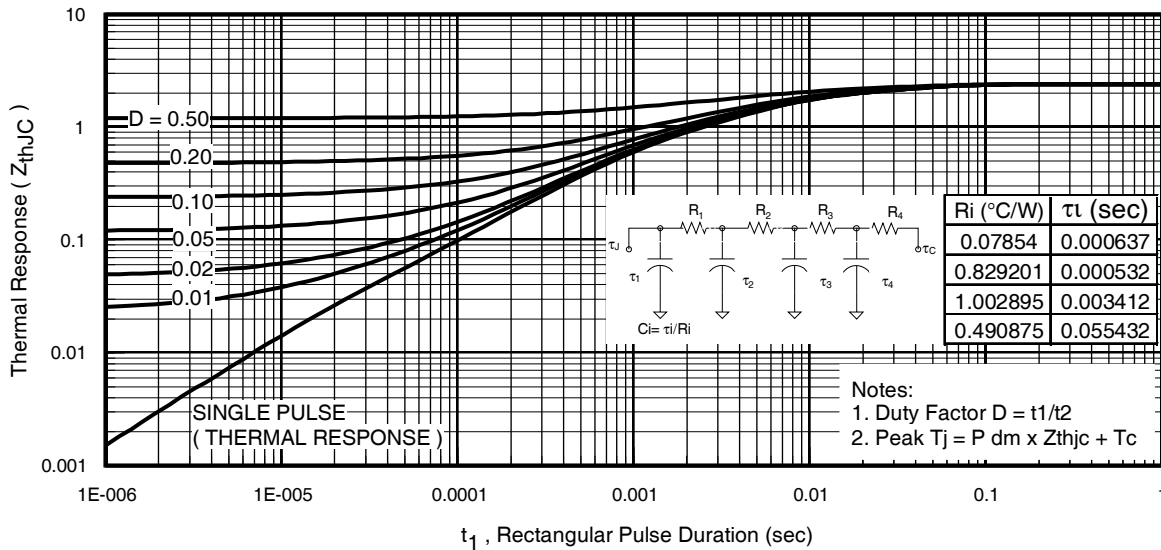


Fig 16. Maximum Effective Transient Thermal Impedance, Junction-to-Case (DIODE)

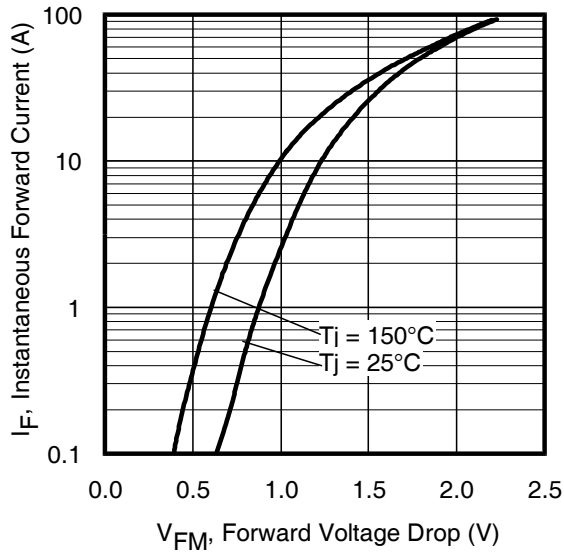


Fig. 17 - Typical Forward Voltage Drop Characteristics

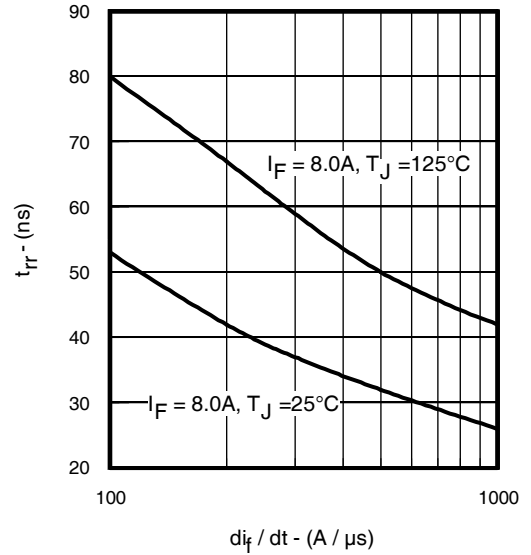


Fig. 18 - Typical Reverse Recovery vs.  $di_F/dt$

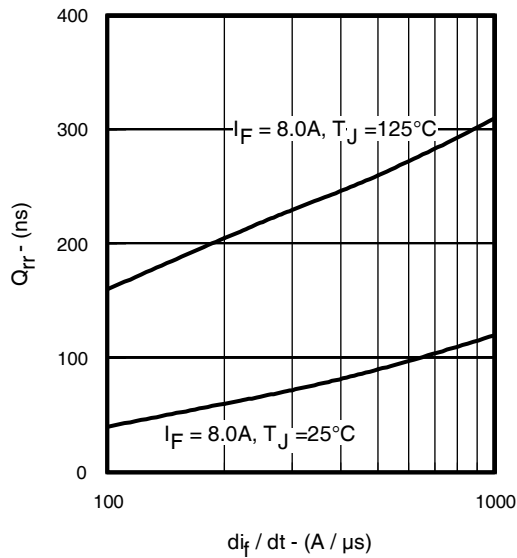


Fig. 19 - Typical Stored Charge vs.  $di_F/dt$

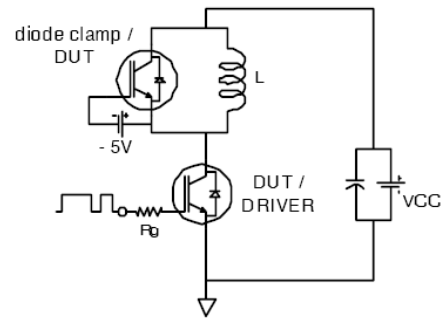


Fig. 20 - Switching Loss Circuit

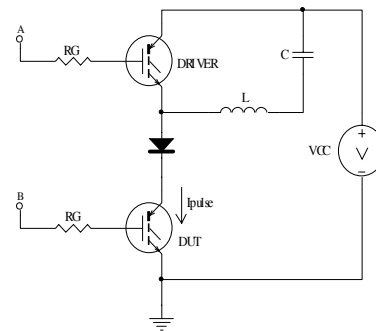


Fig 21a.  $t_{st}$  and  $E_{PULSE}$  Test Circuit

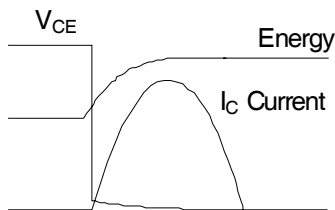


Fig 21b.  $t_{st}$  Test Waveforms

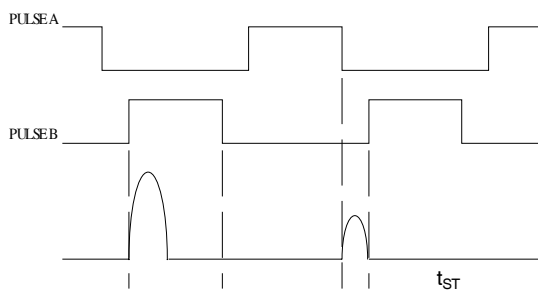


Fig 21c.  $E_{PULSE}$  Test Waveforms

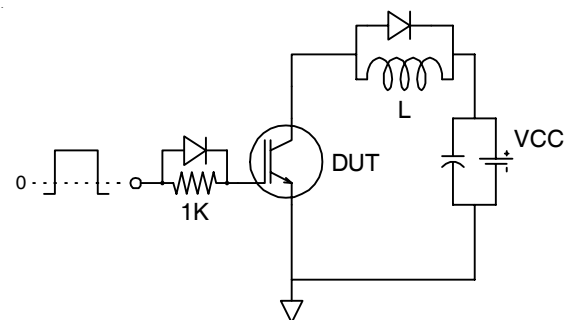
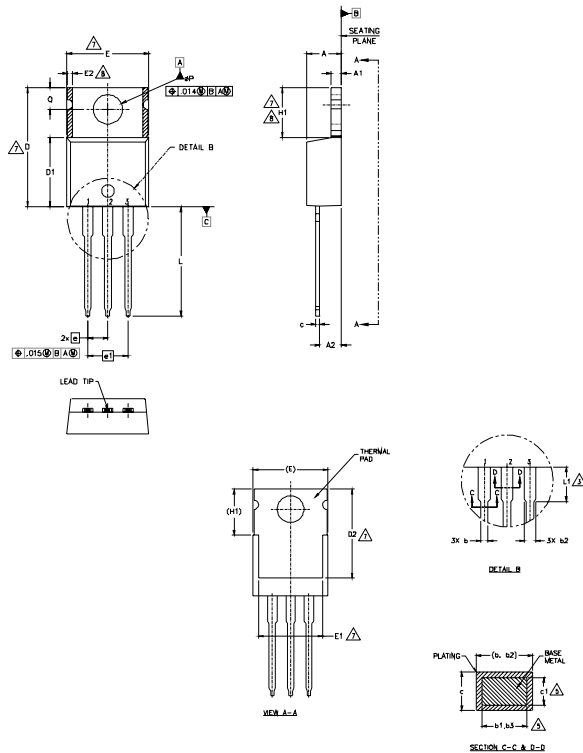


Fig. 22 - Gate Charge Circuit (turn-off)

## TO-220AB Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

- 1.- DIMENSIONING AND TOLERANCING AS PER ASME Y14.5 M- 1994.
- 2.- DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
- 3.- LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
- 4.- DIMENSION D, D1 & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- 5.- DIMENSION b1, b3 & c1 APPLY TO BASE METAL ONLY.
- 6.- CONTROLLING DIMENSION : INCHES.
- 7.- THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS E,H1,D2 & E1
- 8.- DIMENSION E2 X H1 DEFINE A ZONE WHERE STAMPING AND SINGULATION IRREGULARITIES ARE ALLOWED.
- 9.- OUTLINE CONFORMS TO JEDEC TO-220, EXCEPT A2 (max.) AND D2 (min.) WHERE DIMENSIONS ARE DERIVED FROM THE ACTUAL PACKAGE OUTLINE.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	3.56	4.83	.140	.190	
A1	0.51	1.40	.020	.055	
A2	2.03	2.92	.080	.115	
b	0.38	1.01	.015	.040	
b1	0.38	0.97	.015	.038	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.36	0.61	.014	.024	
c1	0.36	0.56	.014	.022	5
D	14.22	16.51	.560	.650	4
D1	8.38	9.02	.330	.355	
D2	11.68	12.88	.460	.507	7
E	9.65	10.67	.380	.420	4,7
E1	6.86	8.89	.270	.350	7
E2	-	0.76	-	.030	8
e	2.54 BSC		.100 BSC		
e1	5.08 BSC		.200 BSC		
H1	5.84	6.86	.230	.270	7,8
L	12.70	14.73	.500	.580	
L1	3.56	4.06	.140	.160	3
φP	3.54	4.08	.139	.161	
Q	2.54	3.42	.100	.135	

LEAD ASSIGNMENTS

- HEXFET  
1.- GATE  
2.- DRAIN  
3.- SOURCE

IGBTs, CoPACK

- 1.- GATE  
2.- COLLECTOR  
3.- EMITTER

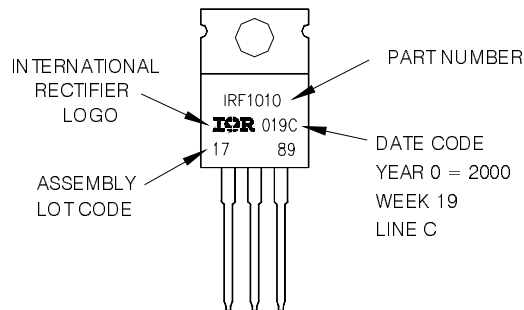
MODES

- 1.- ANODE  
2.- CATHODE  
3.- ANODE

## TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010  
LOT CODE 1789  
ASSEMBLED ON WW 19, 2000  
IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position indicates "Lead - Free"



TO-220AB packages are not recommended for Surface Mount Application.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/pkight.html>

Data and specifications subject to change without notice.  
This product has been designed for the Industrial market.  
Qualification Standards can be found on IR's Web site.

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