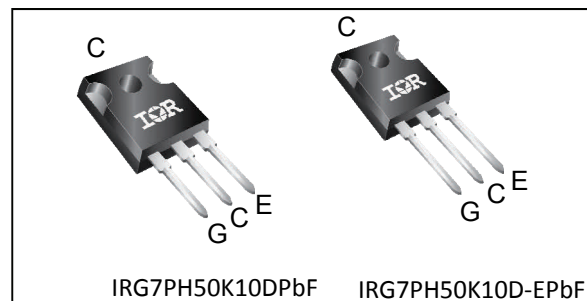
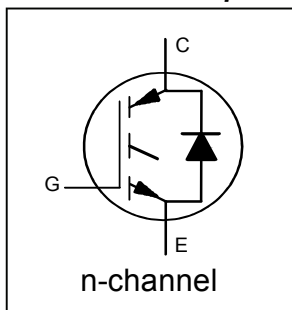


$V_{CES} = 1200V$
$I_C = 50A, T_C = 100^\circ C$
$t_{SC} \geq 10\mu s, T_{J(max)} = 150^\circ C$
$V_{CE(ON)} \text{ typ.} = 1.9V @ I_C = 35A$

**Insulated Gate Bipolar Transistor with Ultrafast Soft Recovery Diode**



G	C	E
Gate	Collector	Emitter

**Applications**

- Industrial Motor Drive
- UPS
- Solar Inverters
- Welding

Features	Benefits
Low $V_{CE(ON)}$ and switching losses	High efficiency in a Wide Range of Applications
$10\mu s$ Short Circuit SOA	Rugged Transient Performance
Square RBSOA	Increased Reliability
Maximum Junction Temperature $150^\circ C$	Excellent Current Sharing in Parallel Operation
Positive $V_{CE(ON)}$ Temperature Coefficient	

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRG7PH50K10DPbF	TO-247AC	Tube	25	IRG7PH50K10DPbF
IRG7PH50K10D-EPbF	TO-247AD	Tube	25	IRG7PH50K10D-EPbF

**Absolute Maximum Ratings**

	Parameter	Max.	Units
$V_{CES}$	Collector-to-Emitter Voltage	1200	V
$I_C @ T_C = 25^\circ C$	Continuous Collector Current	90	A
$I_C @ T_C = 100^\circ C$	Continuous Collector Current	50	
$I_{CM}$	Pulse Collector Current, $V_{GE}=20V$	160	
$I_{LM}$	Clamped Inductive Load Current, $V_{GE}=20V$ ①	160	
$I_F @ T_C = 25^\circ C$	Diode Continuous Forward Current	20	
$I_F @ T_C = 100^\circ C$	Diode Continuous Forward Current	10	
$V_{GE}$	Continuous Gate-to-Emitter Voltage	$\pm 30$	V
$P_D @ T_C = 25^\circ C$	Maximum Power Dissipation	400	W
$P_D @ T_C = 100^\circ C$	Maximum Power Dissipation	160	
$T_J$ $T_{STG}$	Operating Junction and Storage Temperature Range	-40 to +150	C
	Soldering Temperature, for 10 sec.	300 (0.063 in. (1.6mm) from case)	
	Mounting Torque, 6-32 or M3 Screw	10 lbf-in (1.1 N·m)	

**Thermal Resistance**

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$ (IGBT)	Thermal Resistance Junction-to-Case-(each IGBT) ②	—	—	0.3	$^\circ C/W$
$R_{\theta JC}$ (Diode)	Thermal Resistance Junction-to-Case-(each Diode) ②	—	—	1.4	
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink (flat, greased surface)	—	0.24	—	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (typical socket mount)	—	—	40	

**Electrical Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)**

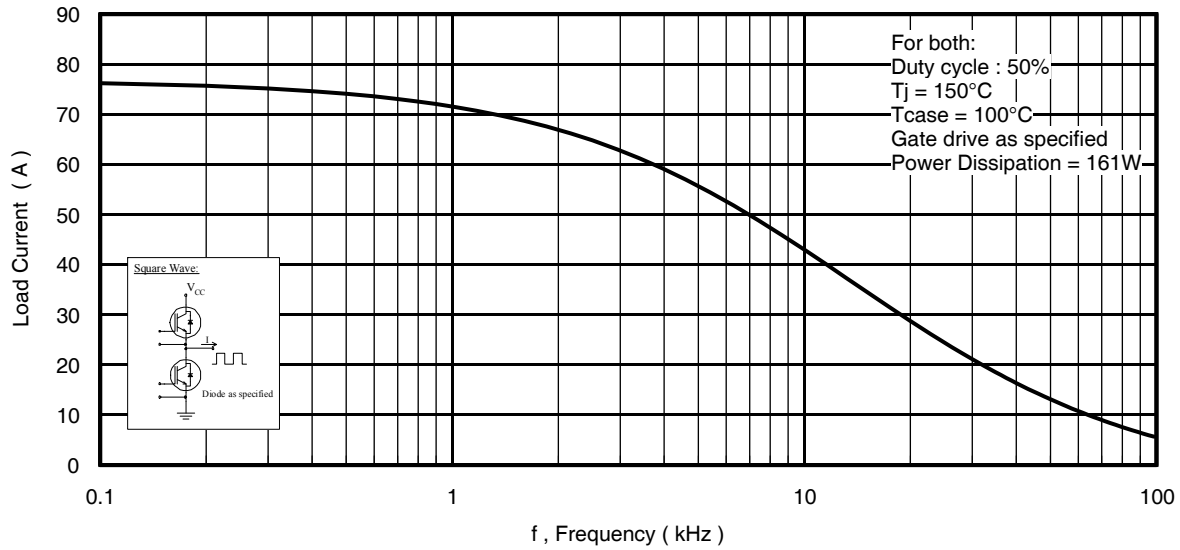
	Parameter	Min.	Typ.	Max.	Units	Conditions
V <sub>(BR)CES</sub>	Collector-to-Emitter Breakdown Voltage	1200	—	—	V	V <sub>GE</sub> = 0V, I <sub>C</sub> = 250μA ③
ΔV <sub>(BR)CES</sub> /ΔT <sub>J</sub>	Temperature Coeff. of Breakdown Voltage	—	1.4	—	V/°C	V <sub>GE</sub> = 0V, I <sub>C</sub> = 2mA (25°C-150°C)
V <sub>CE(on)</sub>	Collector-to-Emitter Saturation Voltage	—	1.9	2.4	V	I <sub>C</sub> = 35A, V <sub>GE</sub> = 15V, T <sub>J</sub> = 25°C
		—	2.4	—		I <sub>C</sub> = 35A, V <sub>GE</sub> = 15V, T <sub>J</sub> = 150°C
V <sub>GE(th)</sub>	Gate Threshold Voltage	5.0	—	7.5	V	V <sub>CE</sub> = V <sub>GE</sub> , I <sub>C</sub> = 1.7mA
ΔV <sub>GE(th)</sub> /ΔT <sub>J</sub>	Threshold Voltage Temperature Coeff.	—	-16	—	mV/°C	V <sub>CE</sub> = V <sub>GE</sub> , I <sub>C</sub> = 1.7mA (25°C-150°C)
g <sub>fe</sub>	Forward Transconductance	—	20	—	S	V <sub>CE</sub> = 50V, I <sub>C</sub> = 35A, PW = 20μs
I <sub>CES</sub>	Collector-to-Emitter Leakage Current	—	1.0	35	μA	V <sub>GE</sub> = 0V, V <sub>CE</sub> = 1200V
		—	1200	—		V <sub>GE</sub> = 0V, V <sub>CE</sub> = 1200V, T <sub>J</sub> = 150°C
I <sub>GES</sub>	Gate-to-Emitter Leakage Current	—	—	±100	nA	V <sub>GE</sub> = ±30V
V <sub>F</sub>	Diode Forward Voltage Drop	—	2.5	3.3	V	I <sub>F</sub> = 8A
		—	2.4	—		I <sub>F</sub> = 8A, T <sub>J</sub> = 150°C

**Switching Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)**

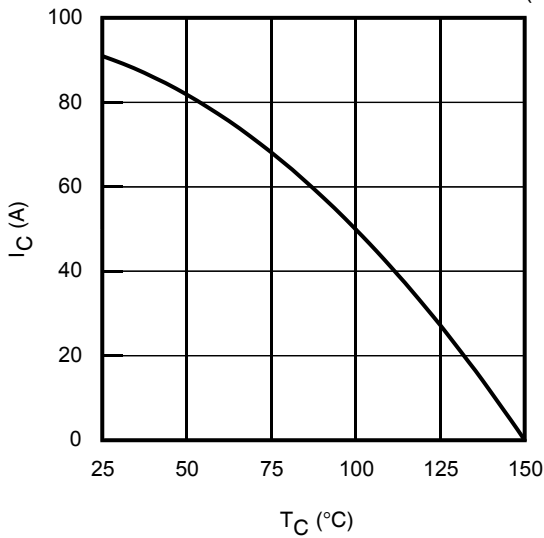
	Parameter	Min.	Typ.	Max④	Units	Conditions
Q <sub>g</sub>	Total Gate Charge (turn-on)	—	200	300	nC	I <sub>C</sub> = 35A V <sub>GE</sub> = 15V V <sub>CC</sub> = 600V
Q <sub>ge</sub>	Gate-to-Emitter Charge (turn-on)	—	40	60		
Q <sub>gc</sub>	Gate-to-Collector Charge (turn-on)	—	90	135		
E <sub>on</sub>	Turn-On Switching Loss	—	2.6	3.5	mJ	I <sub>C</sub> = 35A, V <sub>CC</sub> = 600V, V <sub>GE</sub> = 15V R <sub>G</sub> = 5Ω, T <sub>J</sub> = 25°C
E <sub>off</sub>	Turn-Off Switching Loss	—	1.6	2.5		
E <sub>total</sub>	Total Switching Loss	—	4.2	6.0		
t <sub>d(on)</sub>	Turn-On delay time	—	90	105	ns	Energy losses include tail & diode reverse recovery ⑤⑥
t <sub>r</sub>	Rise time	—	60	80		
t <sub>d(off)</sub>	Turn-Off delay time	—	340	390		
t <sub>f</sub>	Fall time	—	90	110		
E <sub>on</sub>	Turn-On Switching Loss	—	3.5	—	mJ	I <sub>C</sub> = 35A, V <sub>CC</sub> = 600V, V <sub>GE</sub> = 15V R <sub>G</sub> = 5Ω, T <sub>J</sub> = 150°C
E <sub>off</sub>	Turn-Off Switching Loss	—	2.8	—		
E <sub>total</sub>	Total Switching Loss	—	6.3	—		
t <sub>d(on)</sub>	Turn-On delay time	—	70	—	ns	Energy losses include tail & diode reverse recovery ⑤⑥
t <sub>r</sub>	Rise time	—	60	—		
t <sub>d(off)</sub>	Turn-Off delay time	—	350	—		
t <sub>f</sub>	Fall time	—	250	—		
C <sub>ies</sub>	Input Capacitance	—	4300	—	pF	V <sub>GE</sub> = 0V V <sub>CC</sub> = 30V f = 1.0Mhz
C <sub>oes</sub>	Output Capacitance	—	190	—		
C <sub>res</sub>	Reverse Transfer Capacitance	—	100	—		
RBSOA	Reverse Bias Safe Operating Area	FULL SQUARE				T <sub>J</sub> = 150°C, I <sub>C</sub> = 160A V <sub>CC</sub> = 960V, V <sub>p</sub> ≤ 1200V V <sub>GE</sub> = +20V to 0V
SCSOA	Short Circuit Safe Operating Area	10	—	—	μs	T <sub>J</sub> = 150°C, V <sub>CC</sub> = 600V, V <sub>p</sub> ≤ 1200V V <sub>GE</sub> = +15V to 0V
E <sub>rec</sub>	Reverse Recovery Energy of the Diode	—	190	—	μJ	T <sub>J</sub> = 150°C
t <sub>rr</sub>	Diode Reverse Recovery Time	—	130	—	ns	V <sub>CC</sub> = 600V, I <sub>F</sub> = 8A
I <sub>rr</sub>	Peak Reverse Recovery Current	—	13	—	A	V <sub>GE</sub> = 15V, R <sub>g</sub> = 5Ω

**Notes:**

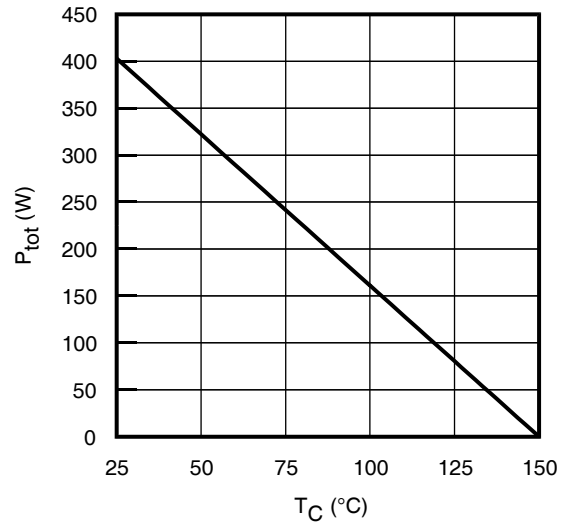
- ① V<sub>CC</sub> = 80% (V<sub>CES</sub>), V<sub>GE</sub> = 20V
- ② R<sub>θ</sub> is measured at T<sub>J</sub> of approximately 90°C.
- ③ Refer to AN-1086 for guidelines for measuring V<sub>(BR)CES</sub> safely.
- ④ Maximum limits are based on statistical sample size characterization.
- ⑤ Pulse width limited by max. junction temperature.
- ⑥ Values influenced by parasitic L and C in measurement.



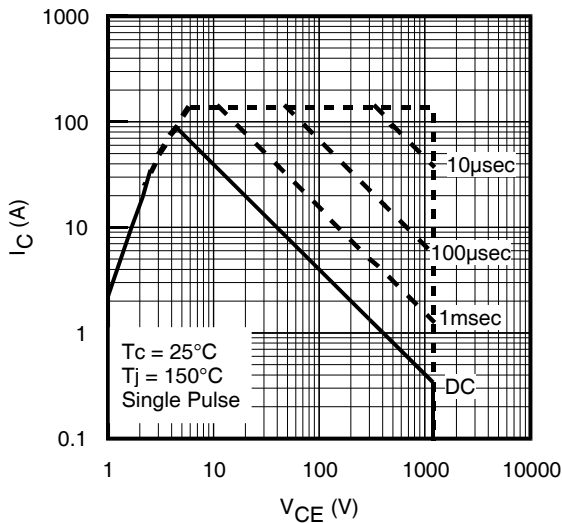
**Fig. 1 - Typical Load Current vs. Frequency**  
(Load Current =  $I_{RMS}$  of fundamental)



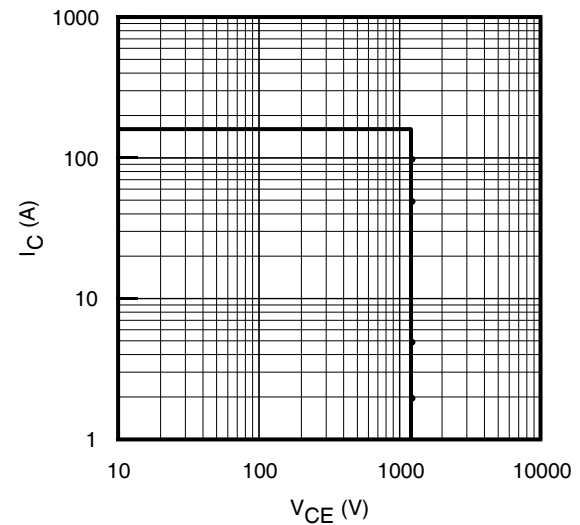
**Fig. 2 - Maximum DC Collector Current vs. Case Temperature**



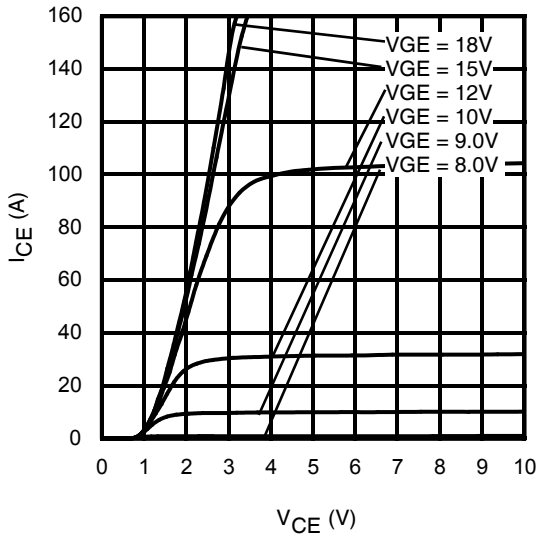
**Fig. 3 - Power Dissipation vs. Case Temperature**



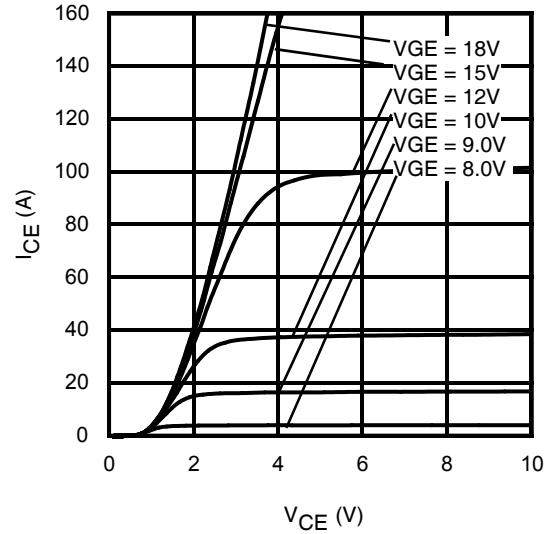
**Fig. 4 - Forward SOA**  
 $T_C = 25^\circ\text{C}$ ,  $T_J \leq 150^\circ\text{C}$ ,  $V_{GE} = 15\text{V}$



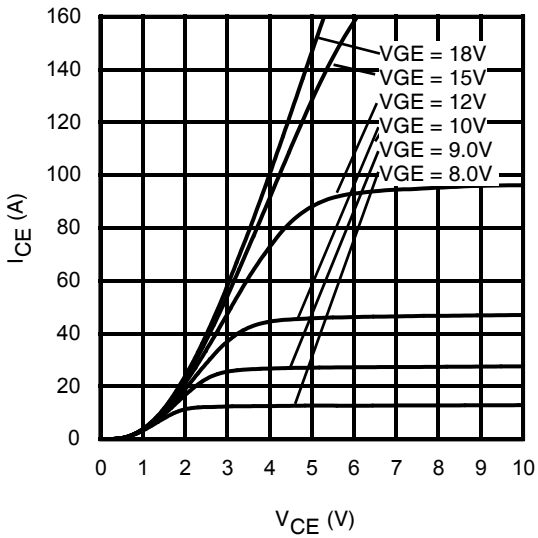
**Fig. 5- Reverse Bias SOA**  
 $T_J = 150^\circ\text{C}$ ;  $V_{GE} = 20\text{V}$



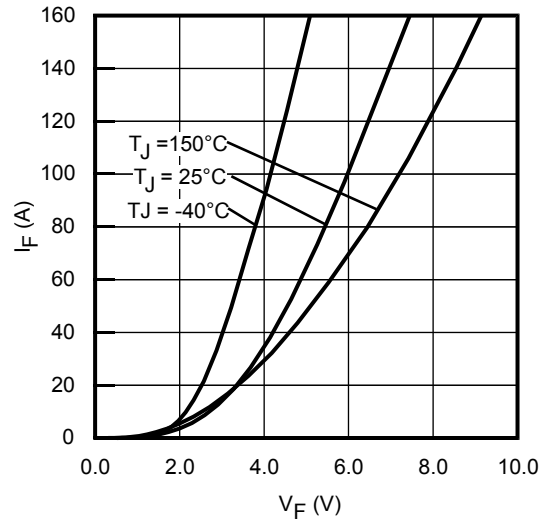
**Fig. 6** - Typ. IGBT Output Characteristics  
 $T_J = -40^\circ\text{C}$ ;  $t_p = 20\mu\text{s}$



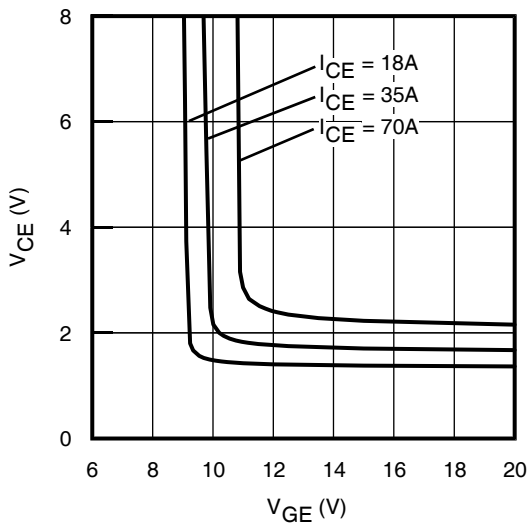
**Fig. 7** - Typ. IGBT Output Characteristics  
 $T_J = 25^\circ\text{C}$ ;  $t_p = 20\mu\text{s}$



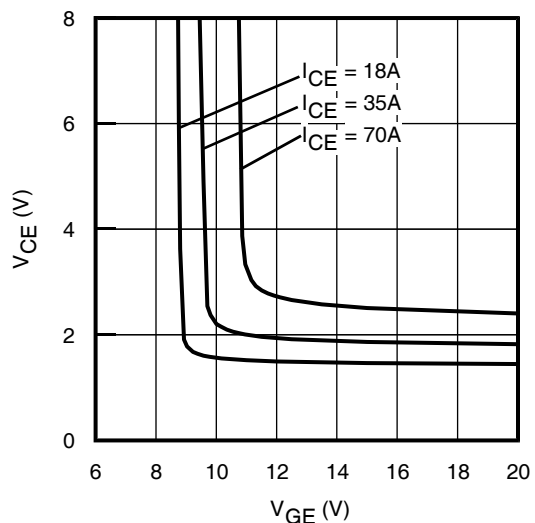
**Fig. 8** - Typ. IGBT Output Characteristics  
 $T_J = 150^\circ\text{C}$ ;  $t_p = 20\mu\text{s}$



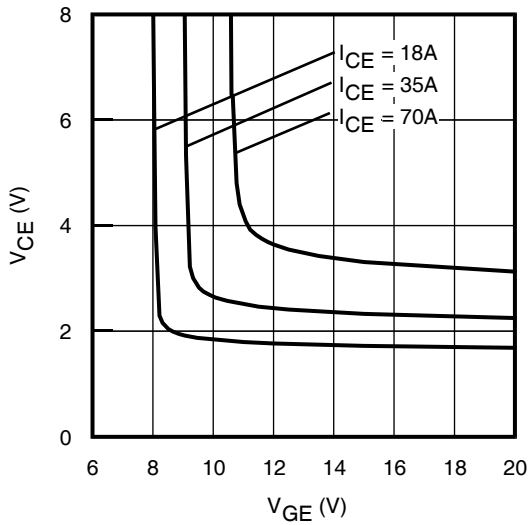
**Fig. 9** - Typ. Diode Forward Characteristics  
 $t_p = 20\mu\text{s}$



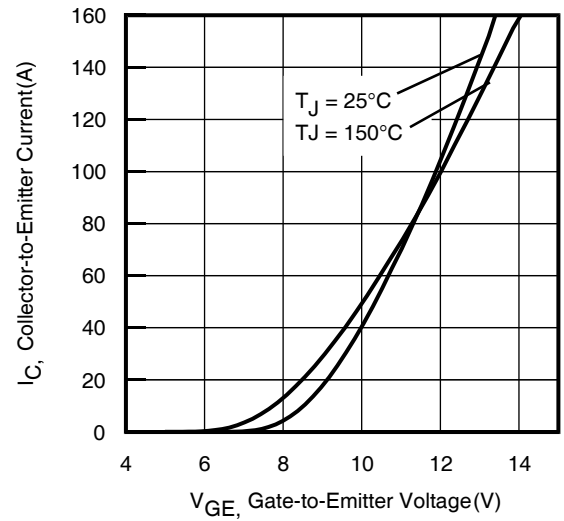
**Fig. 10** - Typical  $V_{CE}$  vs.  $V_{GE}$   
 $T_J = -40^\circ\text{C}$



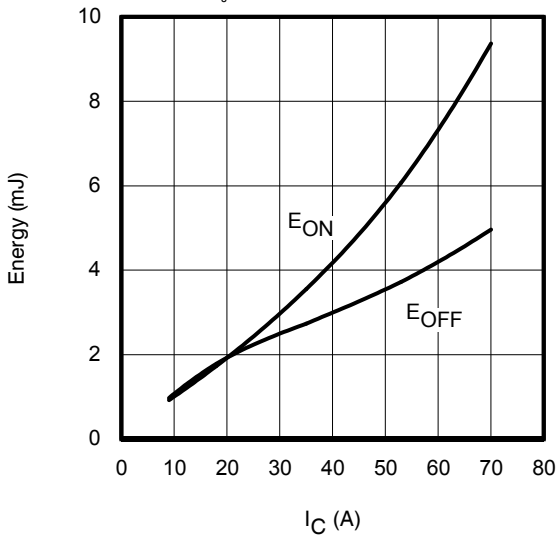
**Fig. 11** - Typical  $V_{CE}$  vs.  $V_{GE}$   
 $T_J = 25^\circ\text{C}$



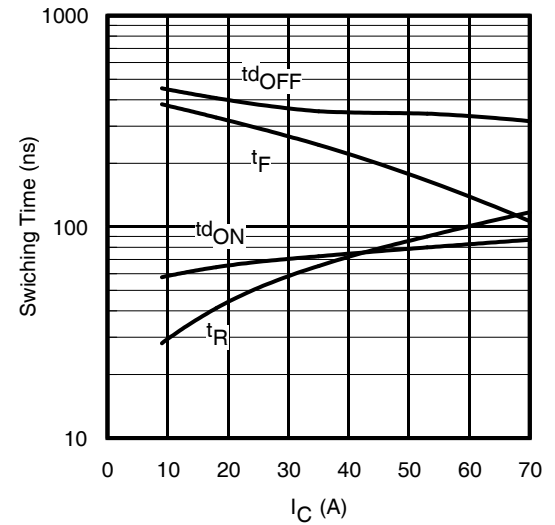
**Fig. 12** - Typical  $V_{CE}$  vs.  $V_{GE}$   
 $T_J = 150^\circ\text{C}$



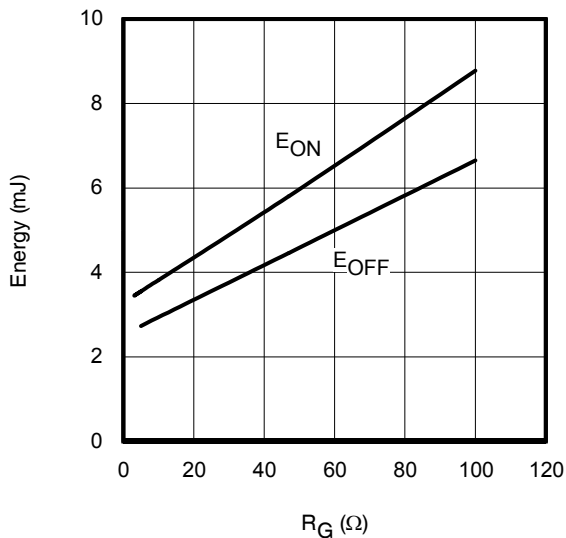
**Fig. 13** - Typ. Transfer Characteristics  
 $V_{CE} = 50\text{V}$ ;  $t_p = 20\mu\text{s}$



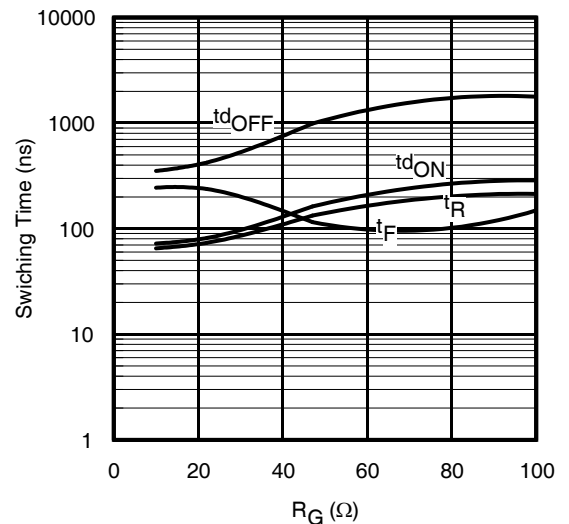
**Fig. 14** - Typ. Energy Loss vs.  $I_C$   
 $T_J = 150^\circ\text{C}$ ;  $V_{CE} = 600\text{V}$ ,  $R_G = 5\Omega$ ;  $V_{GE} = 15\text{V}$



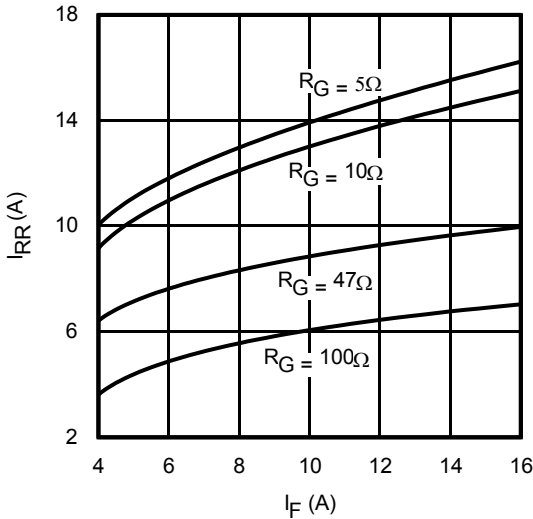
**Fig. 15** - Typ. Switching Time vs.  $I_C$   
 $T_J = 150^\circ\text{C}$ ;  $V_{CE} = 600\text{V}$ ,  $R_G = 5\Omega$ ;  $V_{GE} = 15\text{V}$



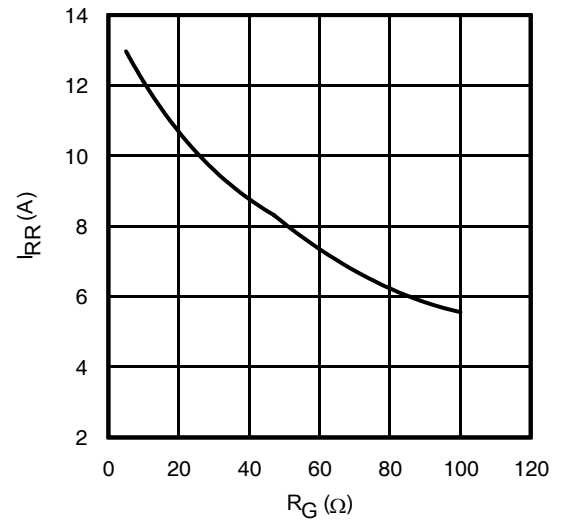
**Fig. 16** - Typ. Energy Loss vs.  $R_G$   
 $T_J = 150^\circ\text{C}$ ;  $V_{CE} = 600\text{V}$ ,  $I_{CE} = 35\text{A}$ ;  $V_{GE} = 15\text{V}$



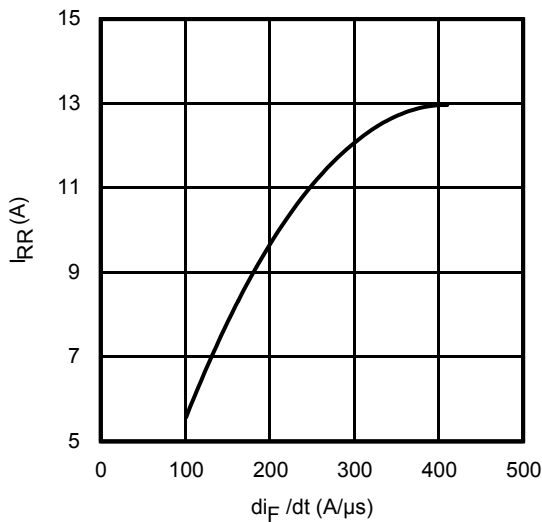
**Fig. 17** - Typ. Switching Time vs.  $R_G$   
 $T_J = 150^\circ\text{C}$ ;  $V_{CE} = 600\text{V}$ ,  $I_{CE} = 35\text{A}$ ;  $V_{GE} = 15\text{V}$



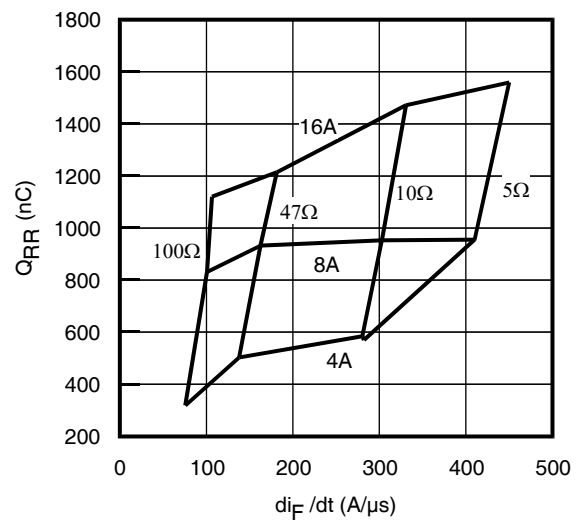
**Fig. 18** - Typ. Diode  $I_{RR}$  vs.  $I_F$   
 $T_J = 150^\circ\text{C}$



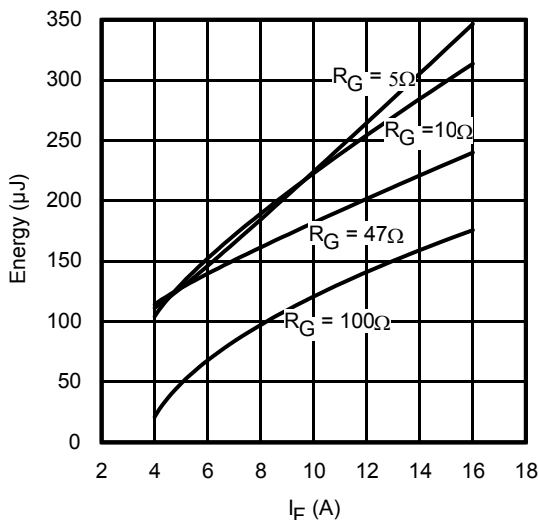
**Fig. 19** - Typ. Diode  $I_{RR}$  vs.  $R_G$



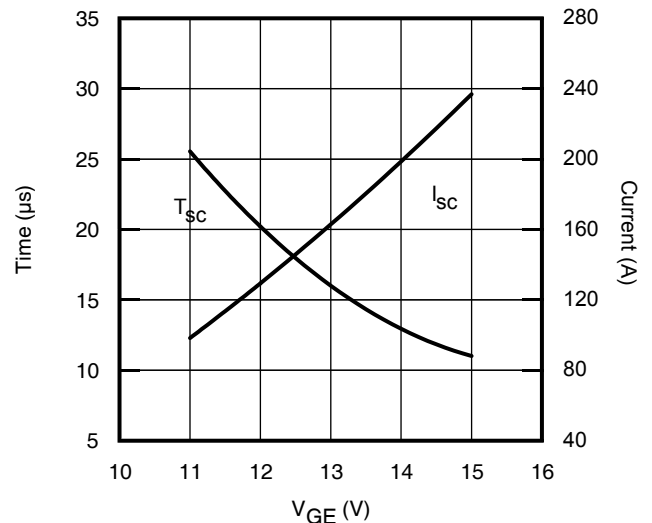
**Fig. 20** - Typ. Diode  $I_{RR}$  vs.  $di_F/dt$   
 $V_{CC} = 600\text{V}$ ;  $V_{GE} = 15\text{V}$ ;  $I_F = 8\text{A}$ ;  $T_J = 150^\circ\text{C}$



**Fig. 21** - Typ. Diode  $Q_{RR}$  vs.  $di_F/dt$   
 $V_{CC} = 600\text{V}$ ;  $V_{GE} = 15\text{V}$ ;  $T_J = 150^\circ\text{C}$



**Fig. 22** - Typ. Diode  $E_{RR}$  vs.  $I_F$   
 $T_J = 150^\circ\text{C}$



**Fig. 23** -  $V_{CE}$  vs. Short Circuit Time  
 $V_{CC} = 600\text{V}$ ;  $T_C = 150^\circ\text{C}$

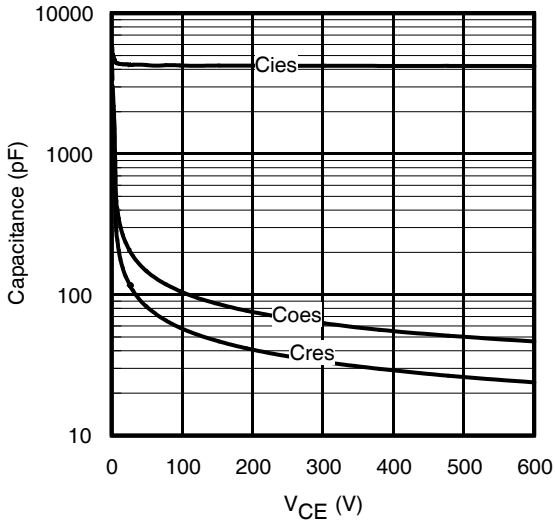


Fig. 24 - Typ. Capacitance vs.  $V_{CE}$

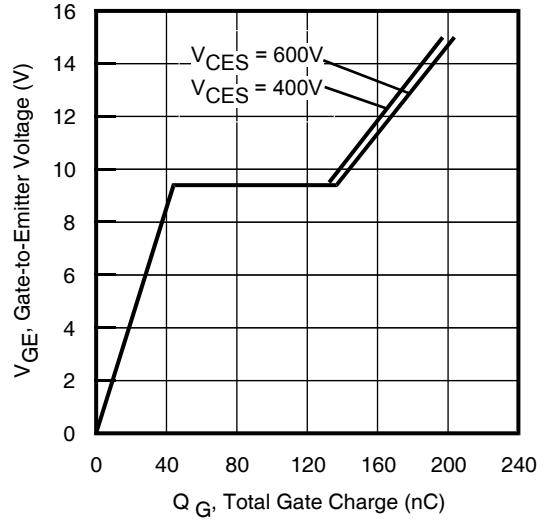


Fig. 25 - Typical Gate Charge vs.  $V_{GE}$   
 $I_{GE} = 35A$

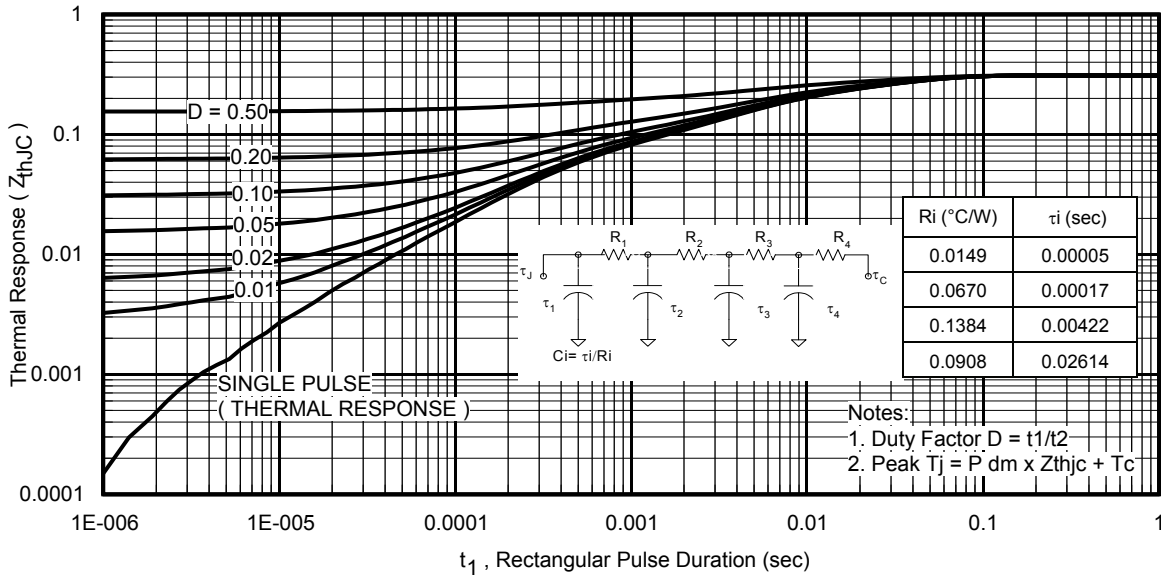


Fig. 26 Maximum Transient Thermal Impedance, Junction-to-Case (IGBT)

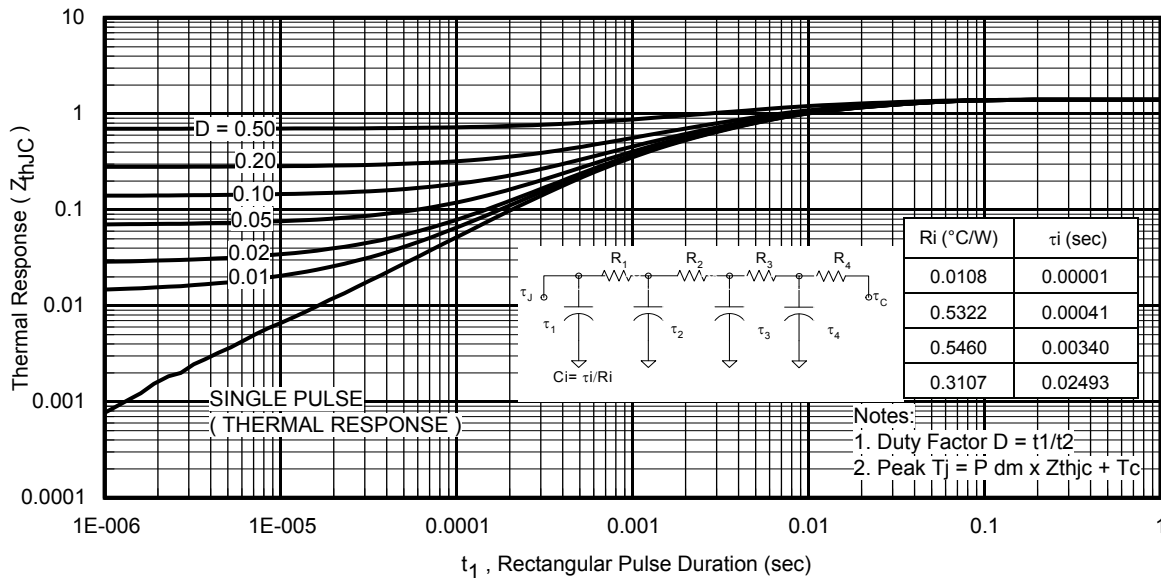
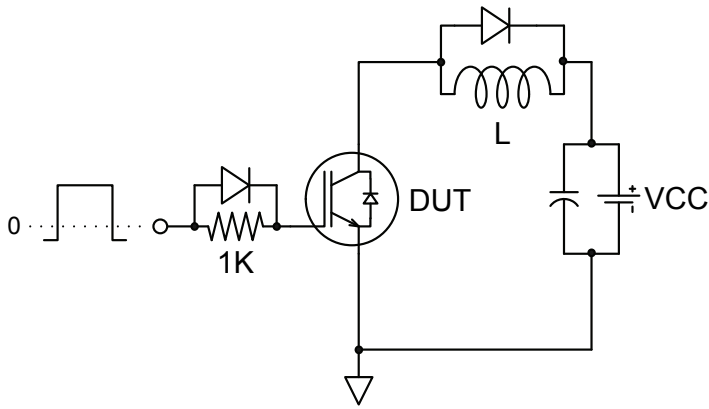
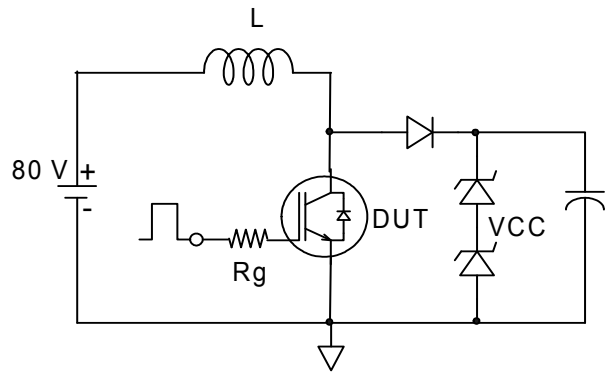
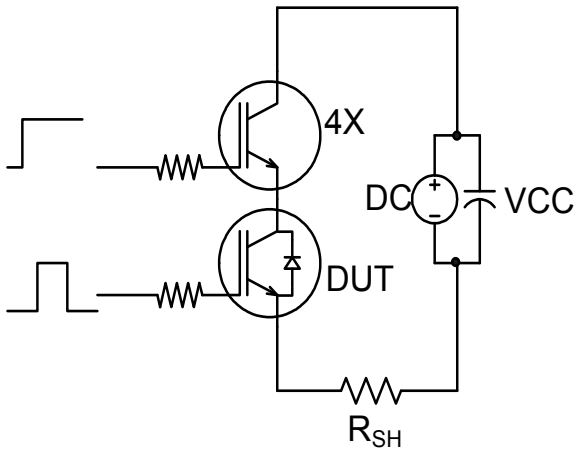
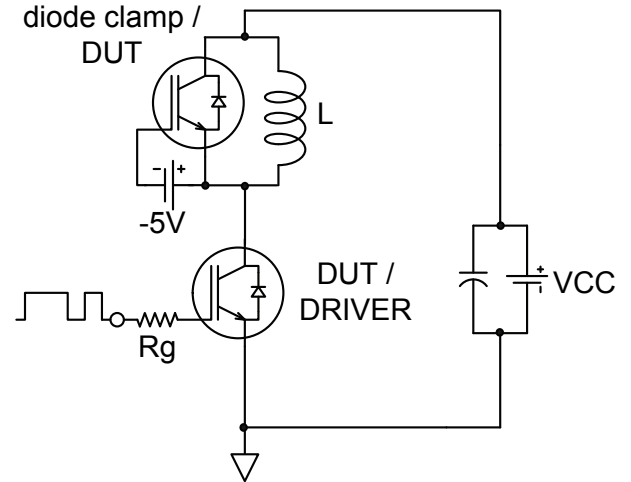
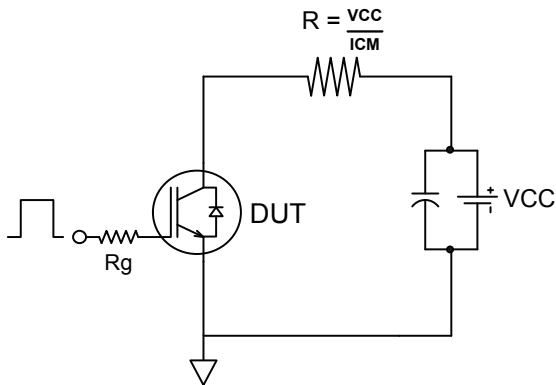
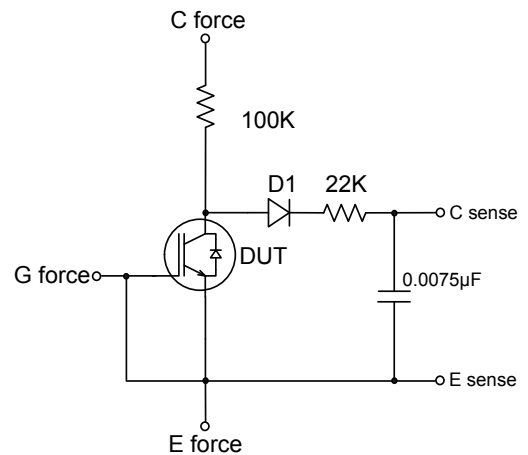
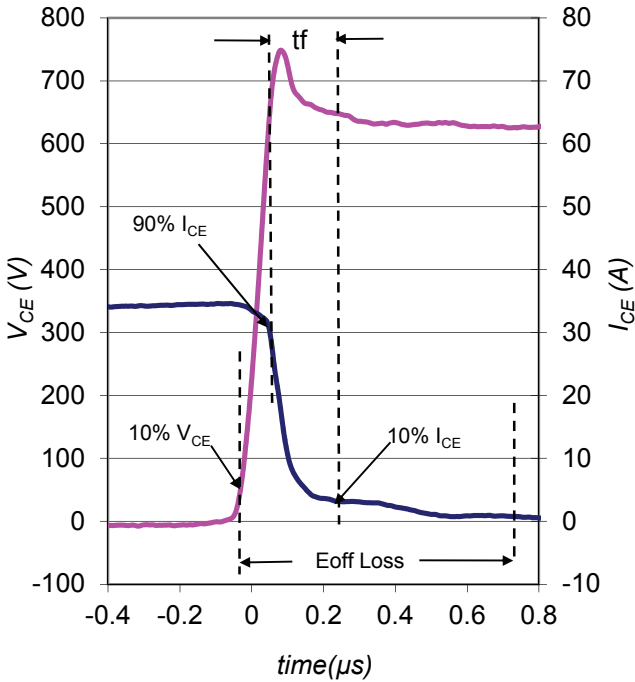


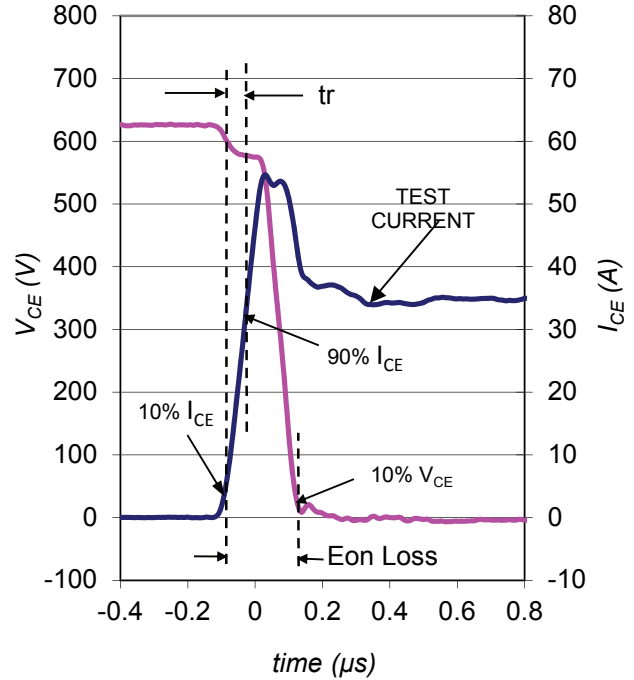
Fig. 27 Maximum Transient Thermal Impedance, Junction-to-Case (DIODE)


**Fig.C.T.1 - Gate Charge Circuit (turn-off)**

**Fig.C.T.2 - RBSOA Circuit**

**Fig.C.T.3 - S.C. SOA Circuit**

**Fig.C.T.4 - Switching Loss Circuit**

**Fig.C.T.5 - Resistive Load Circuit**

**Fig.C.T.6 - BVCES Filter Circuit**

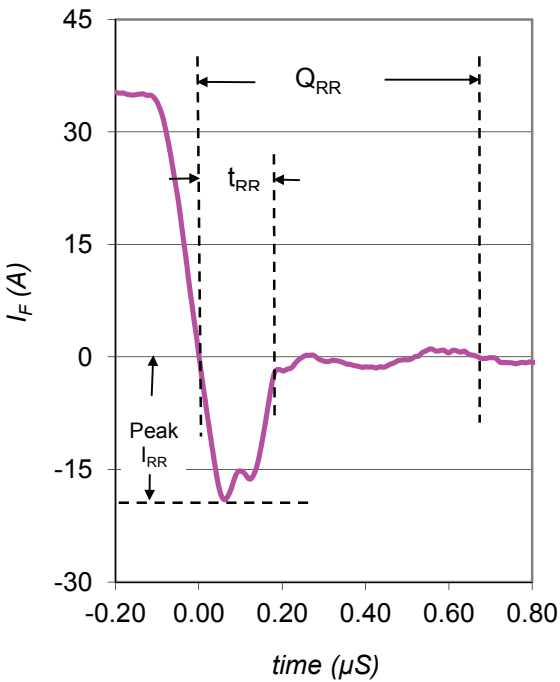




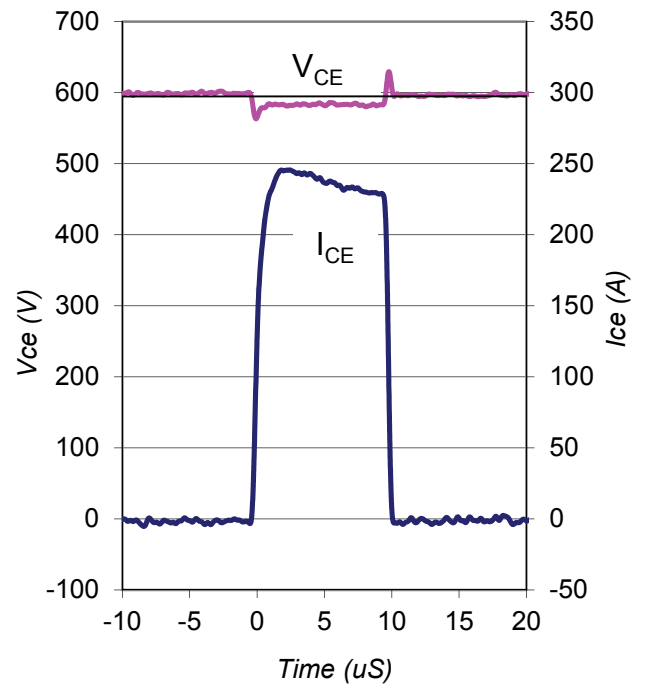
**Fig. WF1** - Typ. Turn-off Loss Waveform  
@  $T_J = 150^\circ\text{C}$  using Fig. CT.4



**Fig. WF2** - Typ. Turn-on Loss Waveform  
@  $T_J = 150^\circ\text{C}$  using Fig. CT.4



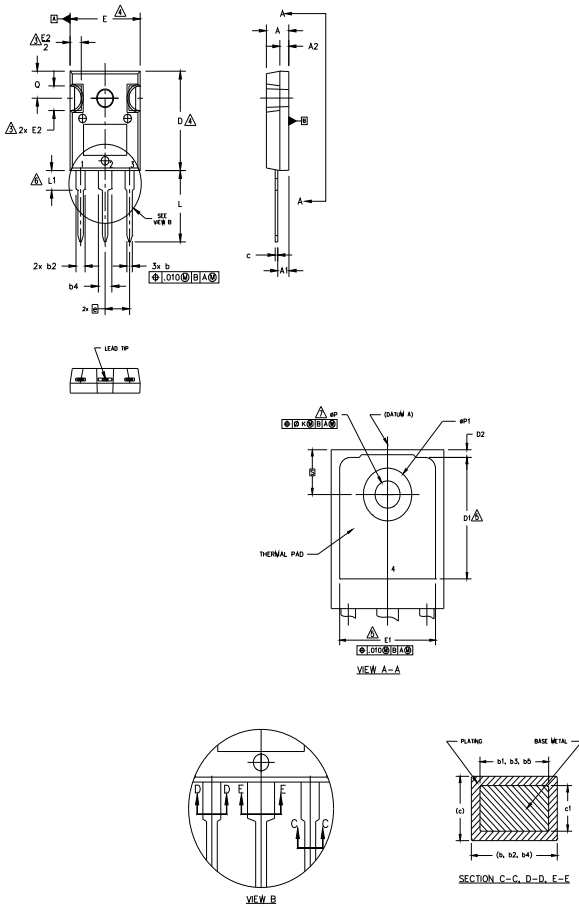
**Fig. WF3** - Typ. Diode Recovery Waveform  
@  $T_J = 150^\circ\text{C}$  using Fig. CT.4



**Fig. WF4** - Typ. S.C. Waveform  
@  $T_J = 150^\circ\text{C}$  using Fig. CT.3

# TO-247AC Package Outline

Dimensions are shown in millimeters (inches)



- NOTES:
1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M 1994.
  2. DIMENSIONS ARE SHOWN IN INCHES.
  3. CONTOUR OF SLOT OPTIONAL.
  4. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
  5. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS D1 & E1.
  6. LEAD FINISH UNCONTROLLED IN L1.
  7. ØP TO HAVE A MAXIMUM DRAFT ANGLE OF 1.5 ° TO THE TOP OF THE PART WITH A MAXIMUM HOLE DIAMETER OF .154 INCH.
  8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-247AC .

SYMBOL	DIMENSIONS				NOTES
	INCHES		MILLIMETERS		
	MIN.	MAX.	MIN.	MAX.	
A	.183	.209	4.65	5.31	
A1	.087	.102	2.21	2.59	
A2	.059	.098	1.50	2.49	
b	.039	.055	0.99	1.40	
b1	.039	.053	0.99	1.35	
b2	.065	.094	1.65	2.39	
b3	.065	.092	1.65	2.34	
b4	.102	.135	2.59	3.43	
b5	.102	.133	2.59	3.38	
c	.015	.035	0.38	0.89	
c1	.015	.033	0.38	0.84	
D	.776	.815	19.71	20.70	4
D1	.515	-	13.08	-	5
D2	.020	.053	0.51	1.35	4
E	.602	.625	15.29	15.87	4
E1	.530	-	13.46	-	
E2	.178	.216	4.52	5.49	
e	.215 BSC		5.46 BSC		
Øk	.010		0.25		
L	.559	.634	14.20	16.10	
L1	.146	.169	3.71	4.29	
ØP	.140	.144	3.56	3.66	
ØP1	-	.291	-	7.39	
Q	.209	.224	5.31	5.69	
S	.217 BSC		5.51 BSC		

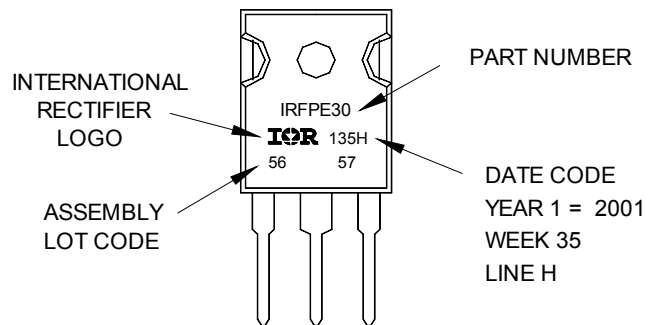
- LEAD ASSIGNMENTS**
- HEXFET**
- 1.- GATE
  - 2.- DRAIN
  - 3.- SOURCE
  - 4.- DRAIN
- IGBTs, CoPACK**
- 1.- GATE
  - 2.- COLLECTOR
  - 3.- EMITTER
  - 4.- COLLECTOR
- DIODES**
- 1.- ANODE/OPEN
  - 2.- CATHODE
  - 3.- ANODE

## TO-247AC Part Marking Information

Notes: This part marking information applies to devices produced after 02/26/2001

EXAMPLE: THIS IS AN IRFPE30 WITH ASSEMBLY LOT CODE 5657 ASSEMBLED ON WW 35, 2001 IN THE ASSEMBLY LINE "H"

Note: "P" in assembly line position indicates "Lead-Free"

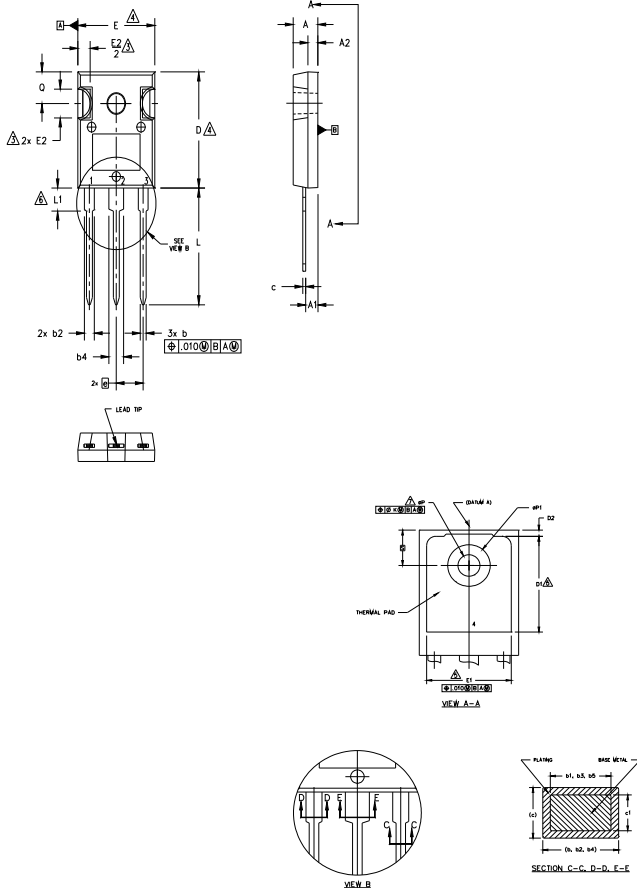


TO-247AC package is not recommended for Surface Mount Application.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

## TO-247AD Package Outline

Dimensions are shown in millimeters (inches)



**NOTES:**

1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M 1994.
2. DIMENSIONS ARE SHOWN IN INCHES.
3. CONTOUR OF SLOT OPTIONAL.
4. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS D1 & E1.
6. LEAD FINISH UNCONTROLLED IN L1.
7.  $\phi P$  TO HAVE A MAXIMUM DRAFT ANGLE OF 1.5 ° TO THE TOP OF THE PART WITH A MAXIMUM HOLE DIAMETER OF .154 INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-247AD.

SYMBOL	DIMENSIONS				NOTES
	INCHES		MILLIMETERS		
	MIN.	MAX.	MIN.	MAX.	
A	.183	.209	4.65	5.31	
A1	.087	.102	2.21	2.59	
A2	.069	.098	1.50	2.49	
b	.039	.055	0.99	1.40	
b1	.039	.053	0.99	1.35	
b2	.065	.094	1.65	2.39	
b3	.065	.092	1.65	2.34	
b4	.102	.135	2.59	3.43	
b5	.102	.133	2.59	3.38	
c	.015	.035	0.38	0.89	
c1	.015	.033	0.38	0.84	
D	.776	.815	19.71	20.70	4
D1	.515	-	13.08	-	5
D2	.020	.053	0.51	1.35	
E	.602	.625	15.29	15.87	4
E1	.530	-	13.46	-	
E2	.178	.216	4.52	5.49	
e	.215 BSC		5.46 BSC		
$\phi k$	.010		0.25		
L	.780	.827	19.57	21.00	
L1	.146	.169	3.71	4.29	
$\phi P$	.140	.144	3.56	3.66	
$\phi P1$	-	.291	-	7.39	
Q	.209	.224	5.31	5.69	
S	.217 BSC		5.51 BSC		

**LEAD ASSIGNMENTS**

**HEXFET**

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

**IGBTs, CoPACK**

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

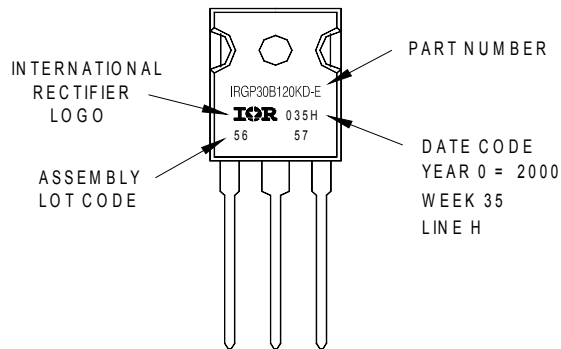
**DIODES**

- 1.- ANODE/OPEN
- 2.- CATHODE
- 3.- ANODE

## TO-247AD Part Marking Information

EXAMPLE: THIS IS AN IRGP30B120KD-E  
WITH ASSEMBLY  
LOT CODE 5657  
ASSEMBLED ON WW 35, 2000  
IN THE ASSEMBLY LINE "H"

Note: "P" in assembly line position  
indicates "Lead-Free"



TO-247AD package is not recommended for Surface Mount Application.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

**Qualification Information<sup>†</sup>**

<b>Qualification Level</b>	Industrial (per JEDEC JESD47F) <sup>††</sup>	
<b>Moisture Sensitivity Level</b>	TO-247AC	N/A
	TO-247AD	
<b>RoHS Compliant</b>	Yes	

† Qualification standards can be found at International Rectifier's web site: <http://www.irf.com/product-info/reliability/>

†† Applicable version of JEDEC standard at the time of product release.

**Revision History**

<b>Date</b>	<b>Comments</b>
3/12/14	Updated Package outline on page10

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