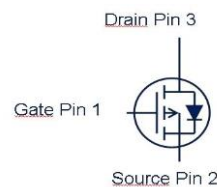
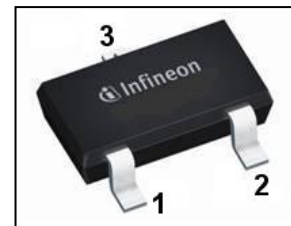


**SIPMOS<sup>®</sup> Small-Signal-Transistor**
**Features**

- P-Channel
- Enhancement mode / Logic level
- Avalanche rated
- Pb-free lead plating; RoHS compliant
- Footprint compatible to SOT23
- Qualified according to AEC Q101
- Halogen free according to IEC61249-2-21

**Product Summary**

$V_{DS}$	-250	V
$R_{DS(on),max}$	11	$\Omega$
$I_D$	-0.14	A


**PG-SC59**


Type	Package	Tape and Reel Information	Marking	Halogen-free	Packing
BSR92P	PG-SC59	H6327 = 3000 pcs. / reel	LD	Yes	Non dry

**Maximum ratings, at  $T_j=25\text{ °C}$ , unless otherwise specified**

Parameter	Symbol	Conditions	Value	Unit
			steady state	
Continuous drain current	$I_D$	$T_A=25\text{ °C}$	-0.14	A
		$T_A=70\text{ °C}$	-0.11	
Pulsed drain current	$I_{D,pulse}$	$T_A=25\text{ °C}$	-0.56	
Avalanche energy, single pulse	$E_{AS}$	$I_D=-0.14\text{ A}$ , $R_{GS}=25\ \Omega$	24	mJ
Gate source voltage	$V_{GS}$		$\pm 20$	V
Power dissipation	$P_{tot}$	$T_C=25\text{ °C}$	0.5	W
Operating and storage temperature	$T_j$ , $T_{stg}$		-55 ... 150	$^{\circ}\text{C}$
ESD class		JESD22-A114 (HBM)	1A (250V to 500V)	
Soldering temperature			260 $^{\circ}\text{C}$	
IEC climatic category; DIN IEC 68-1			55/150/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

**Thermal characteristics**

Thermal resistance, junction - ambient	$R_{thJA}$	minimal footprint, steady state	-	-	250	K/W
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**Electrical characteristics, at  $T_j=25\text{ °C}$ , unless otherwise specified**
**Static characteristics**

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}$ , $I_D=-250\text{ }\mu\text{A}$	-250	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$ , $I_D=-130\text{ }\mu\text{A}$	-2	-1.5	-1	
Zero gate voltage drain current	$I_{DSS}$	$V_{DS}=-250\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=25\text{ °C}$	-	-0.1	-1	$\mu\text{A}$
		$V_{DS}=-250\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=150\text{ °C}$	-	-10	-100	
Gate-source leakage current	$I_{GSS}$	$V_{GS}=-20\text{ V}$ , $V_{DS}=0\text{ V}$	-	-10	-100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=-2.8\text{ V}$ , $I_D=-0.025\text{ A}$	-	11	20	
		$V_{GS}=-4.5\text{ V}$ , $I_D=-0.13\text{ A}$	-	9	13	$\Omega$
		$V_{GS}=-10\text{ V}$ , $I_D=-0.14\text{ A}$	-	8	11	
Transconductance	$g_{fs}$	$ V_{DS} >2 I_D R_{DS(on)max}$ , $I_D=-0.11\text{ A}$	0.1	0.3	-	S

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

**Dynamic characteristics<sup>3)</sup>**

Input capacitance	$C_{iss}$	$V_{GS}=0\text{ V}, V_{DS}=-25\text{ V},$ $f=1\text{ MHz}$	-	82	109	pF
Output capacitance	$C_{oss}$		-	12	16	
Reverse transfer capacitance	$C_{rss}$		-	5	8	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=-125\text{ V},$ $V_{GS}=-10\text{ V},$ $I_D=-0.14\text{ A}, R_{G,ext}=6\ \Omega$	-	6.4	9.0	ns
Rise time	$t_r$		-	6.3	9.0	
Turn-off delay time	$t_{d(off)}$		-	75.0	112	
Fall time	$t_f$		-	71.0	163	

**Gate Charge Characteristics<sup>2), 3)</sup>**

Gate to source charge	$Q_{gs}$	$V_{DD}=-200\text{ V}, I_D=-$ $0.14\text{ A}, V_{GS}=0\text{ to }-$ $10\text{ V}$	-	-0.2	-0.3	nC
Gate to drain charge	$Q_{gd}$		-	-1.2	-1.8	
Gate charge total	$Q_g$		-	-3.6	-4.8	
Gate plateau voltage	$V_{plateau}$		-	-2.7	-	V

**Reverse Diode**

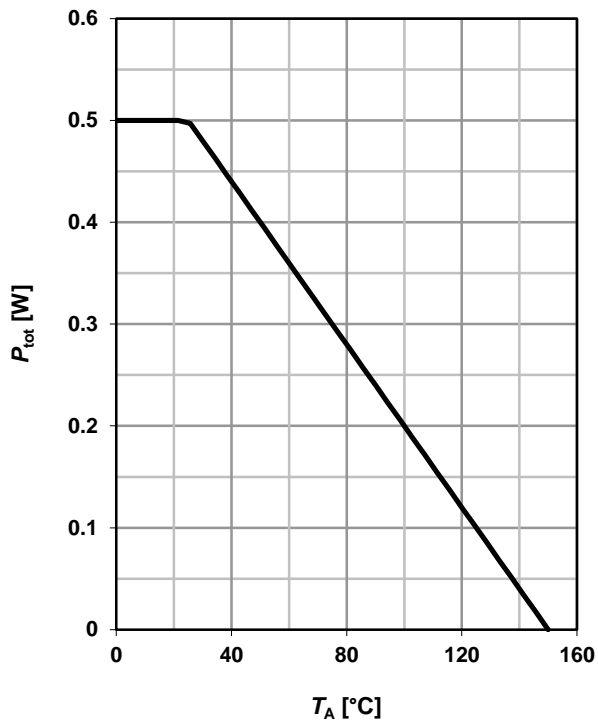
Diode continuous forward current	$I_S$	$T_C=25\text{ }^\circ\text{C}$	-	-	-0.14	A
Diode pulse current	$I_{S,pulse}$		-	-	-0.56	
Diode forward voltage	$V_{SD}$	$V_{GS}=0\text{ V}, I_F=0.14\text{ A},$ $T_j=25\text{ }^\circ\text{C}$	-	-0.8	-1.2	V
Reverse recovery time <sup>3)</sup>	$t_{rr}$	$V_R=125\text{ V}, I_F= I_S ,$ $di_F/dt=100\text{ A}/\mu\text{s}$	-	66	-	ns
Reverse recovery charge <sup>3)</sup>	$Q_{rr}$		-	125	-	nC

<sup>2)</sup> See figure 16 for gate charge parameter definition

<sup>3)</sup> Defined by design. Not subjected to production test

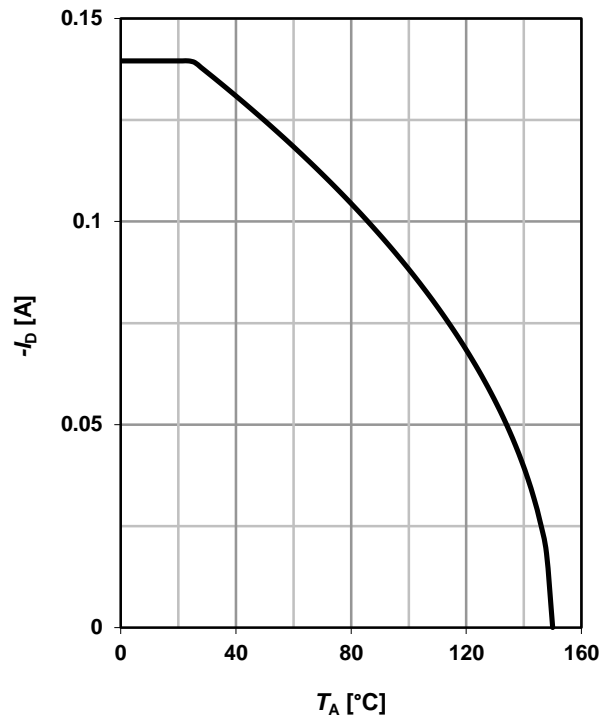
### 1 Power dissipation

$$P_{tot}=f(T_C)$$



### 2 Drain current

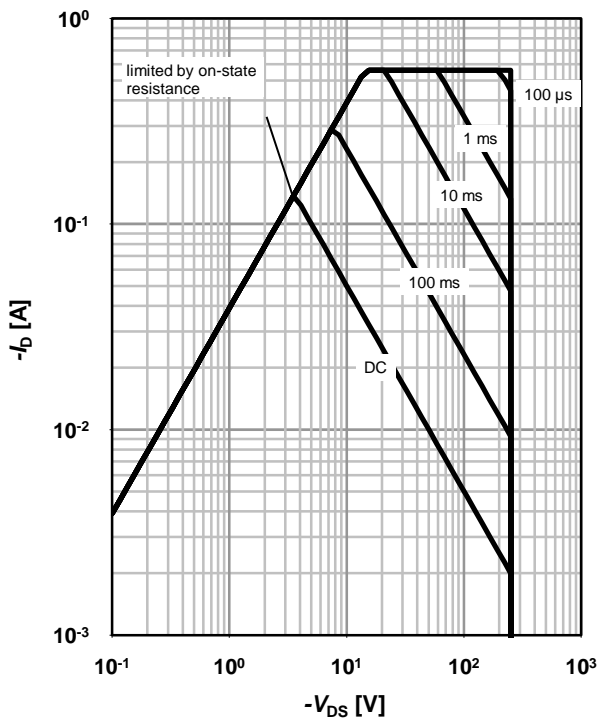
$$I_D=f(T_C); |V_{GS}|\geq 10\text{ V}$$



### 3 Safe operating area

$$I_D=f(V_{DS}); T_C=25\text{ °C}; D=0$$

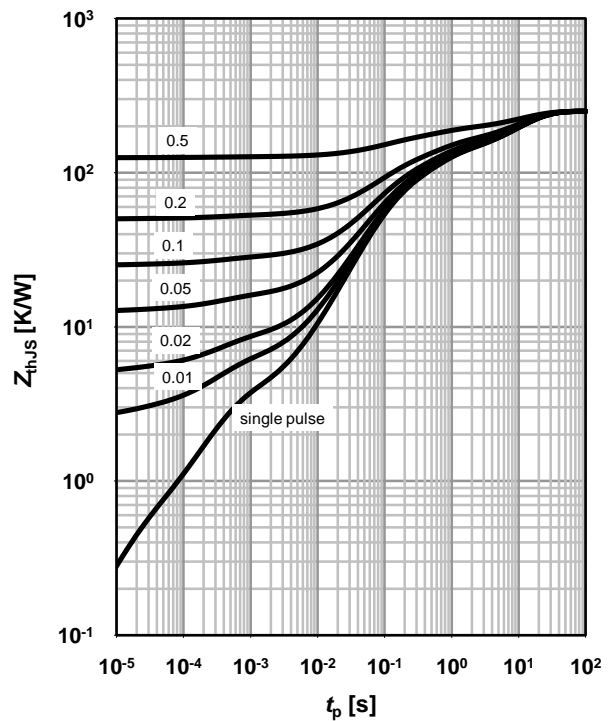
parameter:  $t_p$



### 4 Max. transient thermal impedance

$$Z_{thJC}=f(t_p)$$

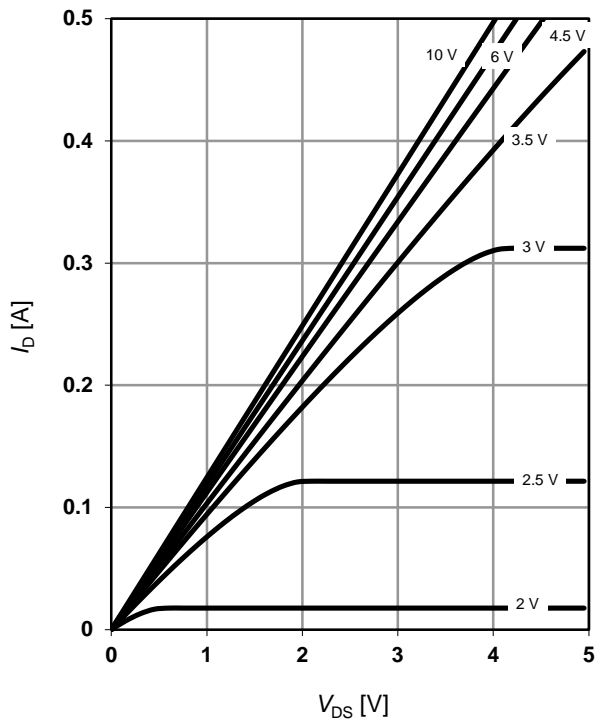
parameter:  $D=t_p/T$



**5 Typ. output characteristics**

$I_D = f(V_{DS}); T_j = 25\text{ °C}$

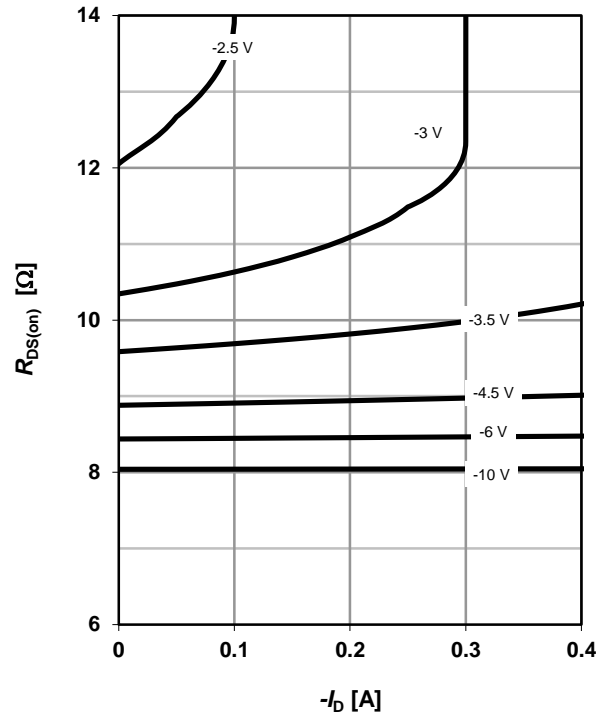
parameter:  $V_{GS}$



**6 Typ. drain-source on resistance**

$R_{DS(on)} = f(I_D); T_j = 25\text{ °C}$

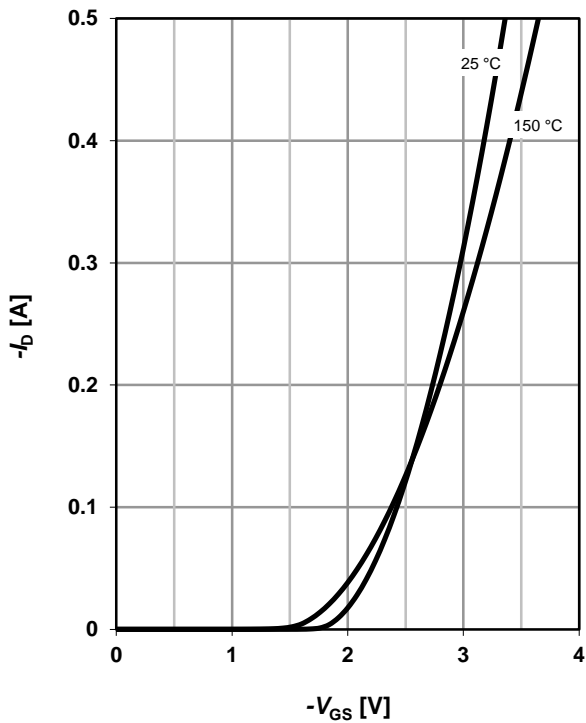
parameter:  $V_{GS}$



**7 Typ. transfer characteristics**

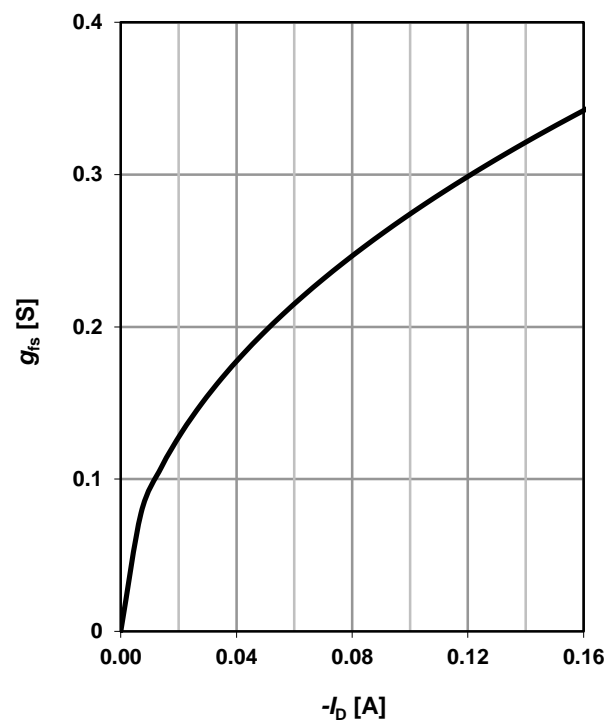
$I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)max}$

parameter:  $T_j$



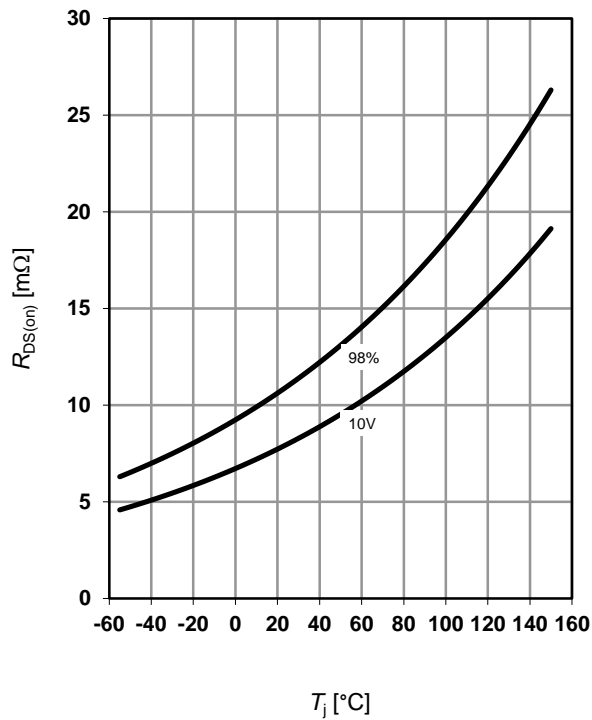
**8 Typ. forward transconductance**

$g_{fs} = f(I_D); T_j = 25\text{ °C}$



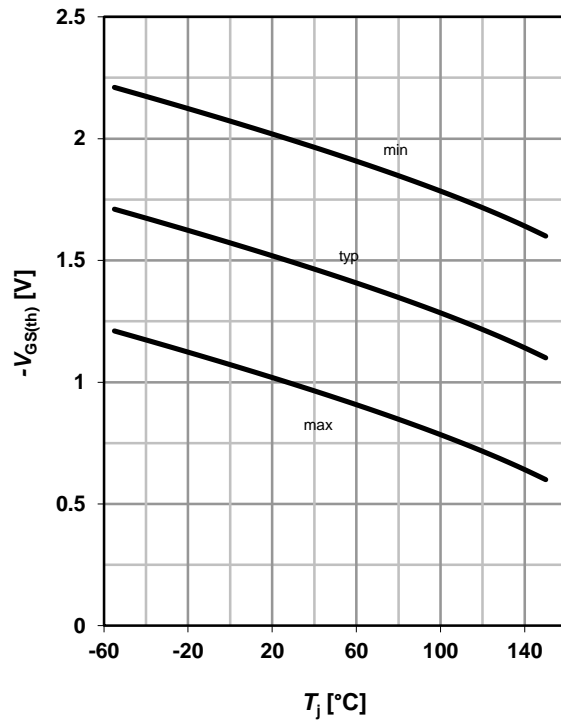
**9 Drain-source on-state resistance**

$R_{DS(on)}=f(T_j); I_D=-0.14\text{ A}; V_{GS}=-10\text{ V}$



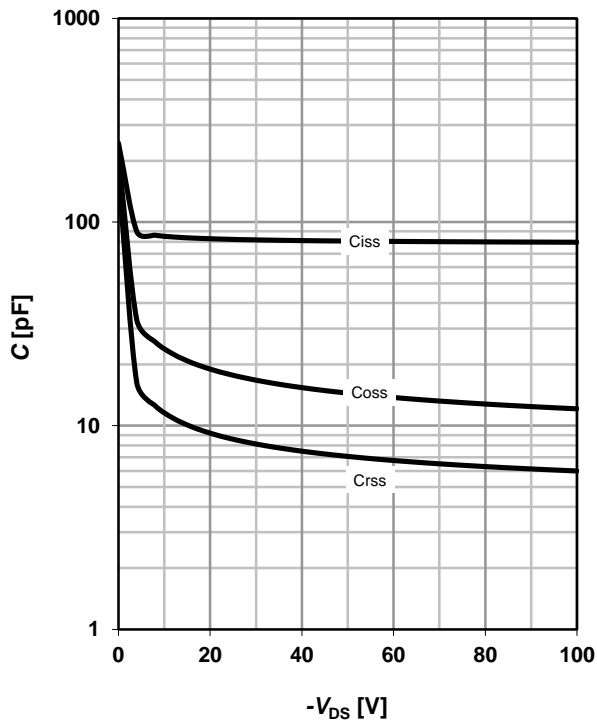
**10 Typ. gate threshold voltage**

$V_{GS(th)}=f(T_j); V_{GS}=V_{DS}; I_D=-130\text{ }\mu\text{A}$



**11 Typ. capacitances**

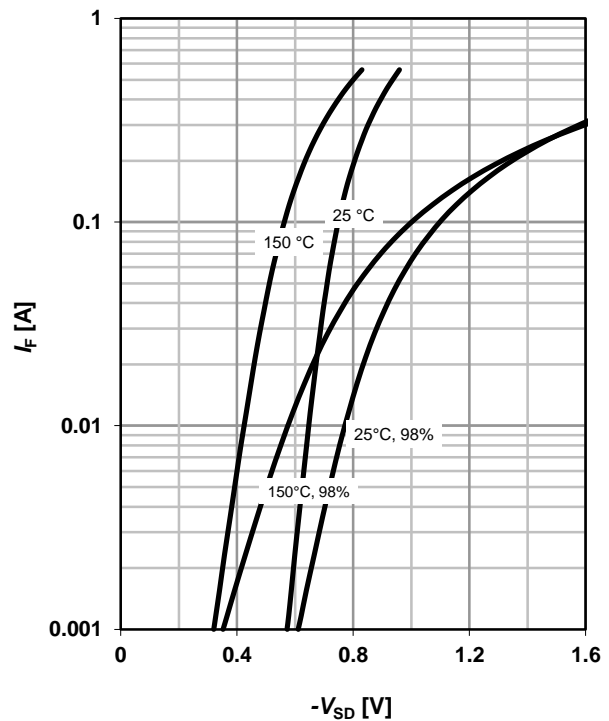
$C=f(V_{DS}); V_{GS}=0\text{ V}; f=1\text{ MHz}$



**12 Forward characteristics of reverse diode**

$I_F=f(V_{SD})$

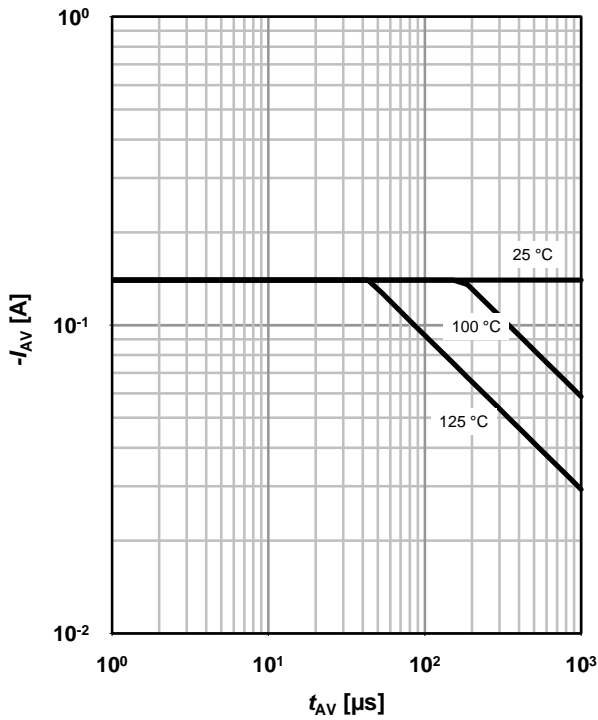
parameter:  $T_j$



**13 Avalanche characteristics**

$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$

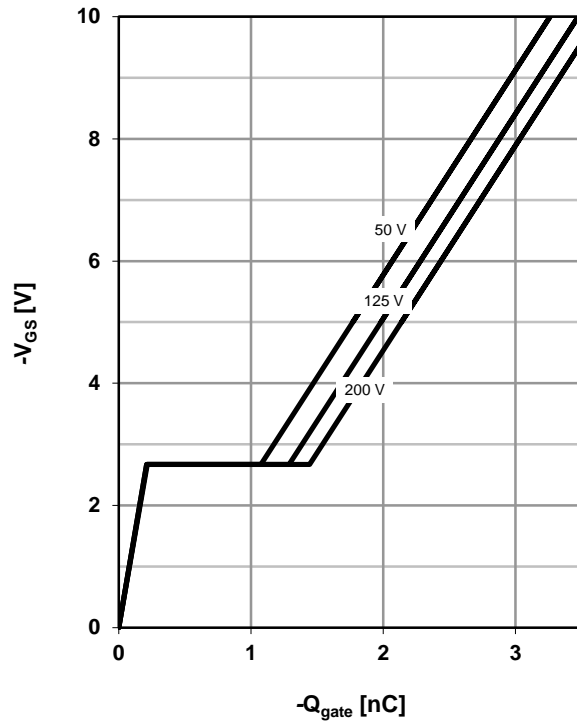
parameter:  $T_{j(\text{start})}$



**14 Typ. gate charge**

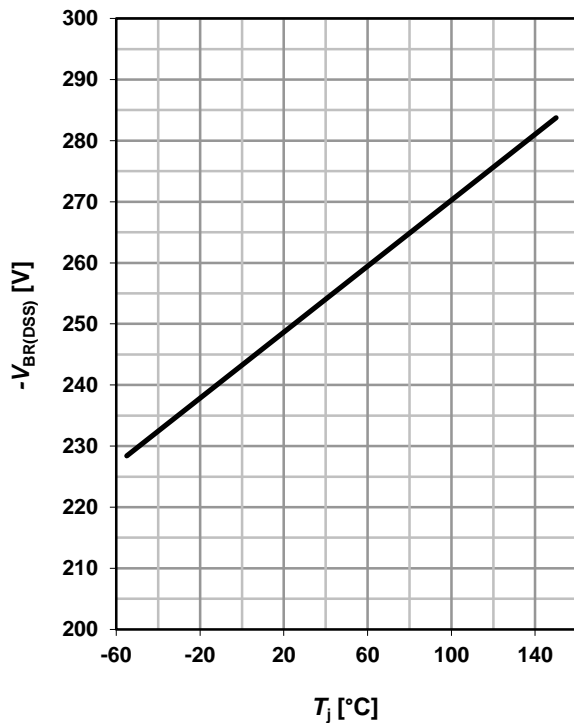
$V_{GS}=f(Q_{\text{gate}}); I_D=-0.14 \text{ A pulsed}$

parameter:  $V_{DD}$

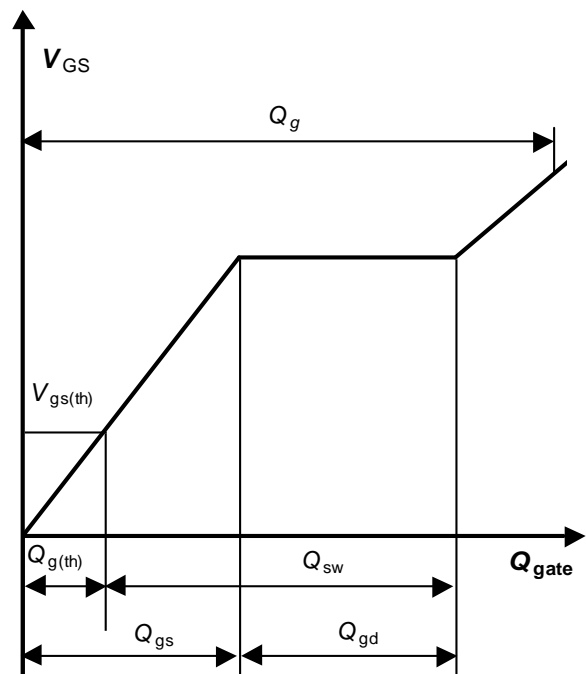


**15 Drain-source breakdown voltage**

$V_{BR(DSS)}=f(T_j); I_D=-250 \mu\text{A}$

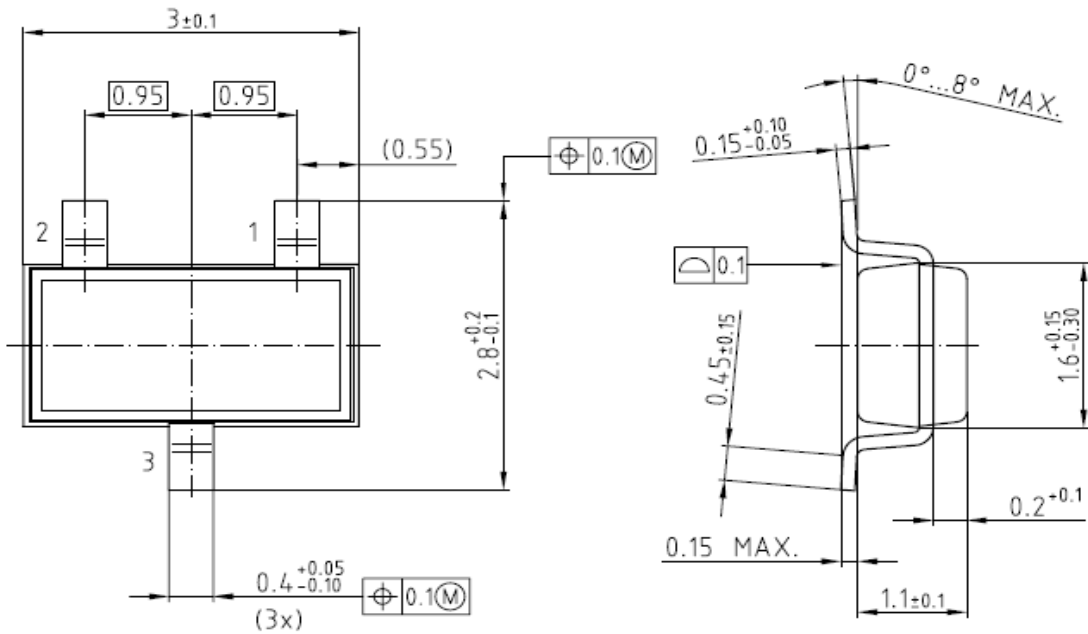


**16 Gate charge waveforms**

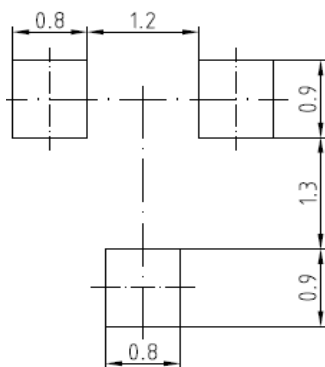


Package Outline

SC-59: Outline

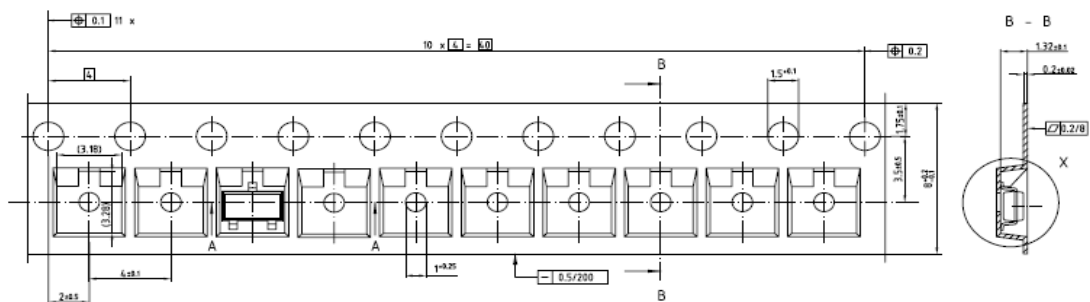


Footprint



Packaging

Tape



Dimensions in mm



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