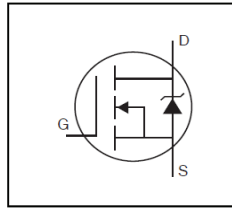


Features

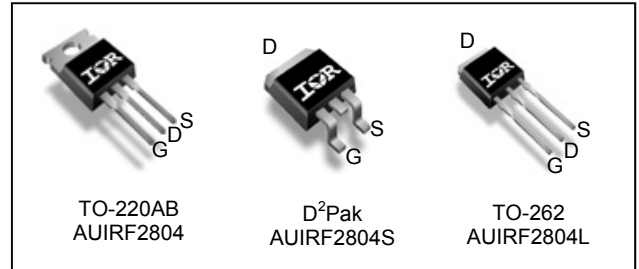
- Advanced Process Technology
- Ultra Low On-Resistance
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax
- Lead-Free, RoHS Compliant
- Automotive Qualified *



V_{DSS}	40V
$R_{DS(on)}$ typ.	1.5mΩ[Ⓢ]
max.	2.0mΩ[Ⓢ]
I_D (Silicon Limited)	270A[Ⓢ]
I_D (Package Limited)	195A

Description

Specifically designed for Automotive applications, this HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in Automotive applications and wide variety of other applications.



G	D	S
Gate	Drain	Source

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
AUIRF2804	TO-220	Tube	50	AUIRF2804
AUIRF2804L	TO-262	Tube	50	AUIRF2804L
AUIRF2804S	D²-Pak	Tube	50	AUIRF2804S
		Tape and Reel Left	800	AUIRF2804STRL

Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the specifications is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature (TA) is 25°C, unless otherwise specified.

Symbol	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ (Silicon Limited)	270 [Ⓢ]	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ (Silicon Limited)	190	
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ (Package Limited)	195	
I_{DM}	Pulsed Drain Current ^②	1080	
$P_D @ T_C = 25^\circ C$	Maximum Power Dissipation	300	W
	Linear Derating Factor	2.0	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy (Thermally Limited) ^③	540	mJ
$E_{AS} (tested)$	Single Pulse Avalanche Energy Tested Value ^⑥	1160	
I_{AR}	Avalanche Current ^②	See Fig.15,16, 12a, 12b	A
E_{AR}	Repetitive Avalanche Energy ^②		mJ
T_J	Operating Junction and Storage Temperature Range	-55 to + 175	°C
T_{STG}			
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ^④	—	0.50	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient	—	62	
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount, steady state) ^⑦	—	40	

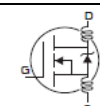
HEXFET® is a registered trademark of Infineon.

*Qualification standards can be found at www.infineon.com

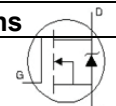
Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	40	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔV _{(BR)DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	0.031	—	V/°C	Reference to 25°C, I _D = 1mA
R _{DS(on)} SMD	Static Drain-to-Source On-Resistance	—	1.5	2.0	mΩ	V _{GS} = 10V, I _D = 75A ④⑩
R _{DS(on)} TO-220	Static Drain-to-Source On-Resistance	—	1.8	2.3	mΩ	V _{GS} = 10V, I _D = 75A ④⑩
V _{GS(th)}	Gate Threshold Voltage	2.0	—	4.0	V	V _{DS} = V _{GS} , I _D = 250μA
g _{fs}	Forward Trans conductance	130	—	—	S	V _{DS} = 10V, I _D = 75A⑩
I _{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	V _{DS} = 40V, V _{GS} = 0V
		—	—	250		V _{DS} = 40V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	200	nA	V _{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-200		V _{GS} = -20V

Dynamic Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

Q _g	Total Gate Charge	—	160	240	nC	I _D = 75A⑩
Q _{gs}	Gate-to-Source Charge	—	41	62		V _{DS} = 32V
Q _{gd}	Gate-to-Drain Charge	—	66	99		V _{GS} = 10V④
t _{d(on)}	Turn-On Delay Time	—	13	—	ns	V _{DD} = 20V
t _r	Rise Time	—	120	—		I _D = 75A⑩
t _{d(off)}	Turn-Off Delay Time	—	130	—		R _G = 2.5Ω
t _f	Fall Time	—	130	—		V _{GS} = 10V ④
L _D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L _S	Internal Source Inductance	—	7.5	—		
C _{iss}	Input Capacitance	—	6450	—	pF	V _{GS} = 0V
C _{oss}	Output Capacitance	—	1690	—		V _{DS} = 25V
C _{rss}	Reverse Transfer Capacitance	—	840	—		f = 1.0MHz, See Fig. 5
C _{oss}	Output Capacitance	—	5350	—		V _{GS} = 0V, V _{DS} = 1.0V f = 1.0MHz
C _{oss}	Output Capacitance	—	1520	—		V _{GS} = 0V, V _{DS} = 32V f = 1.0MHz
C _{oss eff.}	Effective Output Capacitance	—	2210	—		V _{GS} = 0V, V _{DS} = 0V to 32V ⑤

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	270①	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	1080		
V _{SD}	Diode Forward Voltage	—	—	1.3	V	T _J = 25°C, I _S = 75A⑩, V _{GS} = 0V ④
t _{rr}	Reverse Recovery Time	—	56	84	ns	T _J = 25°C, I _F = 75A⑩, V _{DD} = 20V
Q _{rr}	Reverse Recovery Charge	—	67	100	nC	di/dt = 100A/μs ④
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

Notes:

- ① Calculated continuous current based on maximum allowable junction temperature. Bond wire current limit is 195A. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements. (Refer to AN-1140)
- ② Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ③ Limited by T_{Jmax}, starting T_J = 25°C, L = 0.24mH, R_G = 25Ω, I_{AS} = 75A, V_{GS} = 10V. Part not recommended for use above this value.
- ④ Pulse width ≤ 1.0ms; duty cycle ≤ 2%.
- ⑤ C_{oss eff.} is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.
- ⑥ This value determined from sample failure population, starting T_J = 25°C, L = 0.24mH, R_G = 25Ω, I_{AS} = 75A, V_{GS} = 10V.
- ⑦ This is applied to D²Pak When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994
- ⑧ Max R_{DS(on)} for D²Pak and TO-262 (SMD) devices.
- ⑨ TO-220 device will have an R_{th} value of 0.45°C/W.
- ⑩ All AC and DC test condition based on old Package limitation current = 75A.

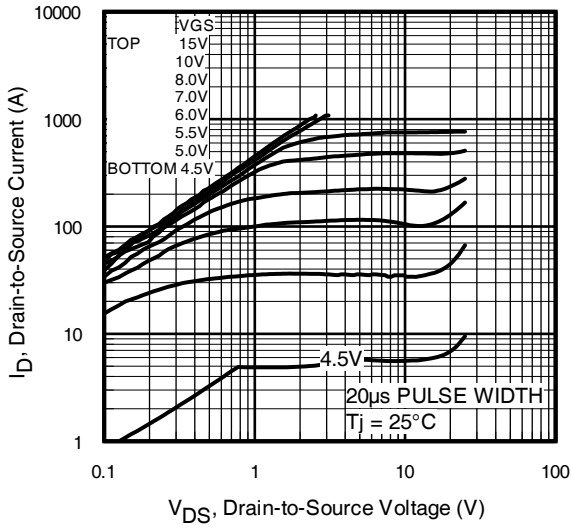


Fig. 1 Typical Output Characteristics

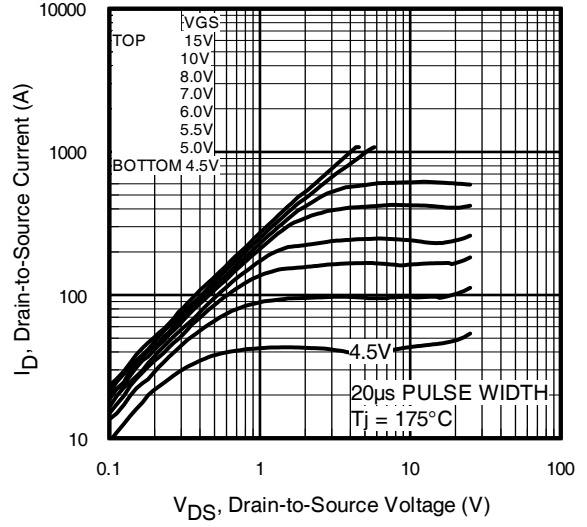


Fig. 2 Typical Output Characteristics

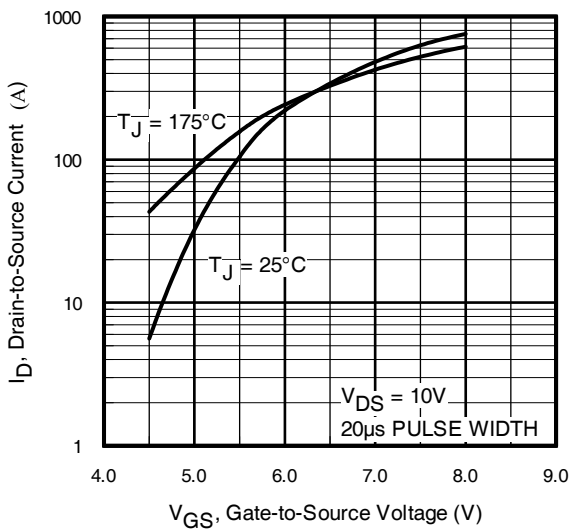


Fig. 3 Typical Transfer Characteristics

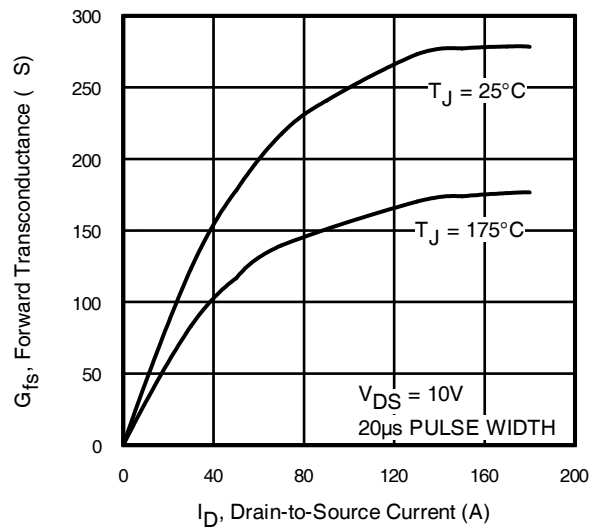


Fig. 4 Typical Forward Transconductance vs. Drain Current

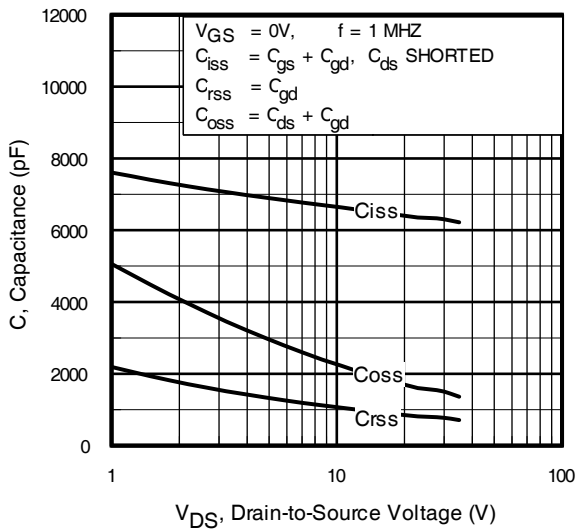


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

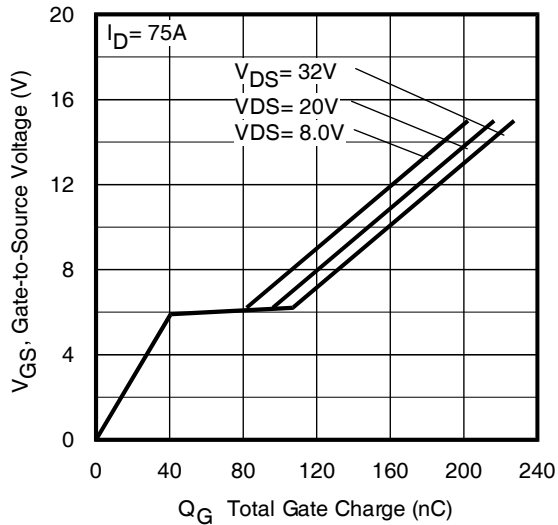


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

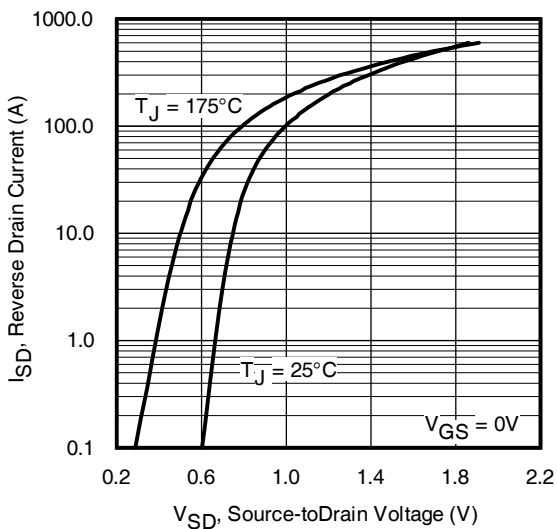


Fig 7 Typical Source-to-Drain Diode Forward Voltage

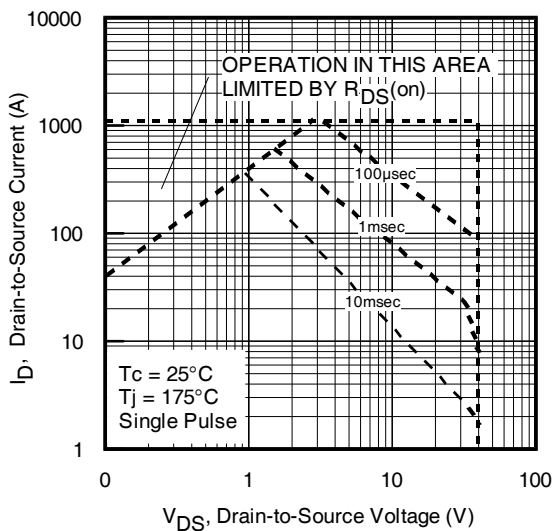


Fig 8. Maximum Safe Operating Area

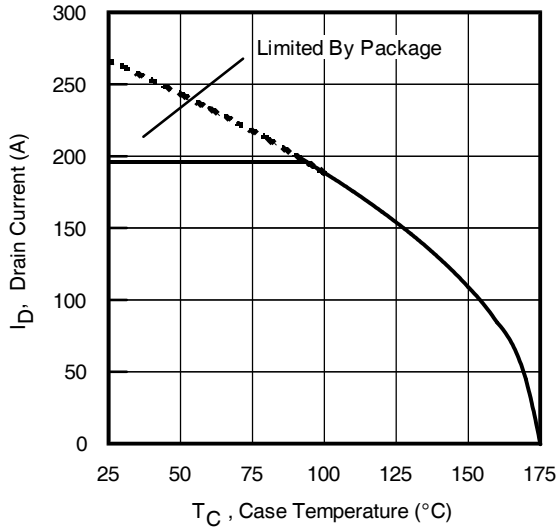


Fig 9. Maximum Drain Current vs. Case Temperature

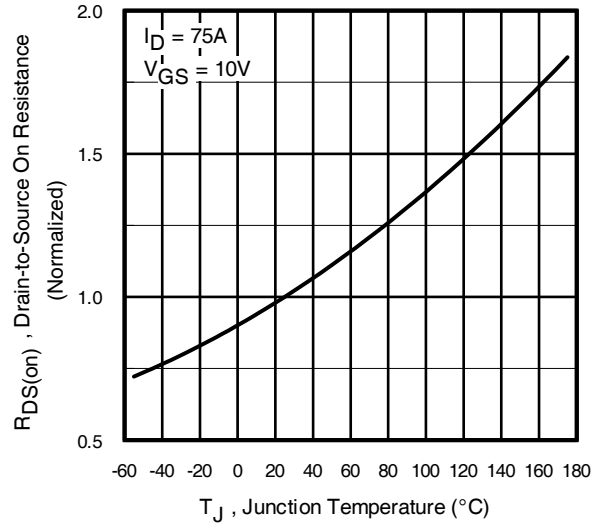


Fig 10. Normalized On-Resistance vs. Temperature

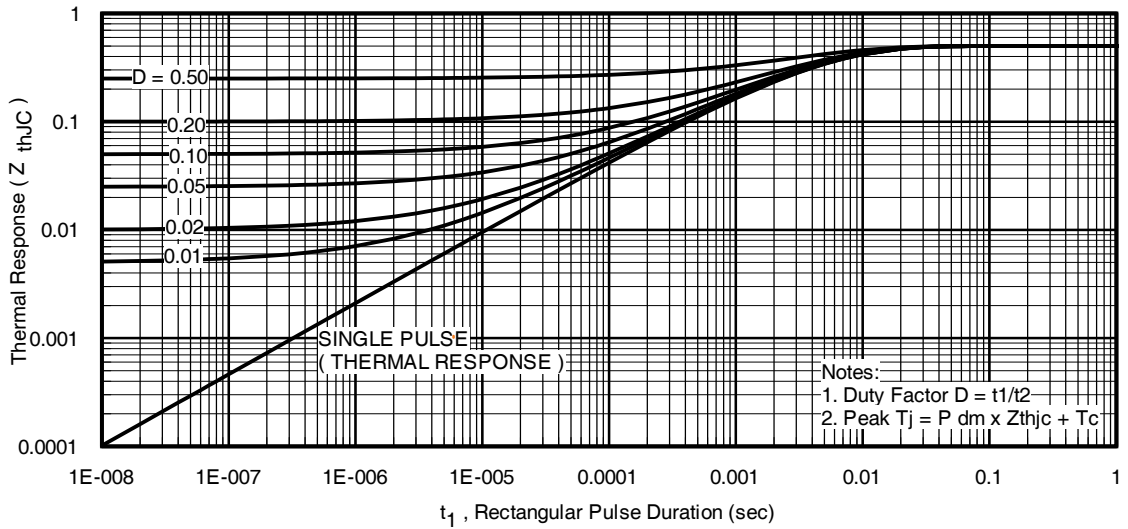


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

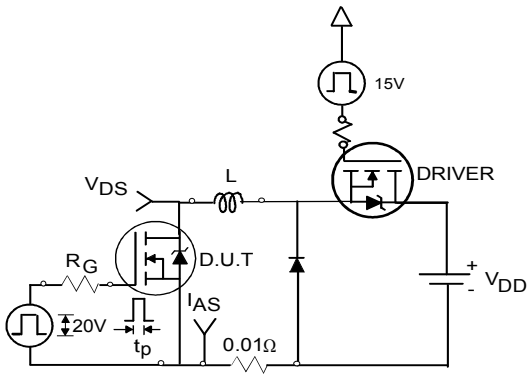


Fig 12a. Unclamped Inductive Test Circuit

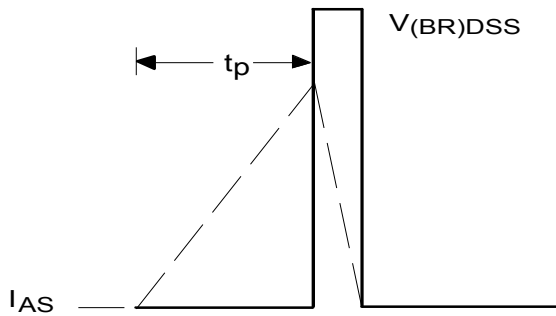


Fig 12b. Unclamped Inductive Waveforms

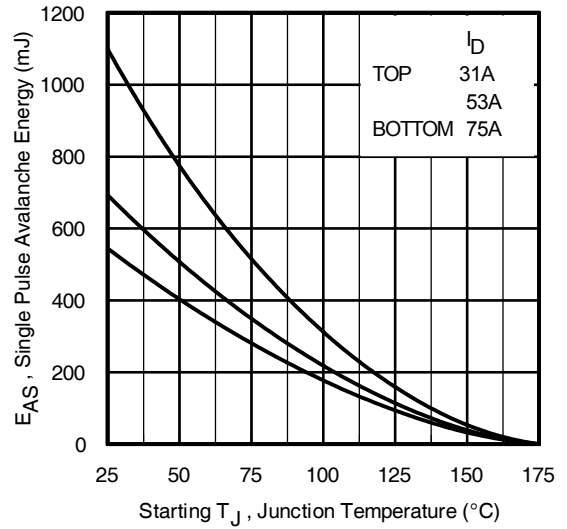


Fig 12c. Maximum Avalanche Energy vs. Drain Current

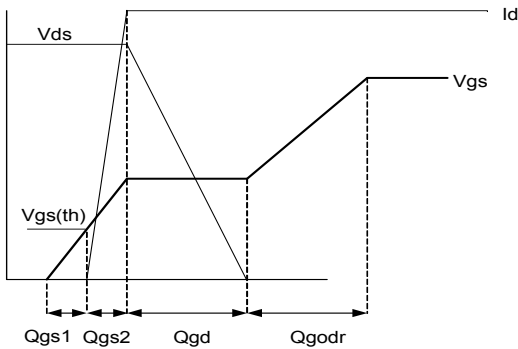


Fig 13a. Gate Charge Waveform

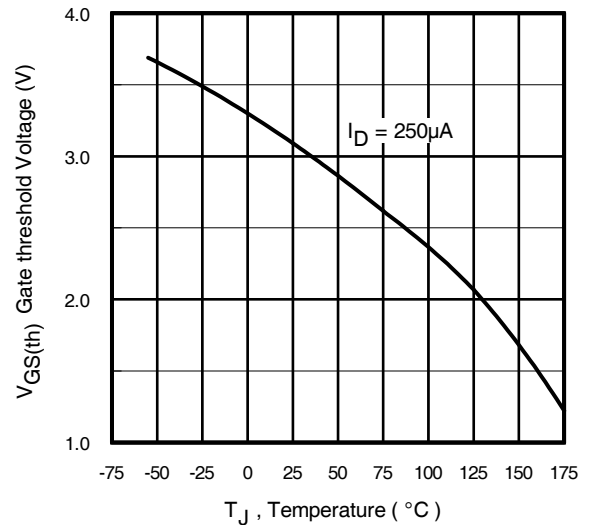


Fig 14. Threshold Voltage vs. Temperature

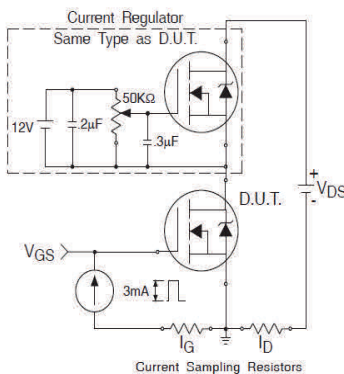


Fig 13b. Gate Charge Test Circuit

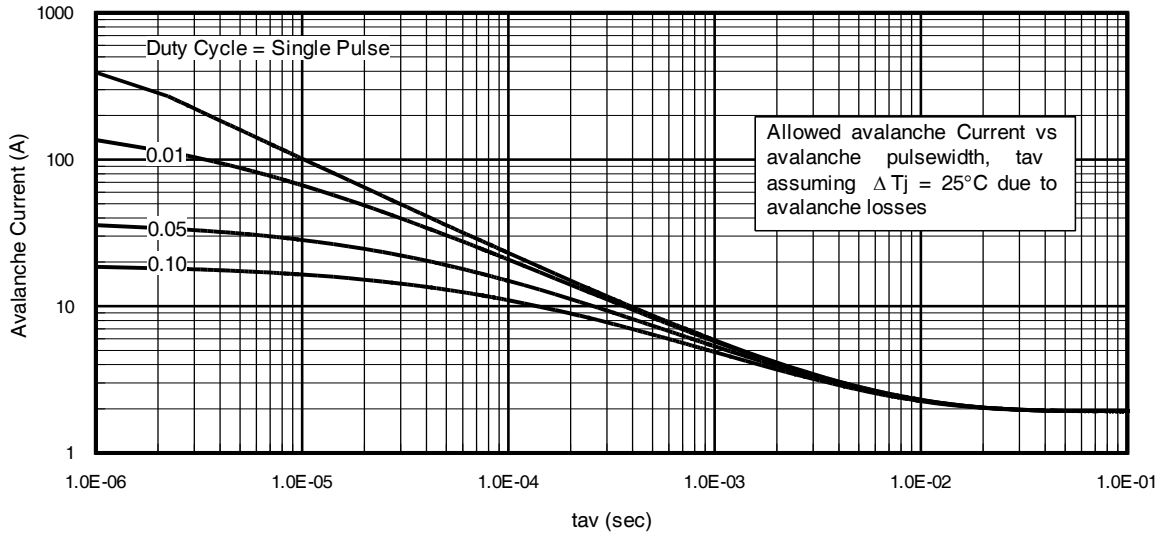


Fig 15. Typical Avalanche Current vs. Pulse width

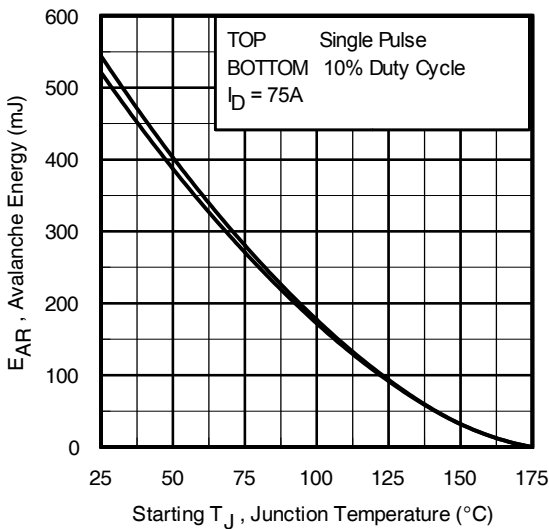


Fig 16. Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 15, 16:
 (For further info, see AN-1005 at www.infineon.com)

1. Avalanche failures assumption:
 Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 15, 16).
 t_{av} = Average time in avalanche.
 D = Duty cycle in avalanche = $t_{av} \cdot f$
 $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 13)

$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{thJC}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

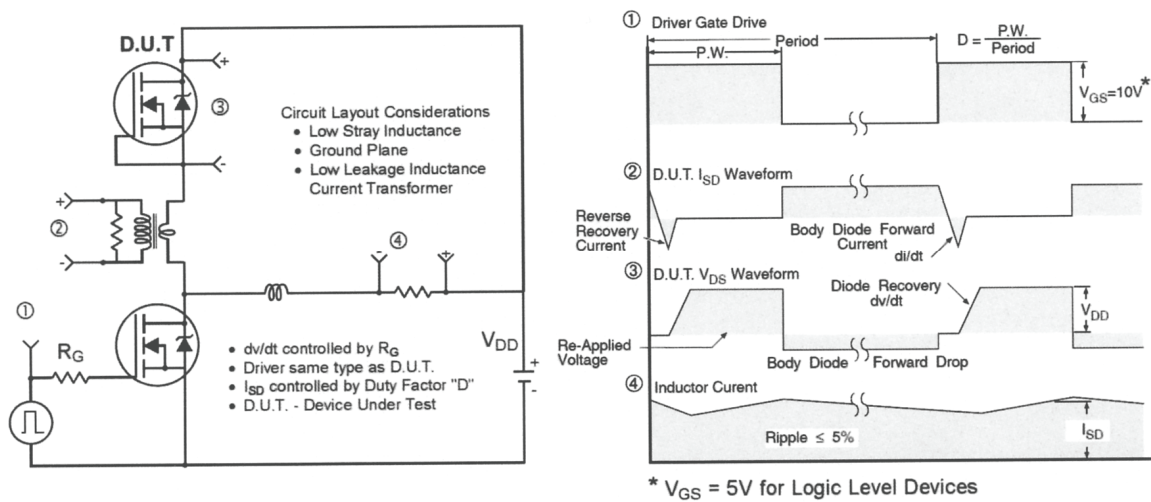


Fig 17. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

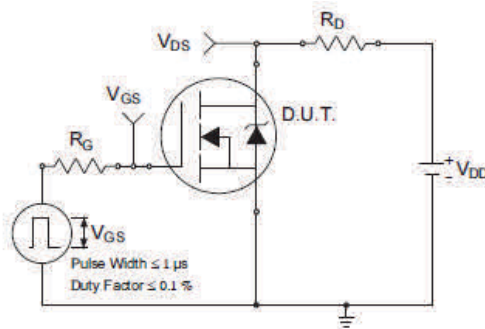


Fig 18a. Switching Time Test Circuit

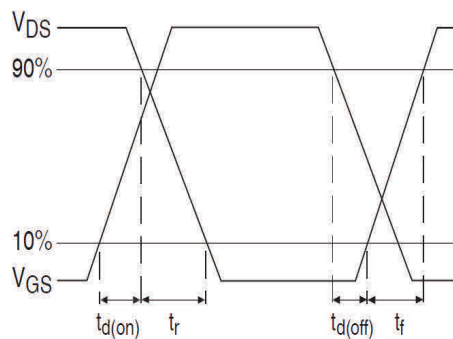
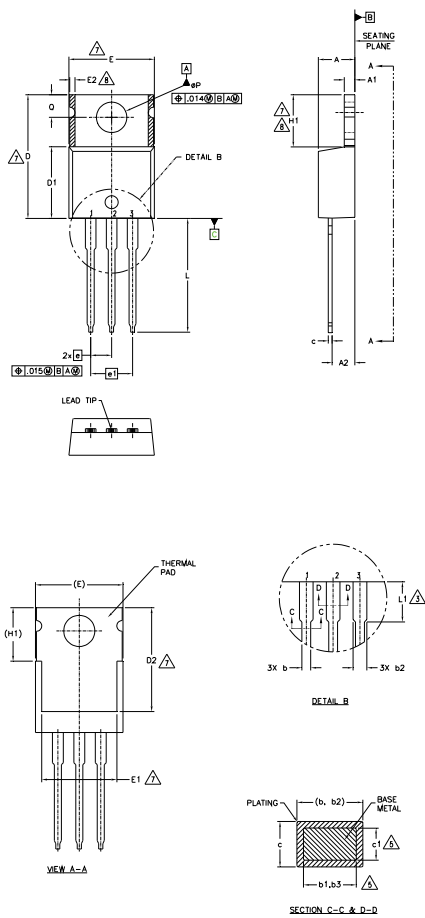


Fig 18b. Switching Time Waveforms

TO-220AB Package Outline (Dimensions are shown in millimeters (inches))



NOTES:

- 1.- DIMENSIONING AND TOLERANCING AS PER ASME Y14.5 M- 1994.
- 2.- DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
- 3.- LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
- 4.- DIMENSION D, D1 & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- 5.- DIMENSION b1, b3 & c1 APPLY TO BASE METAL ONLY.
- 6.- CONTROLLING DIMENSION : INCHES.
- 7.- THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS E,H1,D2 & E1
- 8.- DIMENSION E2 X H1 DEFINE A ZONE WHERE STAMPING AND SINGULATION IRREGULARITIES ARE ALLOWED.
- 9.- OUTLINE CONFORMS TO JEDEC TO-220, EXCEPT A2 (max.) AND D2 (min.) WHERE DIMENSIONS ARE DERIVED FROM THE ACTUAL PACKAGE OUTLINE.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	3.56	4.83	.140	.190	
A1	1.14	1.40	.045	.055	
A2	2.03	2.92	.080	.115	
b	0.38	1.01	.015	.040	
b1	0.38	0.97	.015	.038	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.36	0.61	.014	.024	
c1	0.36	0.56	.014	.022	5
D	14.22	16.51	.560	.650	4
D1	8.38	9.02	.330	.355	
D2	11.68	12.88	.460	.507	7
E	9.65	10.67	.380	.420	4,7
E1	6.86	8.89	.270	.350	7
E2	-	0.76	-	.030	8
e	2.54 BSC		.100 BSC		
e1	5.08 BSC		.200 BSC		
H1	5.84	6.86	.230	.270	7,8
L	12.70	14.73	.500	.580	
L1	3.56	4.06	.140	.160	3
øP	3.54	4.08	.139	.161	
Q	2.54	3.42	.100	.135	

LEAD ASSIGNMENTS

HEXFET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE

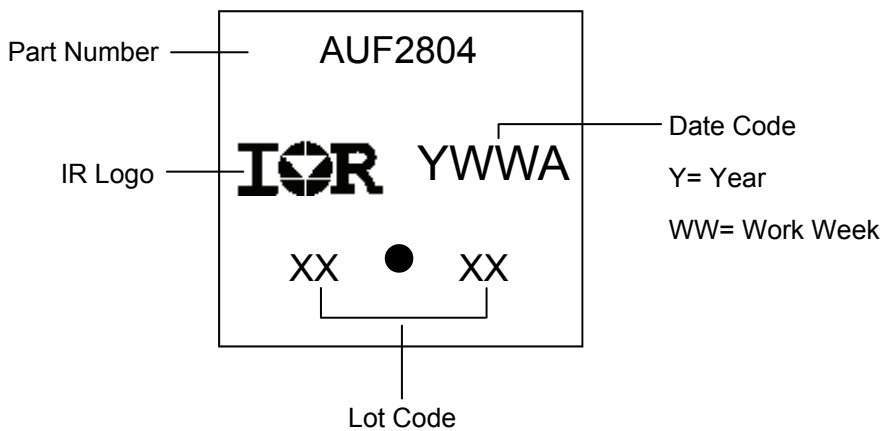
IGBTs, CoPACK

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER

DIODES

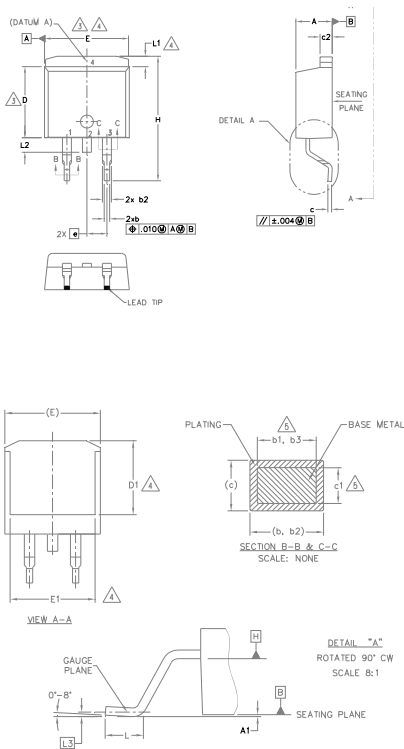
- 1.- ANODE
- 2.- CATHODE
- 3.- ANODE

TO-220AB Part Marking Information



TO-220AB package is not recommended for Surface Mount Application.

D²Pak (TO-263AB) Package Outline (Dimensions are shown in millimeters (inches))

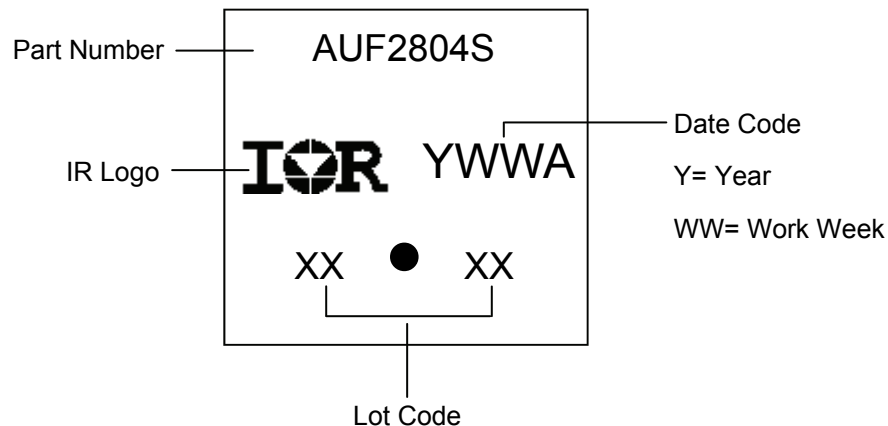


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
 2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
 3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
 4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
 5. DIMENSION b1, b3 AND c1 APPLY TO BASE METAL ONLY.
 6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
 7. CONTROLLING DIMENSION: INCH.
 8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-263AB.

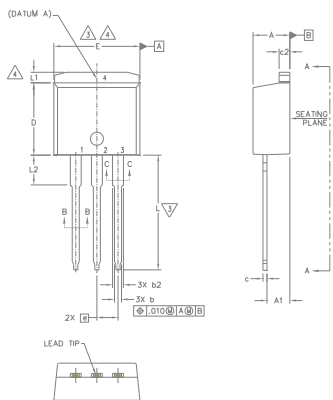
SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	0.00	0.254	.000	.010	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	—	.270	—	4
E	9.65	10.67	.380	.420	3,4
E1	6.22	—	.245	—	4
e	2.54 BSC		.100 BSC		
H	14.61	15.88	.575	.625	
L	1.78	2.79	.070	.110	
L1	—	1.68	—	.066	
L2	—	1.78	—	.070	4
L3	0.25 BSC		.010 BSC		

- LEAD ASSIGNMENTS
- DIODES**
- 1.- ANODE (TWO DIE) / OPEN (ONE DIE)
 - 2.- CATHODE
 - 3.- ANODE
- HEXFET**
- 1.- GATE
 - 2.- DRAIN
 - 3.- SOURCE
- IGBTs, CoPACK**
- 1.- GATE
 - 2.- COLLECTOR
 - 3.- EMITTER

D²Pak (TO-263AB) Part Marking Information



TO-262 Package Outline (Dimensions are shown in millimeters (inches))



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
6. CONTROLLING DIMENSION: INCH.
7. OUTLINE CONFORM TO JEDEC TO-262 EXCEPT A1(max.), b(min.) AND D1(min.) WHERE DIMENSIONS DERIVED THE ACTUAL PACKAGE OUTLINE.

LEAD ASSIGNMENTS

IGBTs, CoPACK

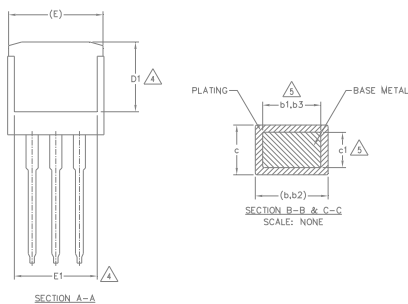
- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

HEXFET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

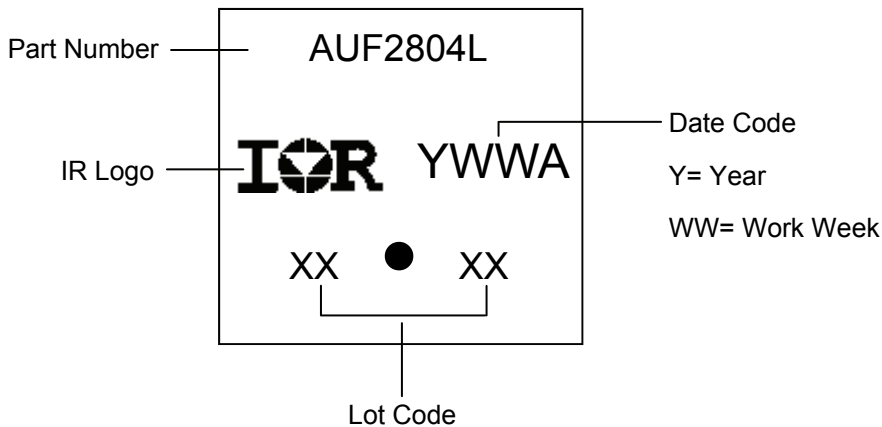
DIODES

- 1.- ANODE (TWO DIE) / OPEN (ONE DIE)
- 2, 4.- CATHODE
- 3.- ANODE

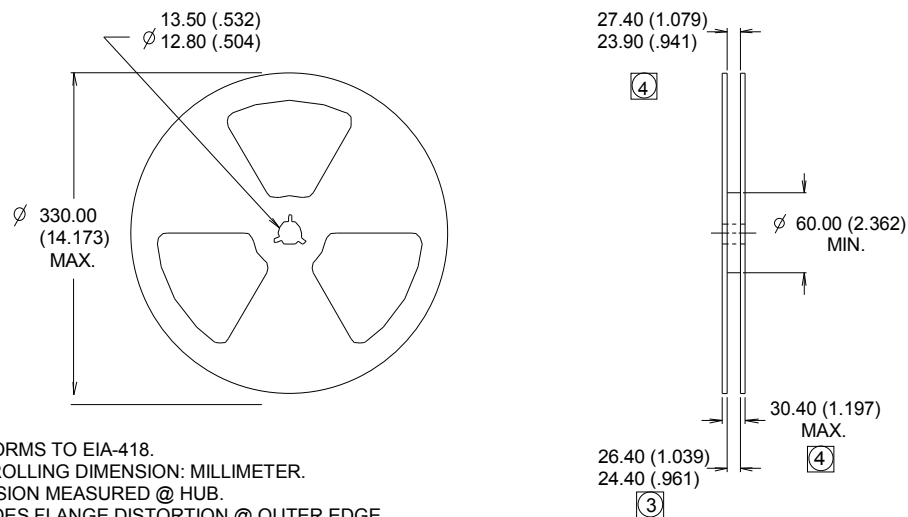
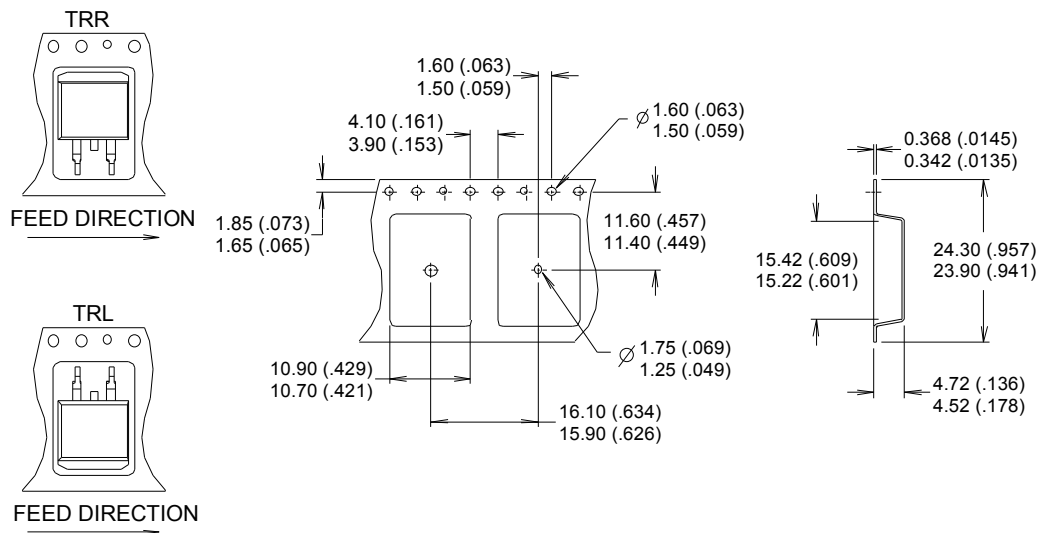


SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	2.03	3.02	.080	.119	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	-	.270	-	4
E	9.65	10.67	.380	.420	3,4
E1	6.22	-	.245	-	4
e	2.54 BSC		.100 BSC		
L	13.46	14.10	.530	.555	
L1	-	1.65	-	.065	4
L2	3.56	3.71	.140	.146	

TO-262 Part Marking Information



D²Pak (TO-263AB) Tape & Reel Information (Dimensions are shown in millimeters (inches))



Qualification Information

Qualification Level		Automotive (per AEC-Q101)	
		Comments: This part number(s) passed Automotive qualification. Infineon's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
Moisture Sensitivity Level		TO-220AB	N/A
		TO-262	MSL1
		D ² -Pak	
ESD	Machine Model	Class M4 [†] AEC-Q101-002	
	Human Body Model	Class H3A [†] AEC-Q101-001	
	Charged Device Model	Class C5 [†] AEC-Q101-005	
RoHS Compliant		Yes	

† Highest passing voltage.

Revision History

Date	Comments
9/30/2015	<ul style="list-style-type: none"> Updated datasheet with corporate template Corrected ordering table on page 1.

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