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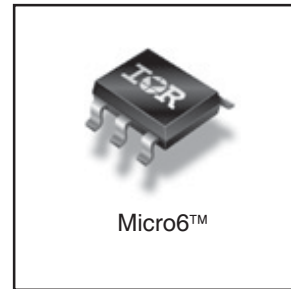
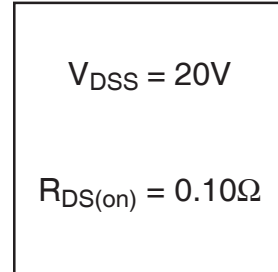
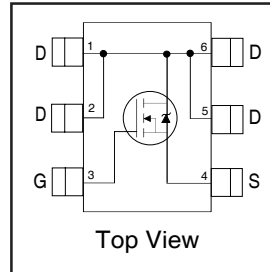
HEXFET® Power MOSFET

- Generation V Technology
- Micro6 Package Style
- Ultra Low $R_{DS(on)}$
- N-Channel MOSFET
- Lead-Free

Description

Fifth Generation HEXFET® power MOSFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET® power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The Micro6™ package with its customized leadframe produces a HEXFET® power MOSFET with $R_{DS(on)}$ 60% less than a similar size SOT-23. This package is ideal for applications where printed circuit board space is at a premium. It's unique thermal design and $R_{DS(on)}$ reduction enables a current-handling increase of nearly 300% compared to the SOT-23.



Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_A = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 4.5V$	3.2	A
$I_D @ T_A = 70^\circ C$	Continuous Drain Current, $V_{GS} @ 4.5V$	2.6	
I_{DM}	Pulsed Drain Current ①	18	
$P_D @ T_A = 25^\circ C$	Power Dissipation	1.7	W
	Linear Derating Factor	13	mW/°C
V_{GS}	Gate-to-Source Voltage	± 12	V
dv/dt	Peak Diode Recovery dv/dt ②	5.0	V/ns
T_J, T_{STG}	Junction and Storage Temperature Range	-55 to + 150	°C

Thermal Resistance Ratings

Parameter		Min.	Typ.	Max	Units
$R_{\theta JA}$	Maximum Junction-to-Ambient ④	—	—	75	°C/W

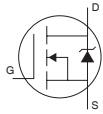
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Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

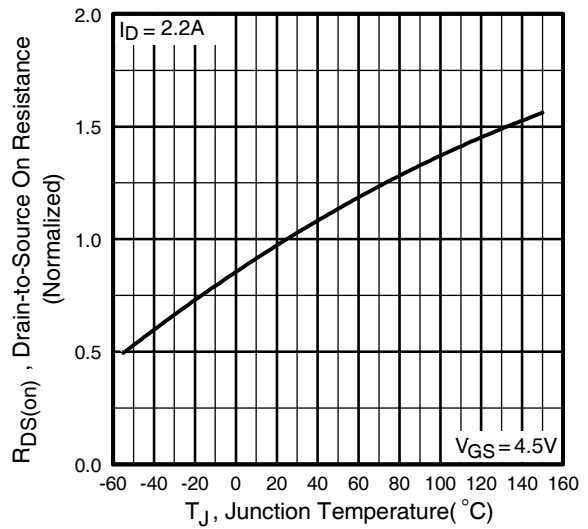
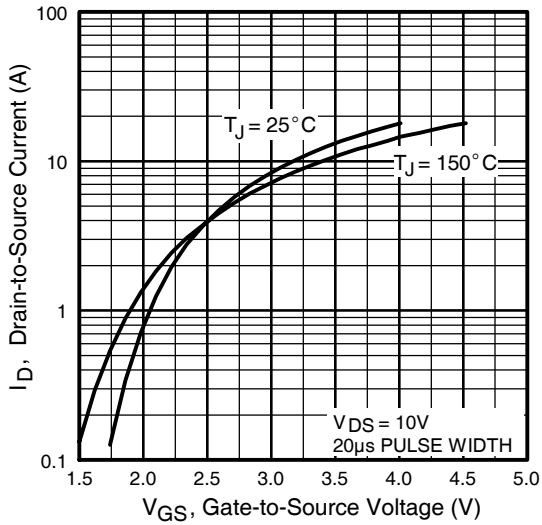
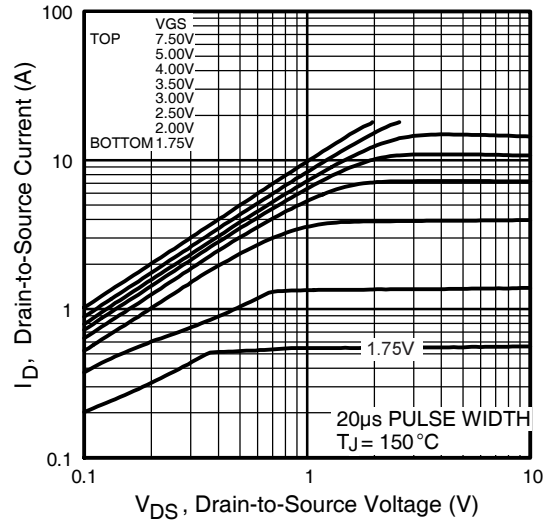
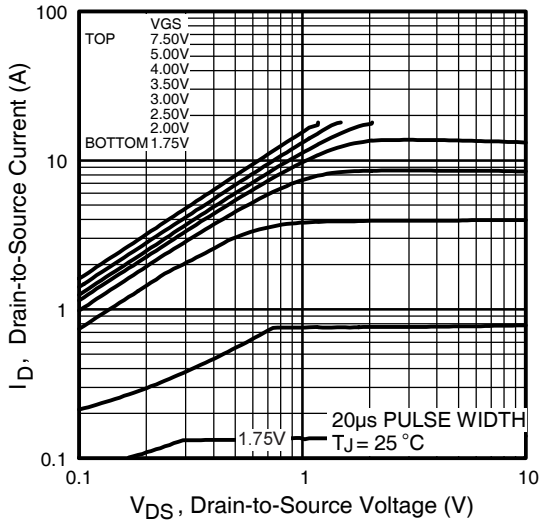
	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	20	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔV _{(BR)DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	0.032	—	V/°C	Reference to 25°C, I _D = 1mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	—	0.10	Ω	V _{GS} = 4.5V, I _D = 2.2A ③
		—	—	0.17		V _{GS} = 2.7V, I _D = 1.1A ③
V _{GS(th)}	Gate Threshold Voltage	0.70	—	—	V	V _{DS} = V _{GS} , I _D = 250μA
g _{fs}	Forward Transconductance	3.2	—	—	S	V _{DS} = 10V, I _D = 1.1A
I _{DSS}	Drain-to-Source Leakage Current	—	—	1.0	μA	V _{DS} = 16V, V _{GS} = 0V
		—	—	25		V _{DS} = 16V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V _{GS} = 12V
	Gate-to-Source Reverse Leakage	—	—	-100		V _{GS} = -12V
Q _g	Total Gate Charge	—	4.7	7.0	nC	I _D = 2.2A
Q _{gs}	Gate-to-Source Charge	—	0.97	1.5		V _{DS} = 16V
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	1.8	2.6		V _{GS} = 4.5V, See Fig. 6 and 9 ③
t _{d(on)}	Turn-On Delay Time	—	7.0	—	ns	V _{DD} = 10V
t _r	Rise Time	—	11	—		I _D = 2.2A
t _{d(off)}	Turn-Off Delay Time	—	12	—		R _G = 6.0Ω
t _f	Fall Time	—	4.0	—		R _D = 4.4Ω, See Fig. 10 ③
C _{iss}	Input Capacitance	—	300	—	pF	V _{GS} = 0V
C _{oss}	Output Capacitance	—	120	—		V _{DS} = 15V
C _{rss}	Reverse Transfer Capacitance	—	50	—		f = 1.0MHz, See Fig. 5

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	1.7	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	18		
V _{SD}	Diode Forward Voltage	—	—	1.2	V	T _J = 25°C, I _S = 2.2A, V _{GS} = 0V ②
t _{rr}	Reverse Recovery Time	—	40	60	ns	T _J = 25°C, I _F = 2.2A
Q _{rr}	Reverse Recovery Charge	—	37	55	nC	di/dt = 100A/μs ②

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② I_{SD} ≤ 2.2A, di/dt ≤ 110A/μs, V_{DD} ≤ V_{(BR)DSS}, T_J ≤ 150°C
- ③ Pulse width ≤ 300μs; duty cycle ≤ 2%.
- ④ Surface mounted on FR-4 board, t ≤ 5sec.



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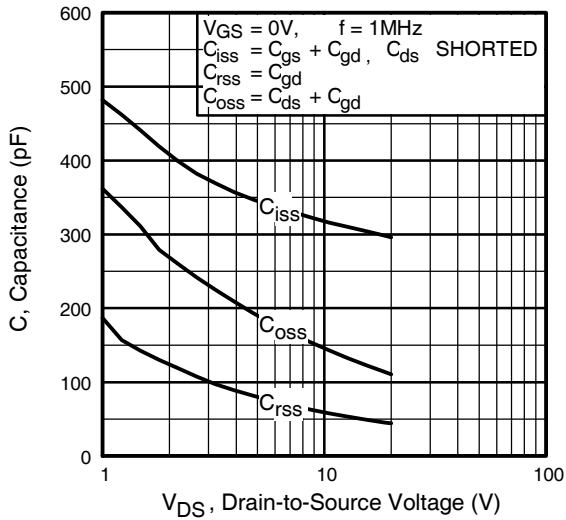


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

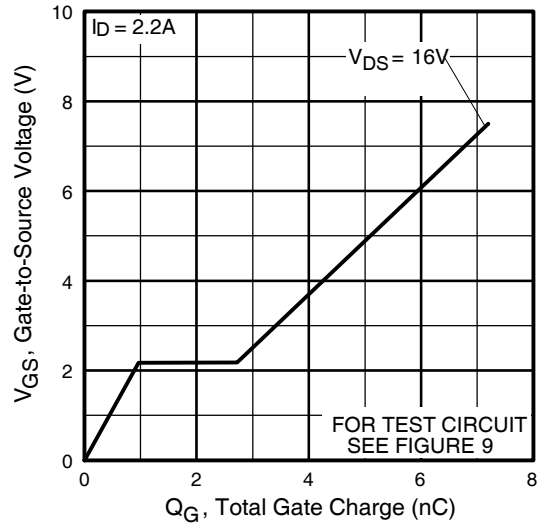


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

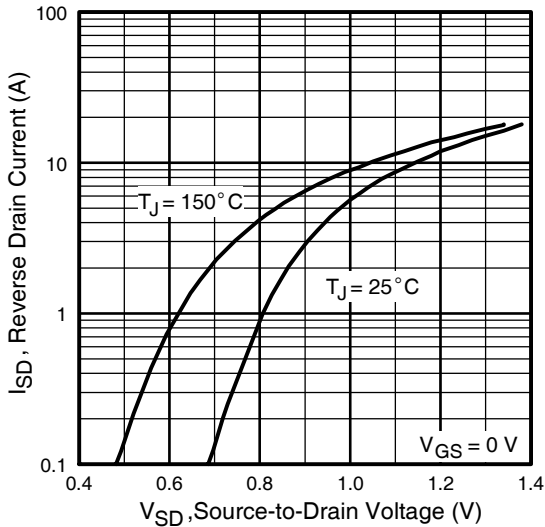


Fig 7. Typical Source-Drain Diode Forward Voltage

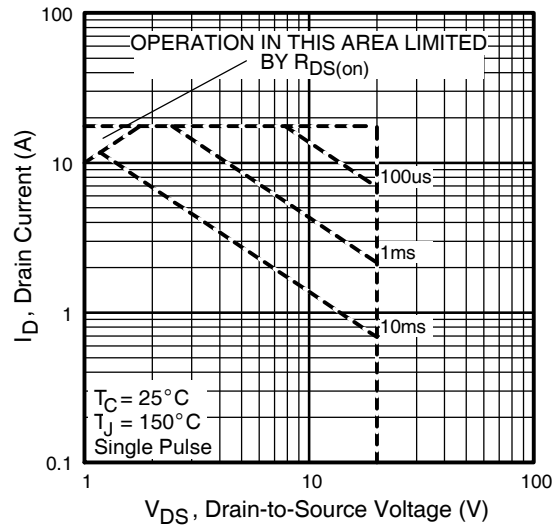


Fig 8. Maximum Safe Operating Area

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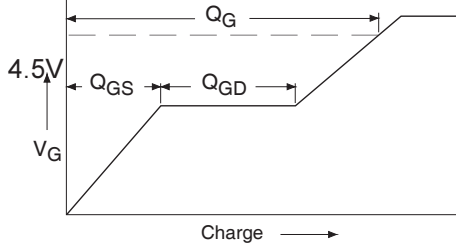


Fig 9a. Basic Gate Charge Waveform

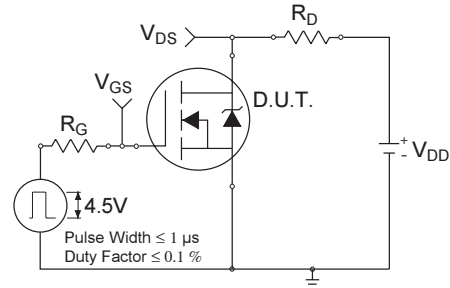


Fig 10a. Switching Time Test Circuit

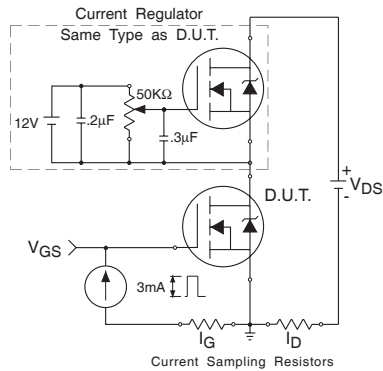


Fig 9b. Gate Charge Test Circuit

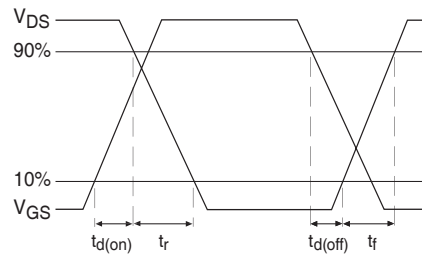


Fig 10b. Switching Time Waveforms

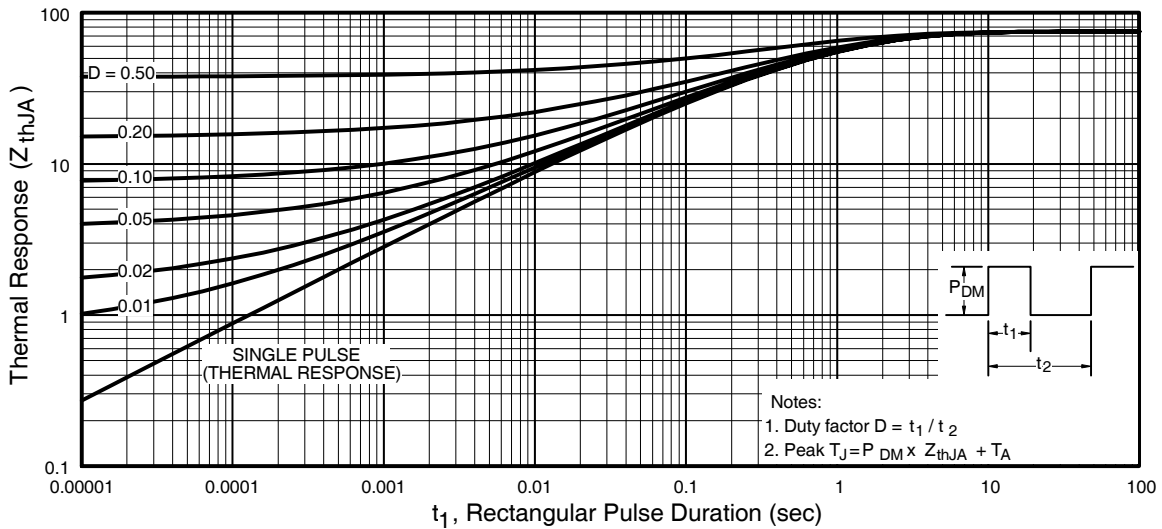
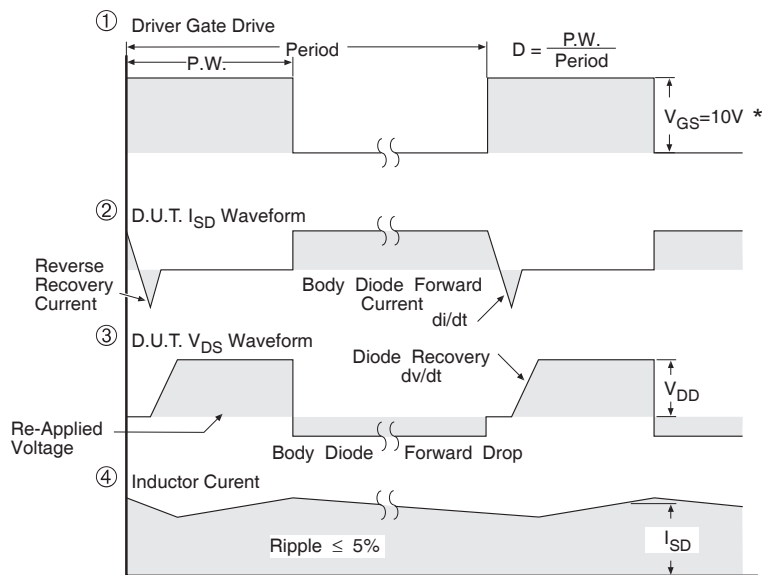
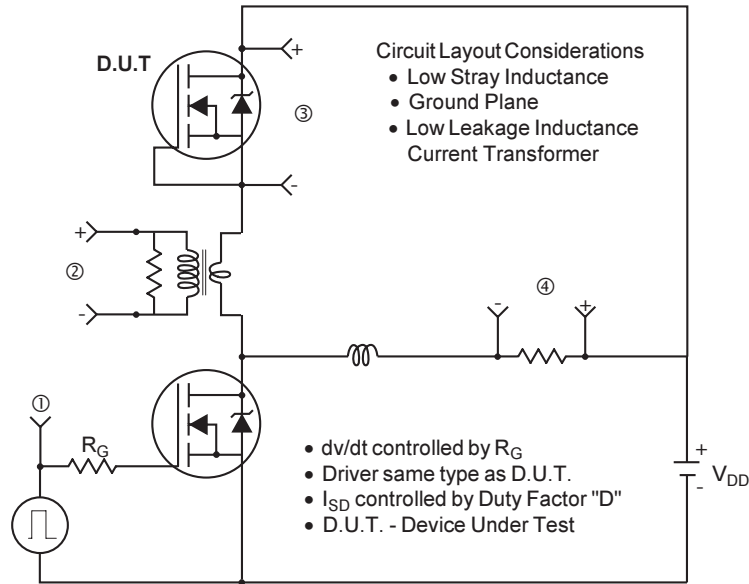


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

Peak Diode Recovery dv/dt Test Circuit

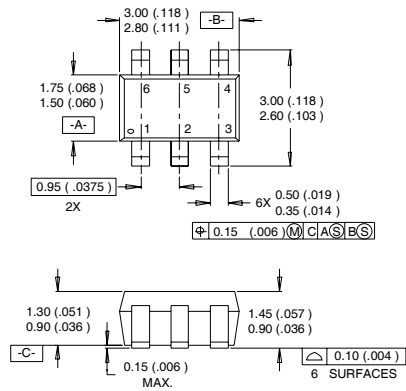


* $V_{GS} = 5V$ for Logic Level Devices

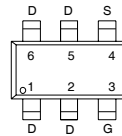
Fig 12. For N-channel HEXFET® power MOSFETs

Micro6 (SOT23 6L) Package Outline

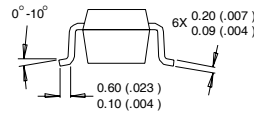
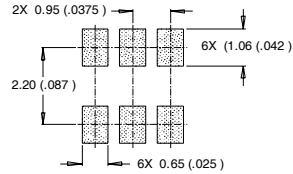
Dimensions are shown in millimeters (inches)



LEAD ASSIGNMENTS



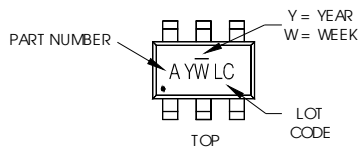
RECOMMENDED FOOTPRINT



- NOTES :
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
 2. CONTROLLING DIMENSION : MILLIMETER.
 3. DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).

Micro6 (SOT23 6L) Part Marking Information

W = (1-26) IF PRECEDED BY LAST DIGIT OF CALENDAR YEAR



PART NUMBER CODE REFERENCE:

- A = IRLMS1902
- B = IRLMS1503
- C = IRLMS6702
- D = IRLMS5703
- E = IRLMS6802
- F = IRLMS4502
- G = IRLMS2002
- H = IRLMS6803

Note: A line above the work week (as shown here) indicates Lead-Free.

YEAR	Y	WORK WEEK	W
2001	1	01	A
2002	2	02	B
2003	3	03	C
2004	4	04	D
2005	5		
2006	6		
2007	7		
2008	8		
2009	9		
2010	0	24	X
		25	Y
		26	Z

W = (27-52) IF PRECEDED BY A LETTER

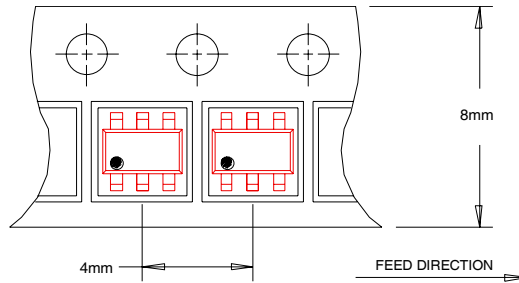
YEAR	Y	WORK WEEK	W
2001	A	27	A
2002	B	28	B
2003	C	29	C
2004	D	30	D
2005	E		
2006	F		
2007	G		
2008	H		
2009	J		
2010	K	50	X
		51	Y
		52	Z

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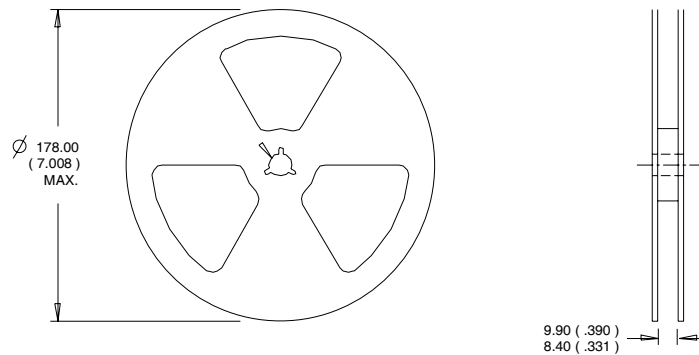
Micro6 Tape & Reel Information

Dimensions are shown in millimeters (inches)



NOTES :

1. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES:

1. CONTROLLING DIMENSION : MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

This product has been designed and qualified for the consumer market.
Qualification Standards can be found on IR's Web site.
Data and specifications subject to change without notice.

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