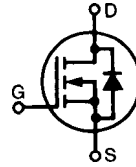


HiPerFET™ Power MOSFETs

N-Channel Enhancement Mode
High dv/dt, Low t_{rr}, HDMOS™ Family

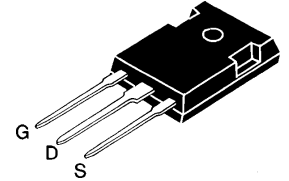
IXFH8N80
IXFH9N80

V _{DSS}	I _{D25}	R _{DS(on)}	t _{rr}
800V	8A	1.1Ω	250 ns
800V	9A	0.9Ω	250 ns

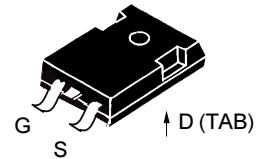


Symbol	Test Conditions	Maximum Ratings	
V _{DSS}	T _J = 25°C to 150°C	800	V
V _{DGR}	T _J = 25°C to 150°C; R _{GS} = 1 MΩ	800	V
V _{GS}	Continuous	±20	V
V _{GSM}	Transient	±30	V
I _{D25}	T _C = 25°C	8N80	8 A
		9N80	9 A
I _{DM}	T _C = 25°C, pulse width limited by T _{JM}	8N80	32 A
		9N80	36 A
I _{AR}	T _C = 25°C	8N80	8 A
		9N80	9 A
E _{AR}	T _C = 25°C	18	mJ
dv/dt	I _S ≤ I _{DM} , di/dt ≤ 100 A/μs, V _{DD} ≤ V _{DSS} , T _J ≤ 150°C, R _G = 2 Ω	5	V/ns
P _D	T _C = 25°C	180	W
T _J		-55 ... +150	°C
T _{JM}		150	°C
T _{stg}		-55 ... +150	°C
M _d	Mounting torque	1.13/10 Nm/lb.in.	
Weight		TO-204 = 18 g, TO-247 = 6 g	
Maximum lead temperature for soldering 1.6 mm (0.062 in.) from case for 10 s		300	°C

TO-247 AD (IXFH)



TO-247 SMD*



G = Gate D = Drain
S = Source TAB = Drain

*Add suffix letter "S" for surface mountable package

Symbol	Test Conditions	Characteristic Values (T _J = 25°C, unless otherwise specified)		
		min.	typ.	max.
V _{DSS}	V _{GS} = 0 V, I _D = 3 mA V _{DSS} temperature coefficient	800	0.088	V %/K
V _{GS(th)}	V _{DS} = V _{GS} , I _D = 2.5 mA V _{GS(th)} temperature coefficient	2	-0.257	V %/K
I _{GSS}	V _{GS} = ±20 V _{DC} , V _{DS} = 0			±100 nA
I _{DSS}	V _{DS} = 0.8 • V _{DSS} , T _J = 25°C V _{GS} = 0 V, T _J = 125°C			250 μA 1 mA
R _{DS(on)}	V _{GS} = 10 V, I _D = 0.5 • I _{D25} Pulse test, t ≤ 300 μs, duty cycle δ ≤ 2%	8N80 9N80		1.1 Ω 0.9 Ω

Features

- International standard packages
- Low R_{DS(on)} HDMOS™ process
- Rugged polysilicon gate cell structure
- Unclamped Inductive Switching (UIS) rated
- Low package inductance
- easy to drive and to protect
- Fast intrinsic Rectifier

Applications

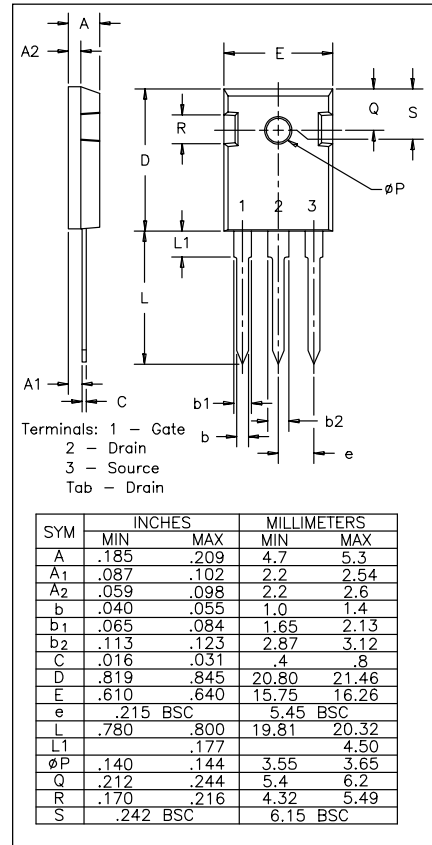
- DC-DC converters
- Battery chargers
- Switched-mode and resonant-mode power supplies
- DC choppers
- AC motor control
- Temperature and lighting controls

Advantages

- Easy to mount with 1 screw (TO-247) (isolated mounting screw hole)
- Space savings
- High power density

Symbol	Test Conditions	Characteristic Values ($T_J = 25^\circ\text{C}$, unless otherwise specified)		
		min.	typ.	max.
g_{fs}	$V_{DS} = 10\text{ V}; I_D = 0.5 \cdot I_{D25}$, pulse test	4	7	S
C_{iss}	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1\text{ MHz}$		2600	pF
C_{oss}			240	pF
C_{rss}			60	pF
$t_{d(on)}$	$V_{GS} = 10\text{ V}, V_{DS} = 0.5 \cdot V_{DSS}, I_D = 0.5 \cdot I_{D25}$ $R_G = 4.7\ \Omega$ (External)		35	ns
t_r			15	ns
$t_{d(off)}$			70	ns
t_f			35	ns
$Q_{g(on)}$	$V_{GS} = 10\text{ V}, V_{DS} = 0.5 \cdot V_{DSS}, I_D = 0.5 \cdot I_{D25}$		85	130 nC
Q_{gs}			15	30 nC
Q_{gd}			40	70 nC
R_{thJC}				0.7 K/W
R_{thCK}				0.25 K/W

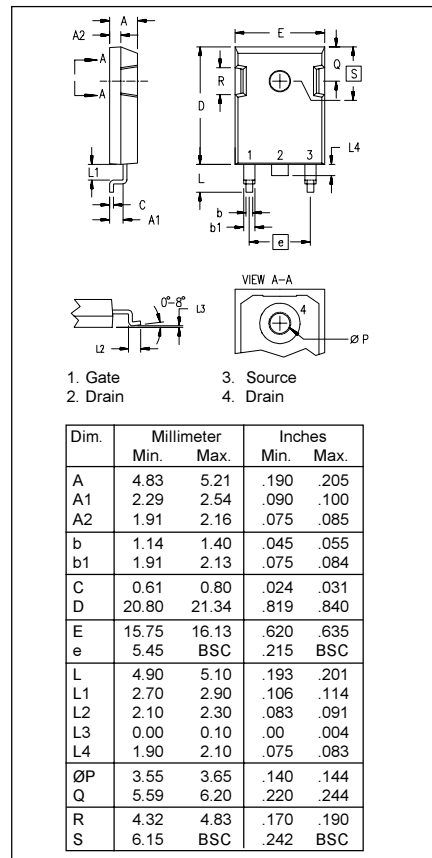
TO-247 AD (IXFH) Outline



Source-Drain Diode

Symbol	Test Conditions	Characteristic Values ($T_J = 25^\circ\text{C}$, unless otherwise specified)		
		min.	typ.	max.
I_S	$V_{GS} = 0$	8N80 9N80		8 A 9 A
I_{SM}	Repetitive; pulse width limited by T_{JM}	8N80 9N80		32 A 36 A
V_{SD}	$I_F = I_S, V_{GS} = 0\text{ V}$, Pulse test, $t \leq 300\ \mu\text{s}$, duty cycle $\delta \leq 2\%$			1.5 V
t_{rr}	$I_F = I_S$ $-di/dt = 100\text{ A}/\mu\text{s}$, $V_R = 100\text{ V}$	$T_J = 25^\circ\text{C}$		250 ns
		$T_J = 125^\circ\text{C}$		400 ns
Q_{RM}		$T_J = 25^\circ\text{C}$	0.5	μC
		$T_J = 125^\circ\text{C}$	1.0	μC
I_{RM}		$T_J = 25^\circ\text{C}$	7.5	A
		$T_J = 125^\circ\text{C}$	9.0	A

TO-247 SMD Outline



IXYS reserves the right to change limits, test conditions, and dimensions.

IXYS MOSFETS and IGBTs are covered by one or more of the following U.S. patents: 4,835,592 4,881,106 5,017,508 5,049,961 5,187,117 5,486,715
4,850,072 4,931,844 5,034,796 5,063,307 5,237,481 5,381,025

Figure 1. Output Characteristics at 25°C

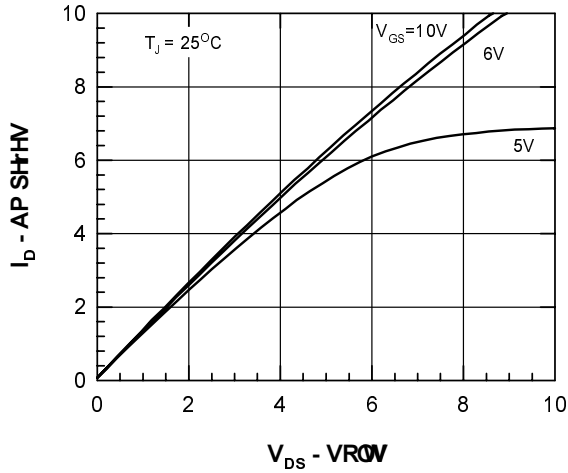


Figure 2. Output Characteristics at 125°C

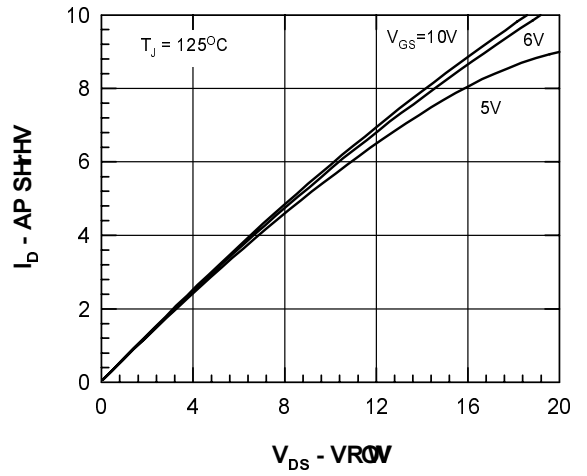


Figure 3. $R_{DS(on)}$ normalized to 15A/25°C vs. I_D

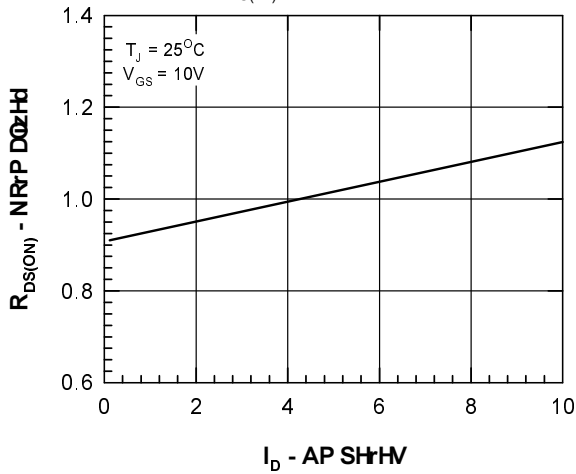


Figure 4. $R_{DS(on)}$ normalized to 15A/25°C vs. T_J

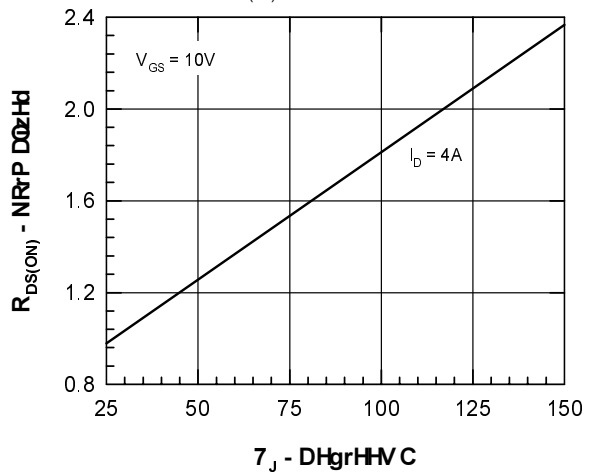


Figure 5. Drain Current vs. Case Temperature

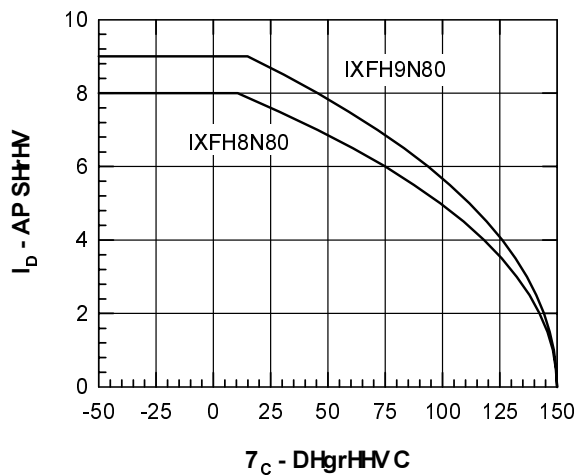


Figure 6. Admittance Curves

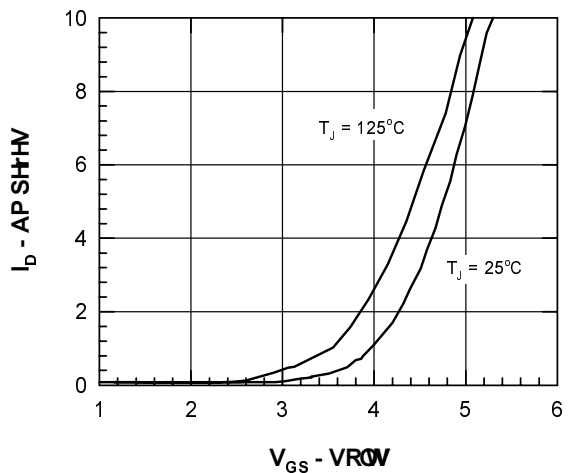


Figure 7. Gate Charge

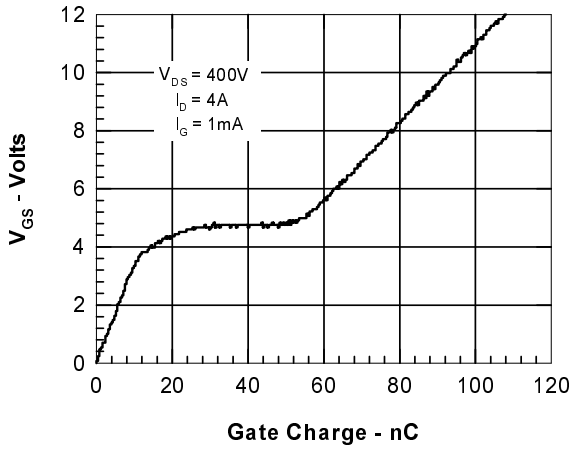


Figure 8. Capacitance Curves

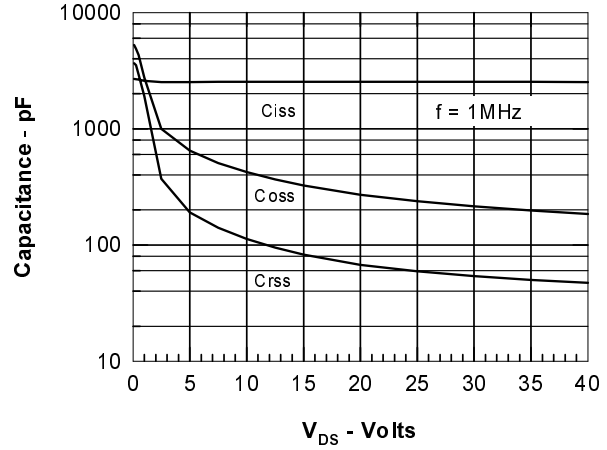


Figure 9. Forward Voltage Drop of the Intrinsic Diode

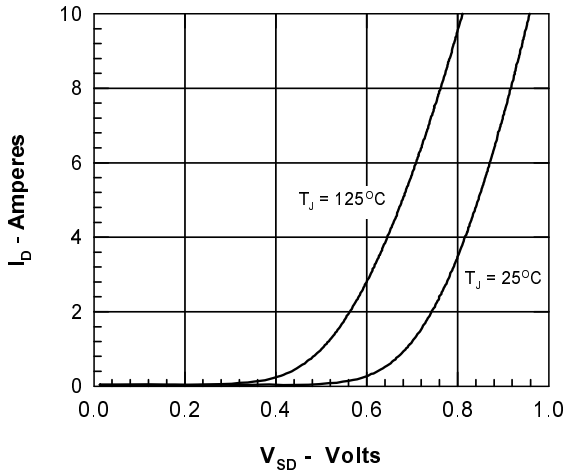


Figure 10. Forward Bias Safe Operating Area

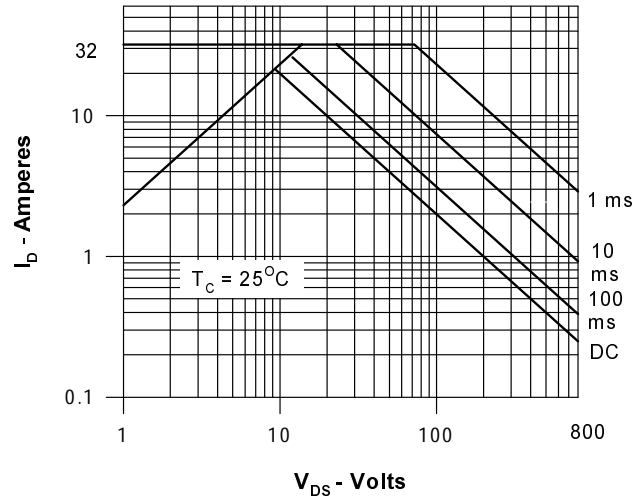
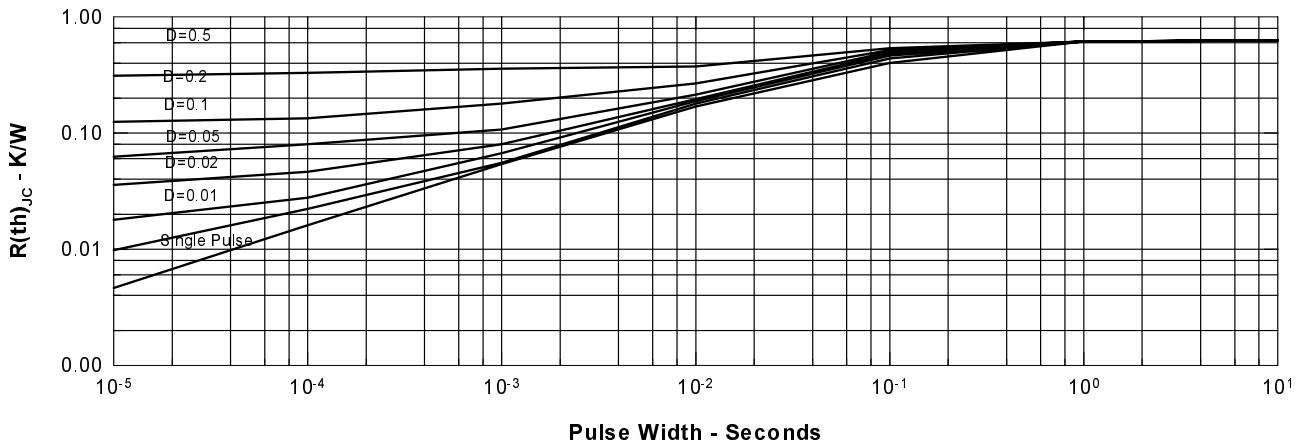


Figure 11. Transient Thermal Resistance



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