



+5V, Fail-Safe, 40Mbps, Profibus RS-485/ RS-422 Transceivers

MAX3465-MAX3469

General Description

The MAX3465–MAX3469 are high-speed differential bus transceivers for RS-485 and RS-422 communications. They are designed to meet TIA/EIA-422-B, TIA/EIA-485-A, V.11, and X.27 standards. The transceiver complies with the Profibus specification providing +2.1V minimum output level with a 54Ω load, 40Mbps data rate, and output skew less than 2ns. Each part contains one three-state differential line driver and one differential input line receiver. The devices operate from a +5V supply and feature true fail-safe circuitry, which guarantees a logic-high receiver output when the receiver inputs are open or shorted. This enables all receiver outputs on a terminated bus to output logic highs when all transmitters are disabled.

All devices feature a 1/4-standard-unit load receiver input impedance that allows 128 transceivers on the bus. Driver and receiver propagation delays are guaranteed under 20ns for multidrop, clock distribution applications. Drivers are short-circuit current limited and are protected against excessive power dissipation by thermal-shutdown circuitry. The driver and receiver feature active-high and active-low enables, respectively, that can be connected together externally to serve as a direction control.

Applications

High-Speed RS-485 Communications
High-Speed RS-422 Communications
Level Translators
Industrial-Control Local Area Networks
Profibus Applications

Features

- ◆ Recommended for Profibus Applications
- ◆ Up to 40Mbps Data Rate
- ◆ 15ns Transmitter Propagation Delay
- ◆ 20ns Receiver Propagation Delay
- ◆ 2ns Transmitter and Receiver Skew
- ◆ High Differential Driver Output Level (2.1V on 54Ω)
- ◆ Hot-Swap Versions
- ◆ 1μA Shutdown Supply Current
- ◆ Low Supply Current Requirements (2.5mA, typ)
- ◆ Allow Up to 128 Transceivers on the Bus
- ◆ True Fail-Safe Receiver while Maintaining EIA/TIA-485 Compatibility
- ◆ Designed for Multipoint Transmissions on Long or Noisy Bus Lines
- ◆ Full-Duplex and Half-Duplex Versions Available
- ◆ Phase Controls to Correct for Twisted-Pair Reversal for 14-Pin Versions
- ◆ Current-Limiting and Thermal Shutdown for Driver Overload Protection

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX3465CSD	0°C to +70°C	14 SO
MAX3465CPD	0°C to +70°C	14 Plastic DIP
MAX3465ESD	-40°C to +85°C	14 SO
MAX3465EPD	-40°C to +85°C	14 Plastic DIP

Ordering Information continued at end of data sheet.

Devices are also available in a lead(Pb)-free/RoHS-compliant package. Specify lead-free by adding "+" to the part number when ordering.

Pin Configurations appear at end of data sheet.

Selector Guide

PART NUMBER	HALF/FULL DUPLEX	RECEIVER/DRIVER ENABLE	LOW-POWER SHUTDOWN	HOT SWAP	RECEIVER/DRIVER PHASE SELECT	INDEPENDENT SHDN PIN	PIN COUNT
MAX3465	Full	Yes	Yes	Yes	Yes	Yes	14
MAX3466	Full	Yes	Yes	No	Yes	Yes	14
MAX3467	Full	No	No	No	No	No	8
MAX3468	Half	Yes	Yes	Yes	No	No	8
MAX3469	Half	Yes	Yes	No	No	No	8

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V _{CC}) to GND-0.3V to +6V	SO (derate 8.33mW/°C above +70°C)667mW
Control Input Voltage (\overline{RE} , DE, DI, SHDN, TXP, RXP) to GND-0.3V to (V _{CC} + 0.3V)	DIP (derate 10mW/°C above +70°C)800mW
Driver Output Voltage (Y, Z) to GND-8V to +13V	Operating Temperature Range	
Receiver Input Voltage (A, B) to GND-8V to +13V	MAX346_C_0°C to +70°C
Differential Driver Output Voltage (Y - Z)±8V	MAX346_E_-40°C to +85°C
Differential Receiver Input (A - B)±8V	Junction Temperature+150°C
Receiver Output Voltage (RO) to GND-0.3V to (V _{CC} + 0.3V)	Storage Temperature Range-65°C to +150°C
Output Driver Current (Y, Z)±250mA	Lead Temperature (soldering, 10s)+300°C
Continuous Power Dissipation (T _A = +70°C)		Soldering Temperature (reflow)	
SO (derate 5.88mW/°C above +70°C)471mW	Lead(Pb)-Free+260°C
DIP (derate 9.09mW/°C above +70°C)727mW	Containing Lead(Pb)+240°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +5V and T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power-Supply Range	V _{CC}		4.75		5.25	V
DRIVER						
Differential Driver Output (No Load)	V _{OD}	Figure 5, R = ∞			V _{CC}	V
Differential Driver Output	V _{OD}	Figure 5, R = 27Ω	2.1			V
Change in Magnitude of Differential Output Voltage	ΔV _{OD}	Figure 5, R = 50Ω or 27Ω (Note 2)			0.2	V
Driver Common-Mode Output Voltage	V _{OC}	Figure 5, R = 50Ω or 27Ω			3	V
Change in Magnitude of Common-Mode Voltage	ΔV _{OC}	Figure 5, R = 50Ω or 27Ω (Note 2)			0.2	V
Input High Voltage	V _{IH}	DE, DI, \overline{RE} , SHDN	2.0			V
Input Low Voltage	V _{IL}	DE, DI, \overline{RE} , SHDN			0.8	V
Input Hysteresis	V _{HYS}	DE, DI, \overline{RE} , SHDN		50		mV
Output Leakage (Y and Z) Full Duplex	I _O	DE = GND, V _{CC} = GND or +5.25V			+125	μA
					-100	
Input Current	I _{IN}	DI, \overline{RE} , DE, SHDN			±1	μA
Pulldown Current		RXP = TXP = V _{CC}	5	15	30	μA
Driver Short-Circuit Output Current (Note 3)	I _{OSD}	0 ≤ V _{OUT} ≤ +12V, output low			+250	mA
		-7V ≤ V _{OUT} ≤ V _{CC} , output high	-250			
Driver Short-Circuit Foldback Output Current (Note 3)	I _{OSFD}	(V _{CC} - 1V) ≤ V _{OUT} ≤ +12V, output low	+25			mA
		-7V ≤ V _{OUT} ≤ +1V, output high			-25	
Thermal Shutdown Threshold				140		°C
RECEIVER						
Differential Input Capacitance	C _{A, B}	Between A and B		8		pF
Input Current (A and B) Full Duplex	I _{A, B}	DE = GND, V _{CC} = GND or +5.25V			+250	μA
					-200	

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ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} = +5V \pm 5\%$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $V_{CC} = +5V$ and $T_A = +25^\circ C$.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
Receiver Differential Threshold Voltage	V_{TH}	$-7V \leq V_{CM} \leq +12V$	-200	-125	-50	mV	
Receiver Input Hysteresis	ΔV_{TH}	$V_{CM} = 0$	20			mV	
Receiver Output High Voltage	V_{OH}	$I_O = -4mA, V_A - V_B = V_{TH}$	$V_{CC} - 1.5$			V	
Receiver Output Low Voltage	V_{OL}	$I_O = 4mA, V_B - V_A = V_{TH}$	0.4			V	
Three-State Output Current at Receiver	I_{OZR}	$0 \leq V_O \leq V_{CC}$	± 1			μA	
Receiver Input Resistance	R_{IN}	$-7V \leq V_{CM} \leq +12V$	48			$k\Omega$	
Receiver Output Short-Circuit Current	I_{OSR}	$0 \leq V_{RO} \leq V_{CC}$	± 7			± 95 mA	
ESD Protection		A, B, Y, and Z pins (MAX3467/MAX3468/MAX3469)	± 6			kV	
SUPPLY CURRENT							
Normal Operation (Static Condition)	I_Q	No load, $DI = V_{CC}$ or $DI = GND$	2.5			4 mA	
Supply Current in SHDN	I_{SHDN}	$DE = GND$ and $\overline{RE} = V_{CC}$, or $SHDN = V_{CC}$	1			10 μA	
SWITCHING CHARACTERISTICS							
Driver Propagation Delay	t_{PLH}	Figures 6 and 7, $R_{DIFF} = 54\Omega$, $C_L = 50pF$				15	ns
	t_{PHL}						
Driver Differential Output Rise or Fall Time	t_R	Figures 6 and 7, $R_{DIFF} = 54\Omega$, $C_L = 50pF$				10	ns
	t_F						
Driver Output Skew $ t_{PLH} - t_{PHL} $	t_{SKEW}	Figures 6 and 7, $R_{DIFF} = 54\Omega$, $C_L = 50pF$, $TXP = GND$ or open				2	ns
Driver Output Transition Skew		Guaranteed by design				1	ns
Maximum Data Rate			30	40		Mbps	
Driver Enable to Output High	t_{ZH}	Figures 8 and 9, S2 closed, $R_L = 500\Omega$, $C_L = 50pF$				30	ns
Driver Enable to Output Low	t_{ZL}	Figures 8 and 9, S1 closed, $R_L = 500\Omega$, $C_L = 50pF$				30	ns
Driver Disable Time from Low	t_{LZ}	Figures 8 and 9, S1 closed, $R_L = 500\Omega$, $C_L = 50pF$				30	ns
Driver Disable to Output High	t_{HZ}	Figures 8 and 9, S2 closed, $R_L = 500\Omega$, $C_L = 50pF$				30	ns
Driver Enable Skew Time	$ t_{ZL} - t_{ZH} $	$R_L = 500\Omega$, $C_L = 50pF$, S1 closed (Figures 8 and 9), output low				5	ns
Driver Disable Skew Time	$ t_{ZL} - t_{ZH} $	$R_L = 500\Omega$, $C_L = 50pF$, S2 closed (Figures 8 and 9), output high				5	ns
Receiver Propagation Delay	t_{PLH}	Figure 10, $C_L = 15pF$ (Note 4)				20	ns
	t_{PHL}						

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ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} = +5V \pm 5\%$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $V_{CC} = +5V$ and $T_A = +25^\circ C$.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Receiver Output Skew	$ t_{PLH} - t_{PHL} $	Figure 10, $C_L = 15pF$, RXP = GND or open (Note 4)			2	ns
Receiver Enable to Output Low	t_{ZL}	Figures 8 and 11, $R_L = 1k\Omega$, $C_L = 15pF$, S1 closed (Note 4)			30	ns
Receiver Enable to Output High	t_{ZH}	Figures 8 and 11, $R_L = 1k\Omega$, $C_L = 15pF$, S2 closed (Note 4)			30	ns
Receiver Disable Time from Low	t_{LZ}	Figures 8 and 11, $R_L = 1k\Omega$, $C_L = 15pF$, S1 closed (Note 4)			30	ns
Receiver Disable Time from High	t_{HZ}	Figures 8 and 11, $R_L = 1k\Omega$, $C_L = 15pF$, S2 closed (Note 4)			30	ns
Time to Shutdown	t_{SHDN}	(Note 5)	50		800	ns
Driver Enable from Shutdown to Output High	$t_{ZH} (SHDN)$	Figures 8 and 9, $R_L = 500\Omega$, $C_L = 50pF$, S2 closed (Note 5)			4	μs
Driver Enable from Shutdown to Output Low	$t_{ZL} (SHDN)$	Figures 8 and 9, $R_L = 500\Omega$, $C_L = 50pF$, S1 closed (Note 5)			4	μs
Receiver Enable from Shutdown to Output High	$t_{ZH} (SHDN)$	Figures 8 and 11, $R_L = 1k\Omega$, $C_L = 15pF$, S2 closed (Notes 4, 5)			4	μs
Receiver Enable from Shutdown to Output Low	$t_{ZL} (SHDN)$	Figures 8 and 11, $R_L = 1k\Omega$, $C_L = 15pF$, S1 closed (Notes 4, 5)			4	μs

Note 1: All currents into the device are positive; all currents out of the device are negative. All voltages are referenced to device ground, unless otherwise noted.

Note 2: ΔV_{OD} and ΔV_{OC} are the changes in V_{OD} and V_{OC} , respectively, when the DI input changes state.

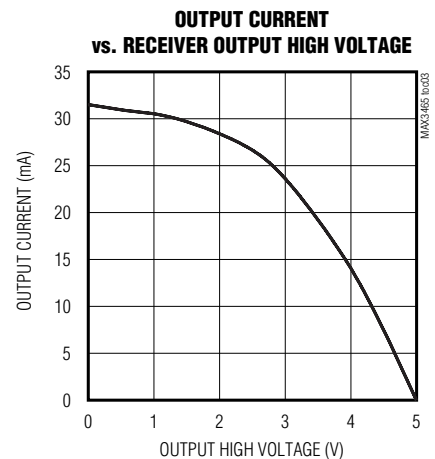
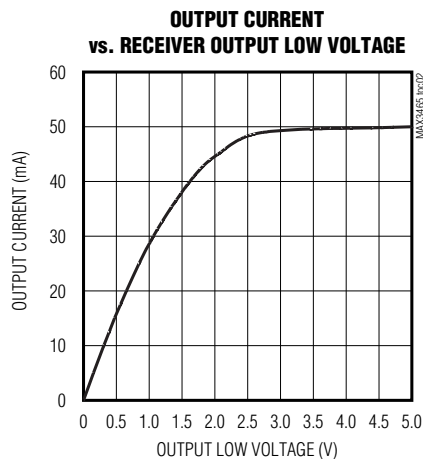
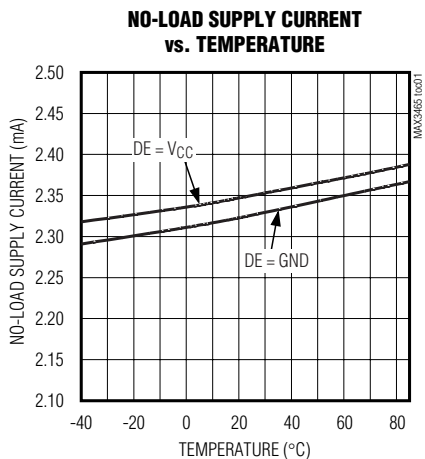
Note 3: The short-circuit output current applies to peak current just prior to foldback-current limiting; the short-circuit foldback output current applies during current limiting to allow a recovery from bus contention.

Note 4: Capacitive load includes test probe and fixture capacitance.

Note 5: Shutdown is enabled by bringing \overline{RE} high and DE low or by bringing SHDN high. If the enable inputs are in this state for less than 50ns, the device is guaranteed not to enter shutdown. If the enable inputs are in this state for at least 800ns, the device is guaranteed to have entered shutdown.

Typical Operating Characteristics

($V_{CC} = +5V$, $T_A = +25^\circ C$, unless otherwise noted.)

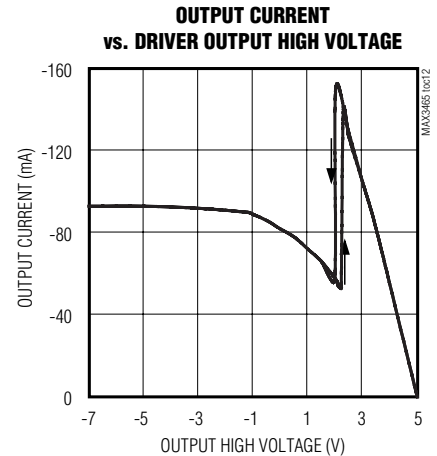
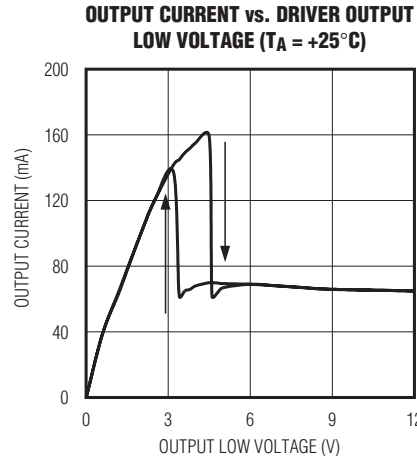
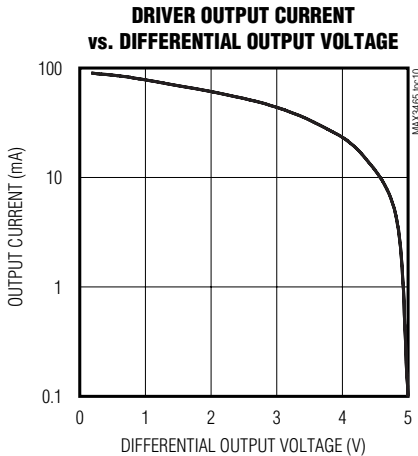
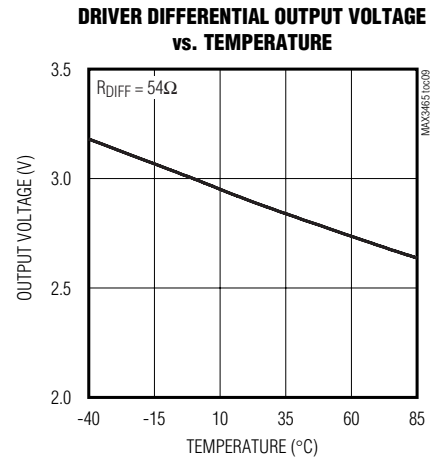
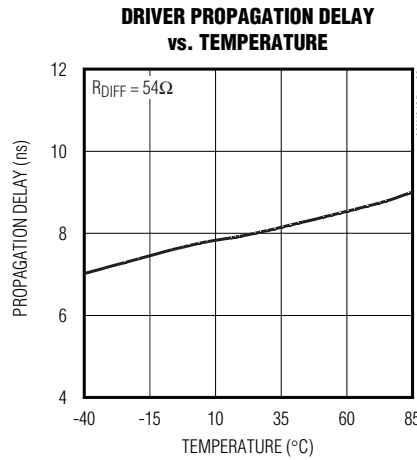
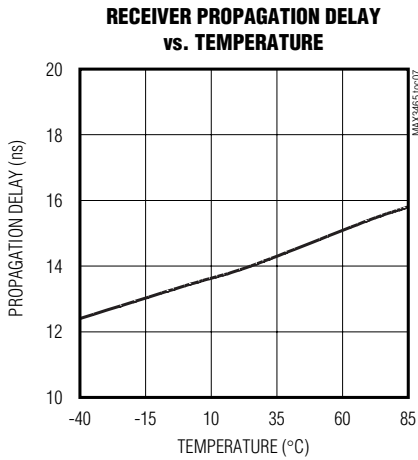
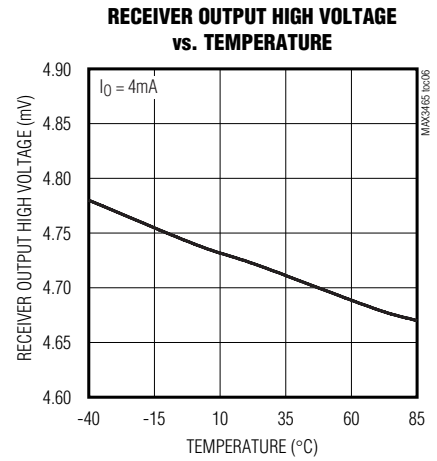
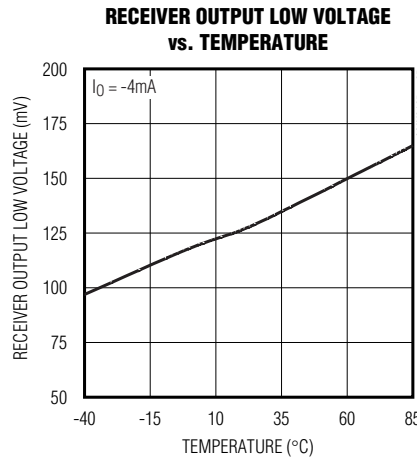
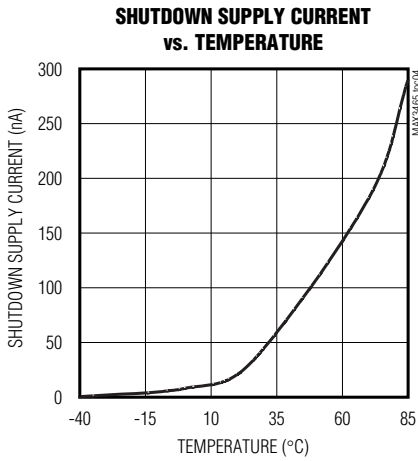


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Typical Operating Characteristics (continued)

($V_{CC} = +5V$, $T_A = +25^\circ C$, unless otherwise noted.)

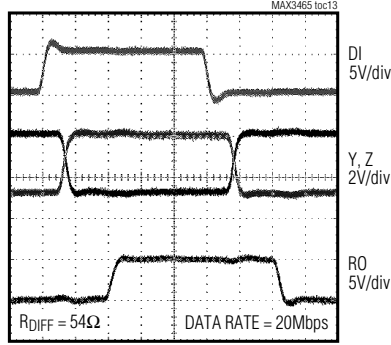


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Typical Operating Characteristics (continued)

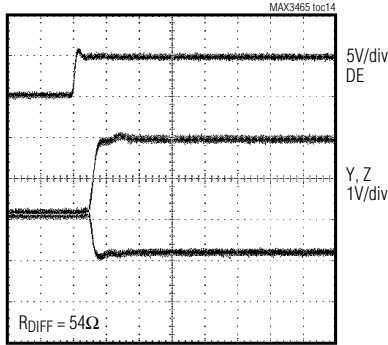
(V_{CC} = +5V, T_A = +25°C, unless otherwise noted.)

**DRIVER AND RECEIVER
PROPAGATION DELAYS**



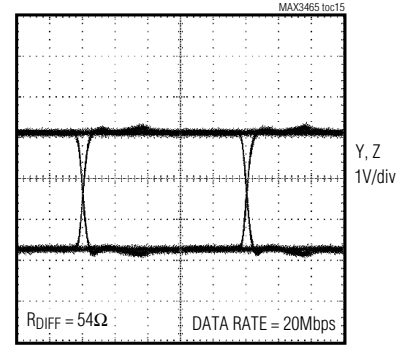
10ns/div

ENABLE RESPONSE TIME



20ns/div

EYE DIAGRAM



10ns/div

Pin Description

PIN			NAME	FUNCTION
FULL DUPLEX		HALF DUPLEX		
MAX3465/ MAX3466	MAX3467	MAX3468/ MAX3469		
1	—	—	SHDN	Shutdown. Drive SHDN high to enter low-power shutdown mode.
2	2	1	RO	Receiver Output. When \overline{RE} is low and $(A - B) \geq -50\text{mV}$, RO is high; if $(A - B) \leq -200\text{mV}$, RO is low.
3	—	2	\overline{RE}	Receiver Output Enable. Drive \overline{RE} low to enable RO; RO is high impedance when \overline{RE} is high. Drive \overline{RE} high and DE low to enter low-power shutdown mode.
4	—	3	DE	Driver Output Enable. Drive DE high to enable driver output. The driver outputs are high impedance when DE is low. Drive \overline{RE} high and DE low to enter low-power shutdown mode. Do not leave \overline{RE} unconnected when using the MAX3466 or MAX3469.
5	3	4	DI	Driver Input. With DE high, a low on DI forces the noninverting output low and the inverting output high. Similarly, a high on DI forces the noninverting output high and the inverting output low.
6, 7	4	5	GND	Ground
8	—	—	TXP	Transmitter Phase. Connect TXP to GND, or leave unconnected for normal transmitter phase/polarity. Connect TXP to V _{CC} to invert the transmitter phase/polarity. TXP has an internal 15μA pulldown.
9	5	—	Y	Noninverting Driver Output
10	6	—	Z	Inverting Driver Output
11	7	—	B	Inverting Receiver Input
12	8	—	A	Noninverting Receiver Input
13	—	—	RXP	Receiver Phase. Connect RXP to GND, or leave unconnected for normal receiver phase/polarity. Connect RXP to V _{CC} to invert the receiver phase/polarity. RXP has an internal 15μA pulldown.
14	1	8	V _{CC}	Positive Supply: $+4.75\text{V} \leq V_{CC} \leq +5.25\text{V}$. Bypass V _{CC} to GND with a 0.1μF capacitor.
—	—	7	B	Inverting Receiver Input and Inverting Driver Output
—	—	6	A	Noninverting Receiver Input and Noninverting Driver Output

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Function Tables

MAX3465-MAX3469

MAX3465/MAX3466

TRANSMITTING					
INPUTS				OUTPUTS	
\overline{RE}	DE	DI	SHDN	Z	Y
X	1	1	0	0	1
X	1	0	0	1	0
0	0	X	0	High-Z	High-Z
1	0	X	X	Shutdown	
X	X	X	1	Shutdown	
RECEIVING					
INPUTS				OUTPUT	
\overline{RE}	DE	A - B	SHDN	RO	
0	X	$\geq -0.05V$	0	1	
0	X	$\leq -0.2V$	0	0	
0	X	Open/Shorted	0	1	
1	1	X	0	High-Z	
1	0	X	X	Shutdown	
X	X	X	1	Shutdown	

MAX3467

TRANSMITTING		
INPUT	OUTPUTS	
DI	Z	Y
1	0	1
0	1	0
RECEIVING		
INPUTS		OUTPUT
A - B		RO
$\geq -0.05V$		1
$\leq -0.2V$		0
Open/Shorted		1

MAX3468/MAX3469

TRANSMITTING				
INPUTS			OUTPUTS	
\overline{RE}	DE	DI	B	A
X	1	1	0	1
X	1	0	1	0
0	0	X	High-Z	High-Z
1	0	X	Shutdown	
RECEIVING				
INPUTS			OUTPUT	
\overline{RE}	DE	A - B	RO	
0	X	$\geq -0.05V$	1	
0	X	$\leq -0.2V$	0	
0	X	Open/Shorted	1	
1	1	X	High-Z	
1	0	X	Shutdown	

+5V, Fail-Safe, 40Mbps, Profibus RS-485/ RS-422 Transceivers

Pin Configurations and Typical Operating Circuit

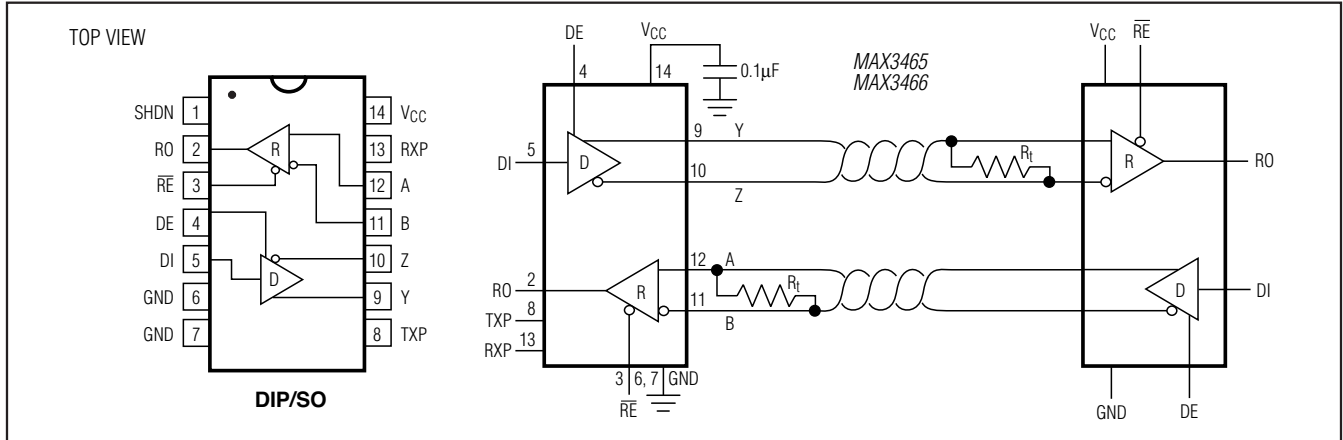


Figure 1. MAX3465/MAX3466 Pin Configuration and Typical Full-Duplex Operating Circuit

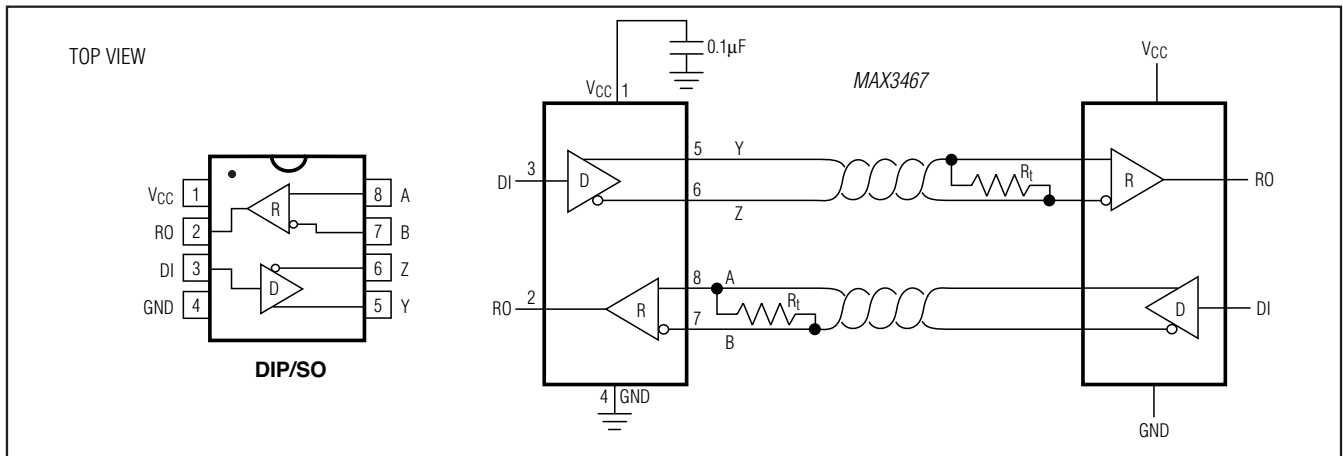


Figure 2. MAX3467 Pin Configuration and Typical Full-Duplex Operating Circuit

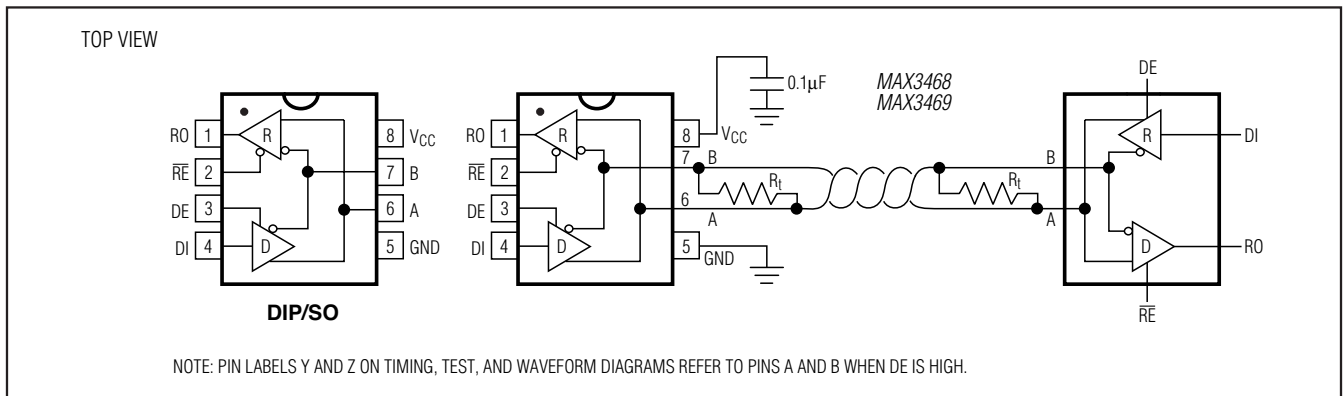


Figure 3. MAX3468/MAX3469 Pin Configuration and Typical Half-Duplex Operating Circuit

+5V, Fail-Safe, 40Mbps, Profibus RS-485/ RS-422 Transceivers

Detailed Description

The MAX3465–MAX3469 high-speed transceivers for RS-485/RS-422 communication contain one driver and one receiver. These devices feature true fail-safe circuitry, which guarantees a logic-high receiver output when the receiver inputs are open or shorted, or when they are connected to a terminated transmission line with all drivers disabled (see the *True Fail-Safe* section). The MAX3465–MAX3469's driver slew rates allow transmit speeds up to 40Mbps.

The MAX3468 and MAX3469 are half-duplex transceivers, while the MAX3465, MAX3466, and MAX3467 are full-duplex transceivers. All of these parts operate from a single +5V supply. Drivers are output short-circuit current limited. Thermal-shutdown circuitry protects drivers against excessive power dissipation. When activated, the thermal-shutdown circuitry places the driver outputs into a high-impedance state. The MAX3465 and MAX3468 devices have a hot-swap input structure that prevents disturbances on the differential signal lines when a circuit board is plugged into a hot backplane (see the *Hot-Swap Capability* section). All devices have output levels that are compatible with Profibus standards.

True Fail-Safe

The MAX3465–MAX3469 guarantee a logic-high receiver output when the receiver inputs are shorted or open, or when they are connected to a terminated transmission line with all drivers disabled. This is done by setting the receiver threshold between -50mV and -200mV. If the differential receiver input voltage (A - B) is greater than or equal to -50mV, RO is logic high. If A - B is less than or equal to -200mV, RO is logic low. In the case of a terminated bus with all transmitters disabled, the receiver's differential input voltage is pulled to 0V by the termination. With the receiver thresholds of the MAX3465–MAX3469, this results in a logic high with a 50mV minimum noise margin. Unlike previous true fail-safe devices, the -50mV to -200mV threshold complies with the $\pm 200\text{mV}$ EIA/TIA-485 standard.

Hot-Swap Capability

Hot-Swap Inputs

When circuit boards are inserted into a "hot" or powered backplane, disturbances to the enable and differential receiver inputs can lead to data errors. Upon initial circuit board insertion, the processor undergoes its power-up sequence. During this period, the processor output drivers are high impedance and are unable to drive the DE input of the MAX3465/MAX3468 to a

defined logic level. Leakage currents up to $10\mu\text{A}$ from the high-impedance output could cause DE to drift to an incorrect logic state. Additionally, parasitic circuit board capacitance could cause coupling of V_{CC} or GND to DE. These factors could improperly enable the driver.

When V_{CC} rises, an internal pulldown circuit holds DE low for around $15\mu\text{s}$. After the initial power-up sequence, the pulldown circuit becomes transparent, resetting the hot-swap-tolerable input.

Hot-Swap Input Circuitry

The MAX3465/MAX3468 enable inputs feature hot-swap capability. At the input there are two NMOS devices, M1 and M2 (Figure 4). When V_{CC} ramps from 0, an internal $15\mu\text{s}$ timer turns on M2 and sets the SR latch, which also turns on M1. Transistors M2, a 2mA current sink, and M1, a $100\mu\text{A}$ current sink, pull DE to GND through a $5.6\text{k}\Omega$ resistor. M2 is designed to pull DE to the disabled state against an external parasitic capacitance up to 100pF that can drive DE high. After $15\mu\text{s}$, the timer deactivates M2 while M1 remains on, holding DE low against three-state leakages that can drive DE high. M1 remains on until an external source overcomes the required input current. At this time, the SR latch resets and M1 turns off. When M1 turns off, DE reverts to a standard, high-impedance CMOS input. Whenever V_{CC} drops below 1V, the hot-swap input is reset.

For $\overline{\text{RE}}$ there is a complementary circuit employing two PMOS devices pulling to V_{CC} .

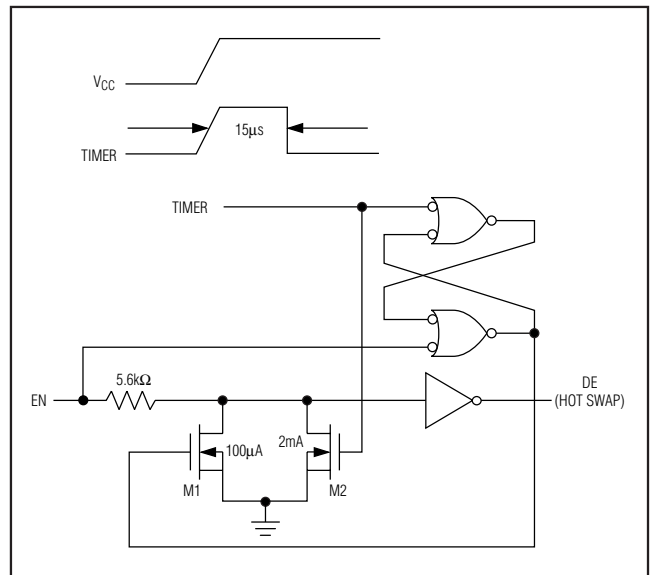


Figure 4. Simplified Structure of the Driver Enable Pin (DE)

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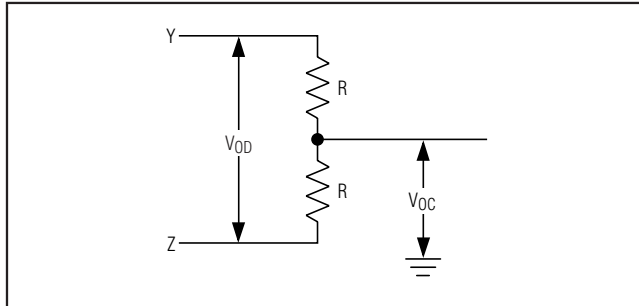


Figure 5. Driver DC Test Load

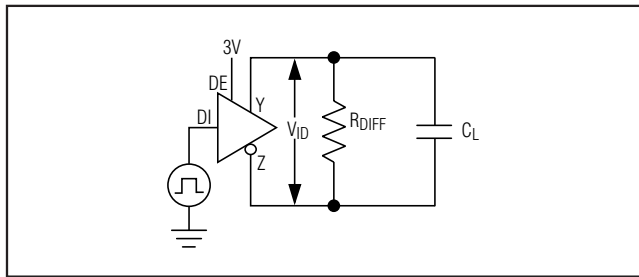


Figure 6. Driver Timing Test Circuit

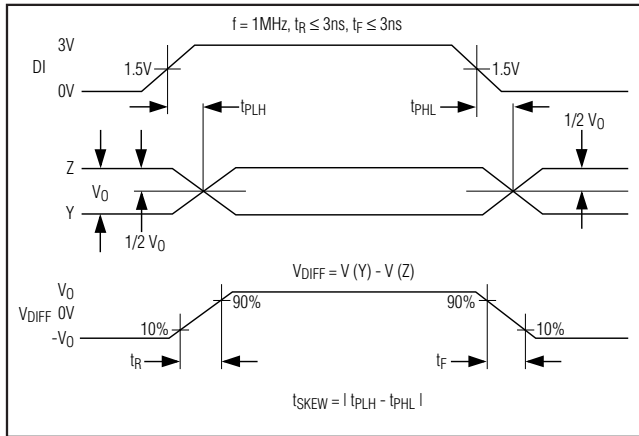


Figure 7. Driver Propagation Delays

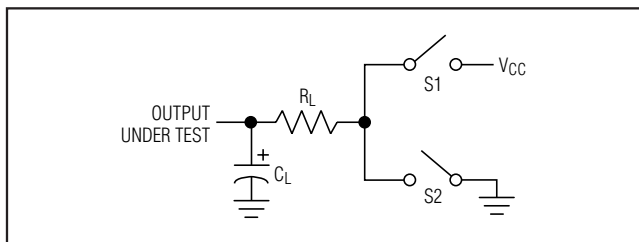


Figure 8. Enable/Disable Timing Test Load

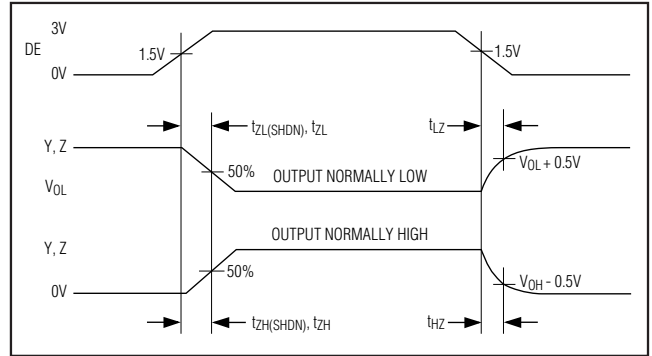


Figure 9. Driver Enable and Disable Times

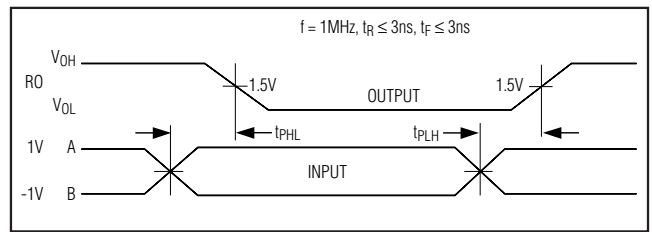


Figure 10. Receiver Propagation Delays

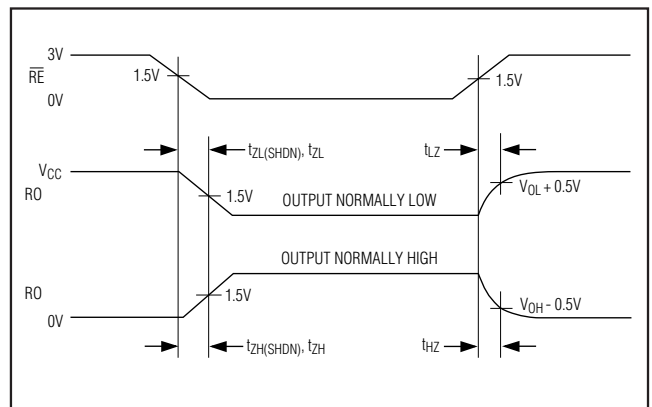


Figure 11. Receiver Enable and Disable Times

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MAX3465-MAX3469

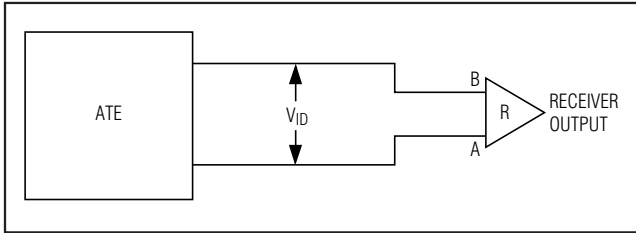


Figure 12. Receiver Propagation Delay Test Circuit

Applications Information

128 Transceivers on the Bus

The standard RS-485 receiver input impedance is 12k Ω (one unit load), and the standard driver can drive up to 32 unit loads. The MAX3465–MAX3469 family of transceivers has a 1/4-unit-load receiver input impedance (48k Ω), allowing up to 128 transceivers to be connected in parallel on one communication line. Any combination of these devices and/or other RS-485 transceivers with a total of 32 unit loads or less can be connected to the line.

Low-Power Shutdown Mode (Except MAX3467)

Low-power shutdown mode is initiated by bringing SHDN high (MAX3465/MAX3466), or both \overline{RE} high and DE low. In shutdown, the devices typically draw only 1 μ A of supply current. \overline{RE} and DE can be driven simultaneously; the devices are guaranteed not to enter shutdown if \overline{RE} is high and DE is low for less than 50ns. If the inputs are in this state for at least 800ns, the devices are guaranteed to enter shutdown.

Driver Output Protection

Two mechanisms prevent excessive output current and power dissipation caused by faults or by bus contention. The first, a foldback current limit on the output stage, provides immediate protection against short circuits over the whole common-mode voltage range (see the *Typical Operating Characteristics*). The second, a thermal-shutdown circuit, forces the driver outputs into a high-impedance state if the die temperature exceeds +140 $^{\circ}$ C.

Propagation Delay

Many digital encoding schemes depend on the difference between the driver and receiver propagation delay times. Typical propagation delays are shown in the *Typical Operating Characteristics*. The difference in receiver delay times, $t_{PLH} - t_{PHL}$, is a maximum of 2ns. The driver skew time $t_{PLH} - t_{PHL}$ is also a maximum of 2ns.

Typical Applications

The MAX3465–MAX3469 transceivers are designed for bidirectional data communications on multipoint bus transmission lines. Figures 13 and 14 show typical network applications circuits. To minimize reflections, the line should be terminated at both ends in its characteristic impedance, and stub lengths off the main line should be kept as short as possible.

Profibus Termination

The MAX3465–MAX3469 are designed for driving Profibus termination networks. With a worst-case loading of two termination networks with 220 Ω termination impedance and 390 Ω pullups and pulldowns, the drivers can drive $V_{A-B} > 2.1V$ output.

Chip Information

PROCESS: BiCMOS

Ordering Information (continued)

PART	TEMP RANGE	PIN-PACKAGE
MAX3466CSD	0 $^{\circ}$ C to +70 $^{\circ}$ C	14 SO
MAX3466CPD	0 $^{\circ}$ C to +70 $^{\circ}$ C	14 Plastic DIP
MAX3466ESD	-40 $^{\circ}$ C to +85 $^{\circ}$ C	14 SO
MAX3466EPD	-40 $^{\circ}$ C to +85 $^{\circ}$ C	14 Plastic DIP
MAX3467CSA	0 $^{\circ}$ C to +70 $^{\circ}$ C	8 SO
MAX3467CPA	0 $^{\circ}$ C to +70 $^{\circ}$ C	8 Plastic DIP
MAX3467ESA	-40 $^{\circ}$ C to +85 $^{\circ}$ C	8 SO
MAX3467EPA	-40 $^{\circ}$ C to +85 $^{\circ}$ C	8 Plastic DIP
MAX3468CSA	0 $^{\circ}$ C to +70 $^{\circ}$ C	8 SO
MAX3468CPA	0 $^{\circ}$ C to +70 $^{\circ}$ C	8 Plastic DIP
MAX3468ESA	-40 $^{\circ}$ C to +85 $^{\circ}$ C	8 SO
MAX3468EPA	-40 $^{\circ}$ C to +85 $^{\circ}$ C	8 Plastic DIP
MAX3469CSA	0 $^{\circ}$ C to +70 $^{\circ}$ C	8 SO
MAX3469CPA	0 $^{\circ}$ C to +70 $^{\circ}$ C	8 Plastic DIP
MAX3469ESA	-40 $^{\circ}$ C to +85 $^{\circ}$ C	8 SO
MAX3469EPA	-40 $^{\circ}$ C to +85 $^{\circ}$ C	8 Plastic DIP

Devices are also available in a lead(Pb)-free/RoHS-compliant package. Specify lead-free by adding "+" to the part number when ordering.

+5V, Fail-Safe, 40Mbps, Profibus RS-485/ RS-422 Transceivers

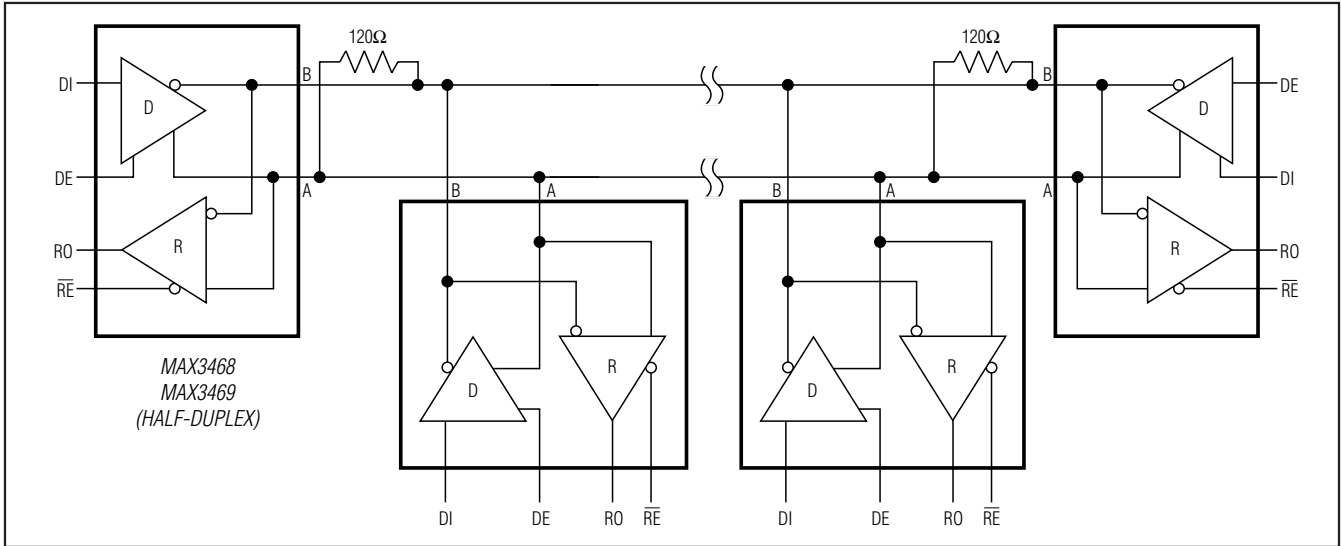


Figure 13. Typical Half-Duplex RS-485 Network

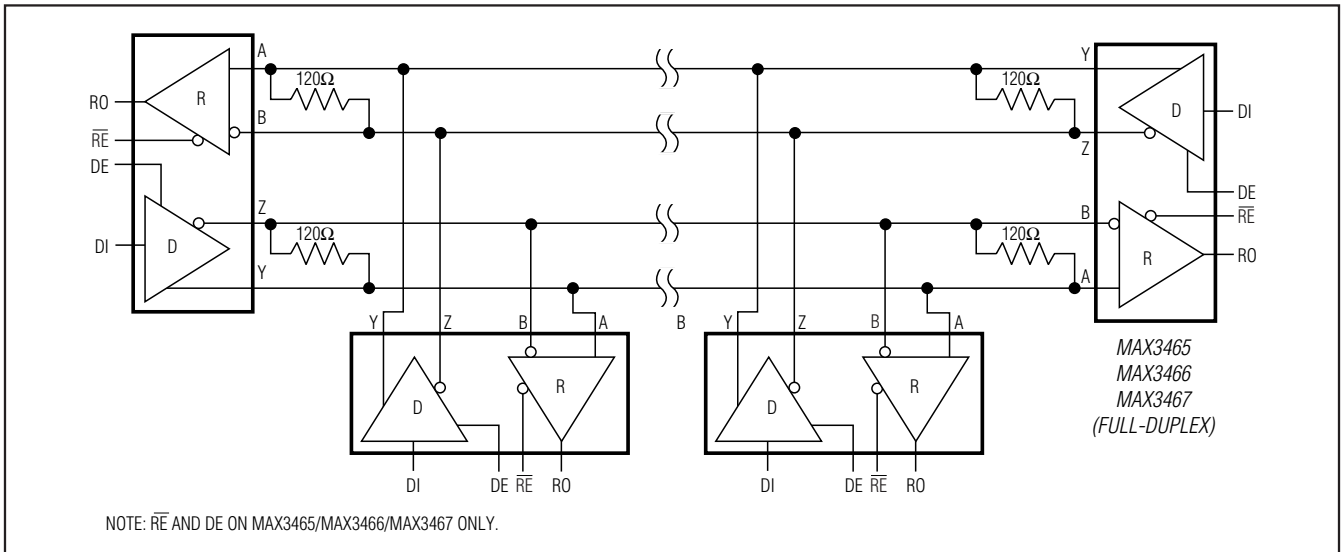


Figure 14. Typical Full-Duplex RS-485 Network

Package Information

For the latest package outline information and land patterns (footprints), go to www.maxim-ic.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
14 SO	S14-1	21-0041	90-0112
14 PDIP	P14-3	21-0043	—
8 SO	S8-2	21-0041	90-0096
8 PDIP	P8-1	21-0043	—

+5V, Fail-Safe, 40Mbps, Profibus RS-485/ RS-422 Transceivers

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/09	Initial release.	—
1	1/04	Updated the description for the DE pin in the <i>Pin Description</i> table.	6
2	8/09	Replaced TOC 11.	5
3	5/12	Added lead-free compliant packaging information, updated Figure 3 caption, updated package table	1, 8, 11, 12

MAX3465-MAX3469

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