MCP87055

High-Speed N-Channel Power MOSFET

Features

- Low Drain-to-Source On Resistance ($R_{DS(ON)}$)
- Low Total Gate Charge (Q_G) and Gate-to-Drain Charge (Q_{GD})
- Low Series Gate Resistance (R_G)
- Fast Switching
- Capable of Short Dead-Time Operation
- ROHS Compliant

Applications

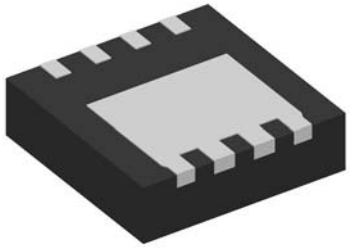
- Point-of-Load DC-DC Converters
- High Efficiency Power Management in Servers, Networking, and Automotive Applications

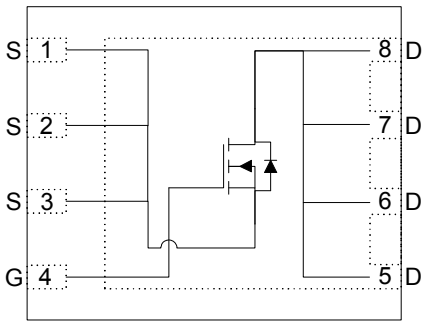
Description

The MCP87055 device is an N-Channel power MOSFET in a popular PDFN 3.3 mm x 3.3 mm package. Advanced packaging and silicon processing technologies allow the MCP87055 to achieve a low Q_G for a given $R_{DS(on)}$ value, resulting in a low Figure of Merit (FOM). Combined with low R_G, the low Figure of Merit of the MCP87055 allows high-efficiency power conversion with reduced switching and conduction losses.

Package Type

PDFN 3.3 x 3.3





Product Summary Table: Unless otherwise indicated, T_A = +25˚C						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Operating Characteristics						
Drain-to-Source Breakdown Voltage	BV_{DSS}	25	—	—	V	V_{GS} = 0V, I_D = 250 µA
Gate-to-Source Threshold Voltage	$V_{GS(TH)}$	1.1	1.35	1.7	V	V_{DS} = V_{GS}, I_D = 250 µA
Drain-to-Source On Resistance	$R_{DS(ON)}$	—	5.7	7	mΩ	V_{GS} = 4.5V, I_D = 20A
		—	4.7	6	mΩ	V_{GS} = 10V, I_D = 20A
Total Gate Charge	Q_G	—	11	14	nC	V_{DS} = 12.5V, I_D = 20A, V_{GS} = 4.5V
Gate-to-Drain Charge	Q_{GD}	—	4.5	—	nC	V_{DS} = 12.5V, I_D = 20A
Series Gate Resistance	R_G	—	2.1	—	Ω	
Thermal Characteristics						
Thermal Resistance Junction-to-X	$R_{\theta JX}$	—	—	66	˚C/W	**Note 1**
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	—	—	3.4	˚C/W	**Note 2**

Note 1: $R_{\theta JX}$ is determined with the device surface mounted on a 4-Layer FR4 PCB, with a 1” x 1” mounting pad of 2 oz. copper. This characteristic is dependent on user’s board design.

2: $R_{\theta JC}$ is determined using JEDEC 51-14 Method. This characteristic is determined by design.

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

V_{DS} .....+25V

V_{GS} ..... +10.0V / -8V

$I_{D,}$ Continuous .....60A, T_C = 25˚C

P_D ..... 1.8W, T_A = +25˚C

T_J, T_{STG}..... -55˚C to +150˚C

E_{AS} Avalanche Energy ..... 162 mJ

I_D = 18A, L = 1 mH, R_G = 25Ω

† Notice: Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C

Parameters	Sym	Min	Typ	Max	Units	Conditions
Static Characteristics						
Drain-to-Source Breakdown Voltage	B_{VDSS}	25	—	—	V	V_{GS} = 0V, I_D = 250 µA
Drain-to-Source Leakage Current	I_{DSS}	—	—	1	µA	V_{GS} = 0V, V_{DS} = 20V
Gate-to-Source Leakage Current	I_{GSS}	—	—	100	nA	V_{DS} = 0V, V_{GS} = 10V/-8V
Gate-to-Source Threshold Voltage	$V_{GS(TH)}$	1.1	1.35	1.7	V	V_{DS} = V_{GS}, I_D = 250 µA
Drain-to-Source On Resistance	$R_{DS(ON)}$	—	5.7	7	mΩ	V_{GS} = 4.5V, I_D = 20A
		—	4.7	6	mΩ	V_{GS} = 10V, I_D = 20A
Transconductance	g_{fs}	—	92	—	S	V_{DS} = 12.5V, I_D = 20A
Dynamic Characteristics						
Input Capacitance	C_{ISS}	—	890	—	pF	V_{GS} = 0V, V_{DS} = 12.5V, f = 1 MHz
Output Capacitance	C_{OSS}	—	420	—	pF	V_{GS} = 0V, V_{DS} = 12.5V, f = 1 MHz
Reverse Transfer Capacitance	C_{RSS}	—	114	—	pF	V_{GS} = 0V, V_{DS} = 12.5V, f = 1 MHz
Total Gate Charge	Q_G	—	11	14	nC	V_{DS} = 12.5V, I_D = 20A, V_{GS} = 4.5V
Gate-to-Drain Charge	Q_{GD}	—	4.5	—	nC	V_{DS} = 12.5V, I_D = 20A
Gate-to-Source Charge	Q_{GS}	—	1.8	—	nC	V_{DS} = 12.5V, I_D = 20A
Gate Charge at VTH	$Q_{G(TH)}$	—	1.1	—	nC	V_{DS} = 12.5V, I_D = 20A
Output Charge	Q_{OSS}	—	8	—	nC	V_{DS} = 12.5V, V_{GS} = 0
Turn-On Delay Time	$t_{d(on)}$	—	4.5	—	ns	V_{DS} = 12.5V, V_{GS} = 4.5V, I_D = 20A, R_G = 2Ω
Rise Time	t_r	—	11	—	ns	V_{DS} = 12.5V, V_{GS} = 4.5V, I_D = 20A, R_G = 2Ω
Turn-Off Delay Time	$t_{d(off)}$	—	9	—	ns	V_{DS} = 12.5V, V_{GS} = 4.5V, I_D = 20A, R_G = 2Ω
Fall Time	t_f	—	4.6	—	ns	V_{DS} = 12.5V, V_{GS} = 4.5V, I_D = 20A, R_G = 2Ω
Series Gate Resistance	R_G	—	2.1	—	Ω	

DC ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Diode Characteristics						
Diode Forward Voltage	V_{FD}	—	0.8	1	V	I_S = 20A, V_{GS} = 0V
Reverse Recovery Charge	Q_{RR}	—	18	—	nC	I_S = 20A, di/dt = 300 A/µs
Reverse Recovery Time	t_{rr}	—	15	—	ns	I_S = 20A, di/dt = 300 A/µs
Avalanche Characteristics						
Avalanche Energy	E_{AS}	50	—	—	mJ	I_D = 10A, L = 1 mH, R_G = 25Ω

TEMPERATURE CHARACTERISTICS

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Temperature Ranges						
Operating Junction Temperature Range	T_J	-55	—	150	°C	
Storage Temperature Range	T_A	-55	—	150	°C	
Package Thermal Resistances						
Thermal Resistance Junction-to-X, 8L 3.3x3.3-PDFN	$R_{\theta JX}$	—	—	66	°C/W	**Note 1**
Thermal Resistance Junction-to-Case, 8L 3.3x3.3-PDFN	$R_{\theta JC}$	—	—	3.4	°C/W	**Note 2**

Note 1: $R_{\theta JX}$ is determined with the device surface mounted on a 4-Layer FR4 PCB, with a 1" x 1" mounting pad of 2 oz. copper. This characteristic is dependent on user's board design.

2: $R_{\theta JC}$ is determined using JEDEC 51-14 Method. This characteristic is determined by design.

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, T_A = +25°C.

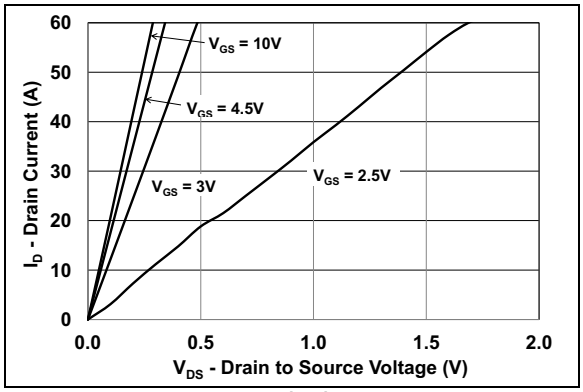


FIGURE 2-1: *Typical Output Characteristics.*

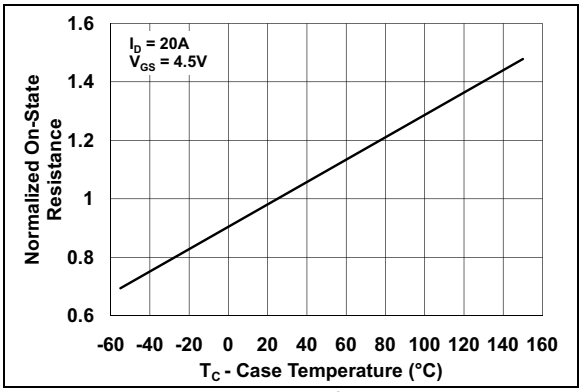


FIGURE 2-4: *On Resistance vs. Temperature.*

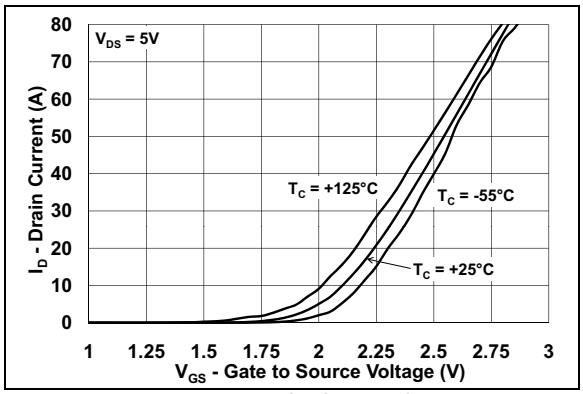


FIGURE 2-2: *Typical Transfer Characteristics.*

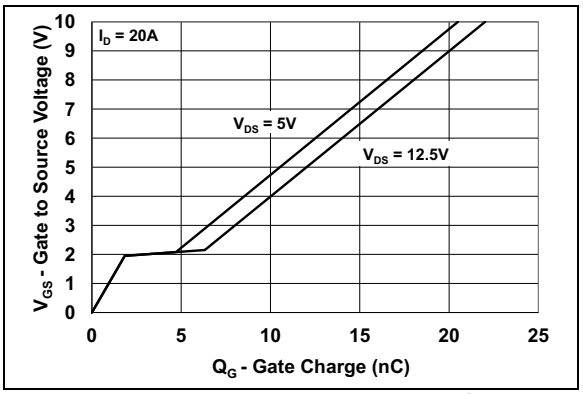


FIGURE 2-5: *Gate-to-Source Voltage vs. Gate Charge.*

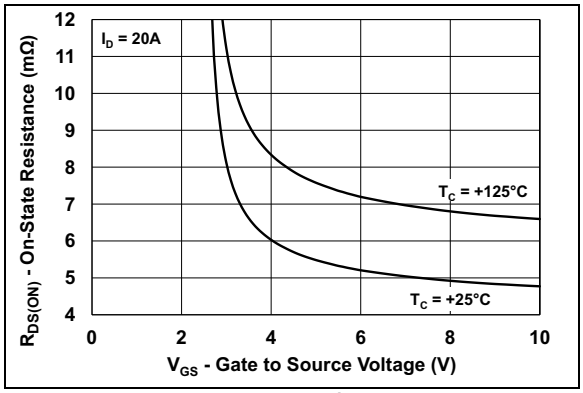


FIGURE 2-3: *On Resistance vs. Gate-to-Source Voltage.*

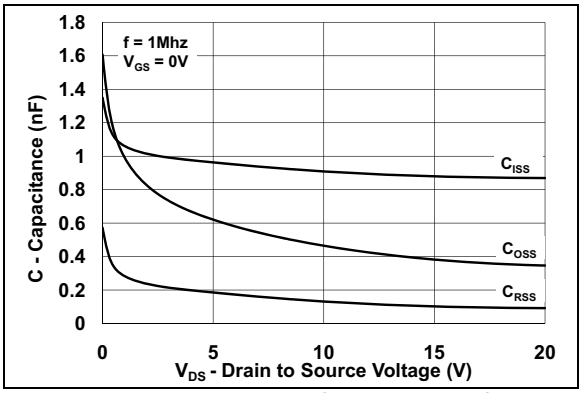


FIGURE 2-6: *Capacitance vs. Drain-to-Source Voltage.*

Note: Unless otherwise indicated, T_A = +25°C.

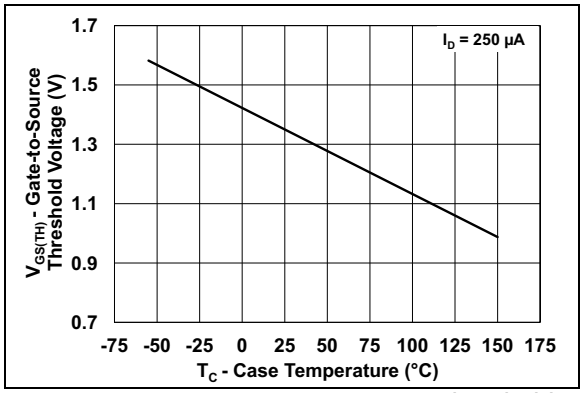


FIGURE 2-7: *Gate-to-Source Threshold Voltage vs. Temperature.*

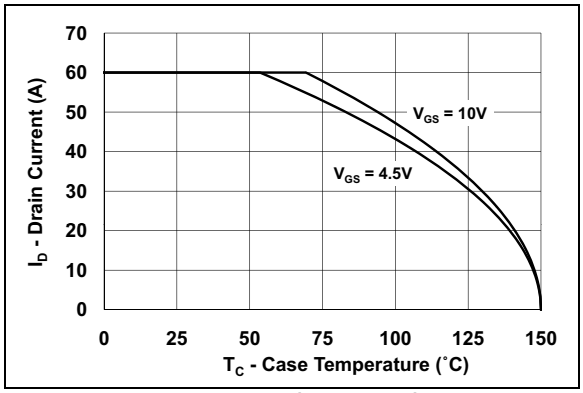


FIGURE 2-10: *Maximum Drain Current vs. Temperature.*

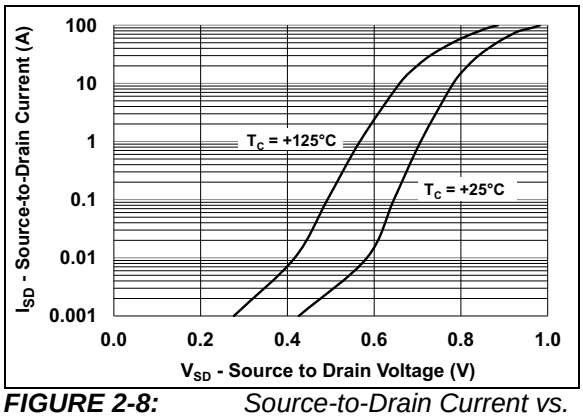


FIGURE 2-8: *Source-to-Drain Current vs. Source-to-Drain Voltage.*

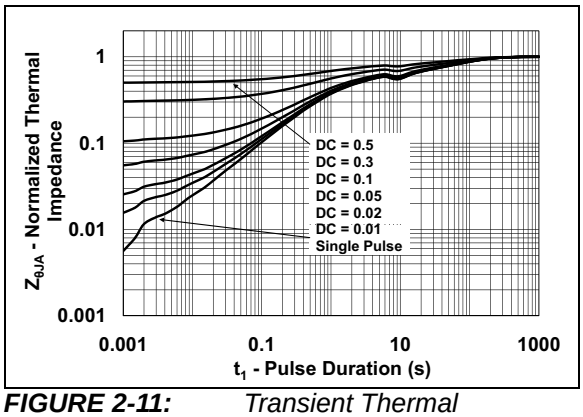


FIGURE 2-11: *Transient Thermal Impedance.*

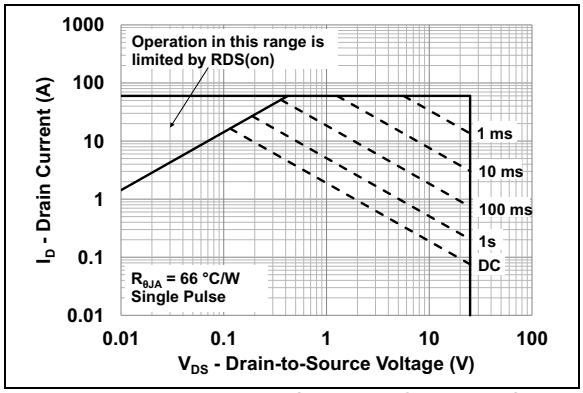


FIGURE 2-9: *Maximum Safe Operating Area.*

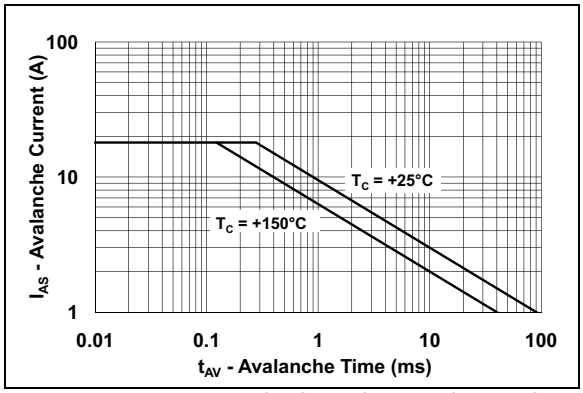


FIGURE 2-12: *Single-Pulse Unclamped Inductive Switching.*

Note: Unless otherwise indicated, T_A = +25°C.

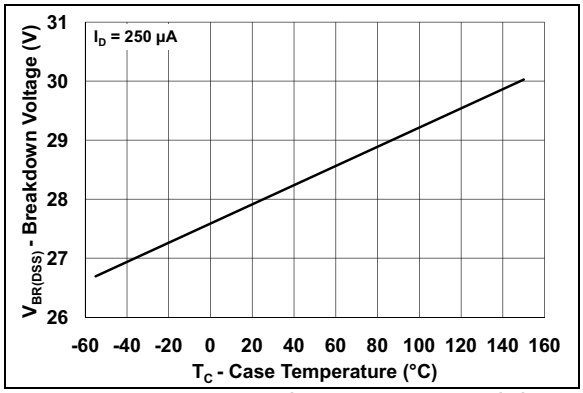


FIGURE 2-13: *Drain-to-Source Breakdown Voltage vs. Temperature.*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

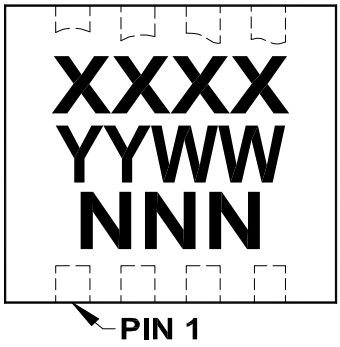
TABLE 3-1: PIN FUNCTION TABLE

MCP87055 3 x 3 PDFN	**Symbol**	**Description**
1, 2, 3	S	Source pin
4	G	Gate pin
5, 6, 7, 8	D	Drain pin, including exposed thermal pad

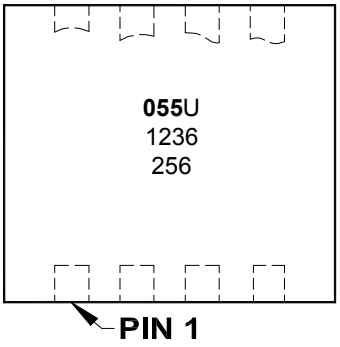
4.0 PACKAGING INFORMATION

4.1 Package Marking Information*

8-Lead PDFN (3.3 x 3.3 x 0.9 mm)



Example



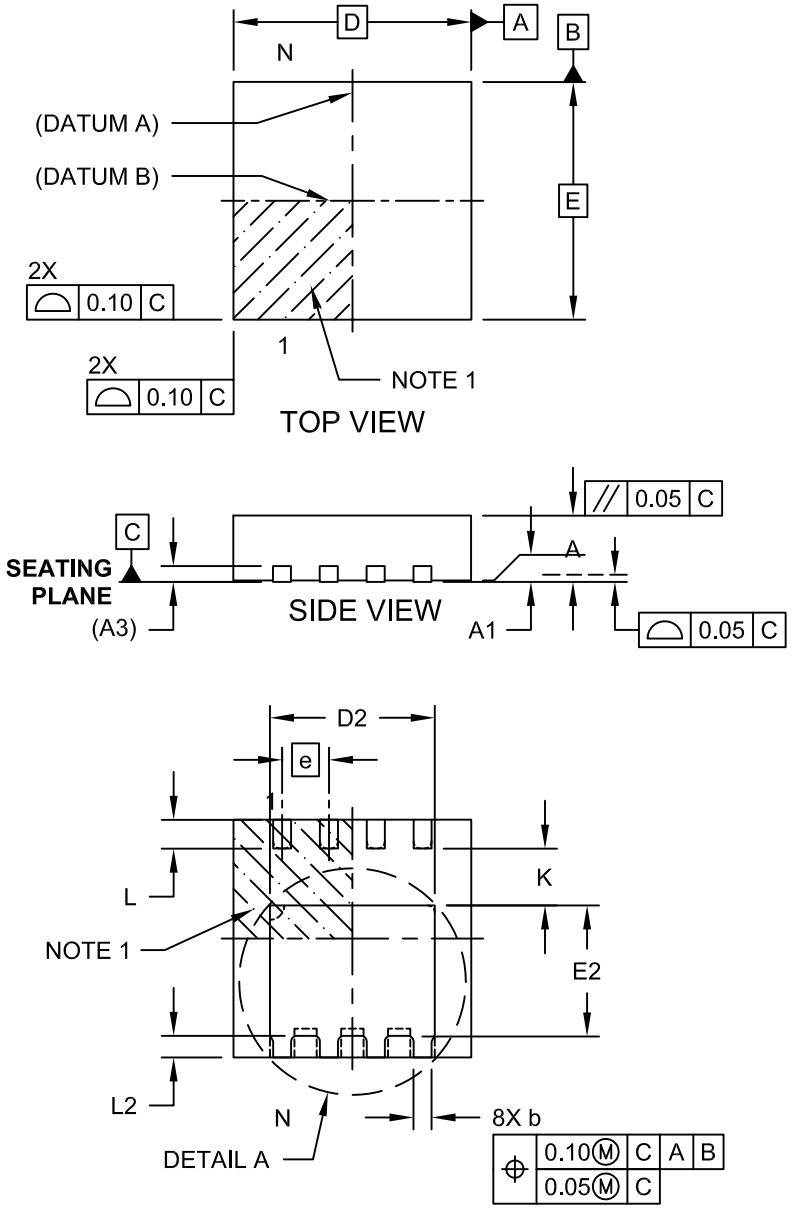
*RoHS compliant using EU-RoHS exemption: 7(a) - Lead in high-melting-temperature-type solders (i.e. lead-based alloys containing 85% by weight or more lead) can be found on the outer packaging for this package.

Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead Power Dual Flatpack No Lead Package (LC) – 3.3x3.3x1.0 mm Body [PDFN]

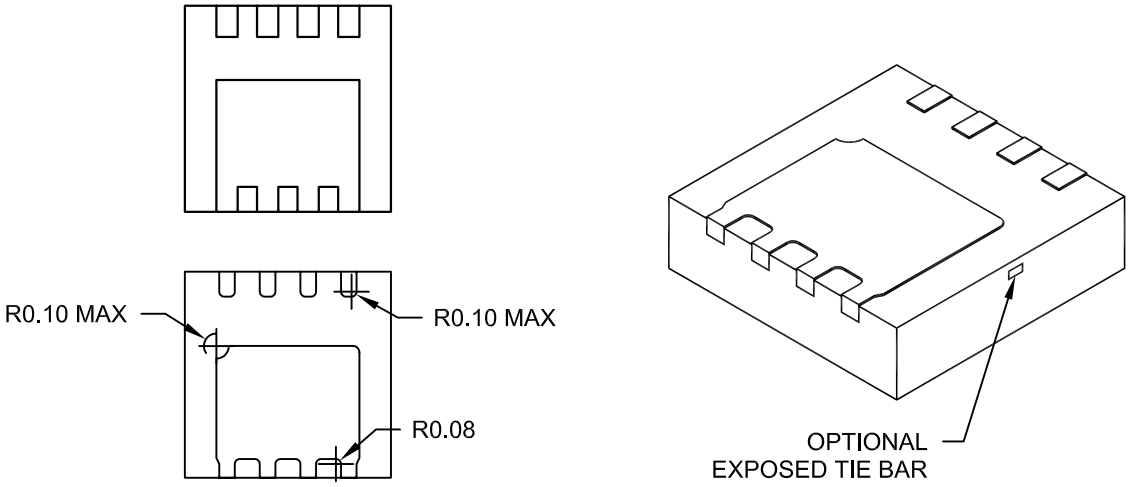
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-195A Sheet 1 of 2

8-Lead Power Dual Flatpack No Lead Package (LC) – 3.3x3.3x1.0 mm Body [PDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



DETAIL A
ALTERNATE EXPOSED PAD CONFIGURATIONS

	Units	MILLIMETERS		
Dimension	Limits	MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	1.00	1.03
Standoff	A1	0.00	-	0.05
Terminal Thickness	(A3)		0.20 REF	
Overall Length	D		3.30 BSC	
Overall Width	E		3.30 BSC	
Exposed Pad length	D2	2.14	2.29	2.39
Exposed Pad Width	E2	1.66	1.81	1.91
Terminal Width	b	0.25	0.30	0.35
Terminal Length	L	0.30	0.40	0.50
Terminal Length	L2	0.30	-	0.40
Terminal to Exposed Pad	K	0.60	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars.
3. Package is saw singulated.
4. Package dimension does not include mold flash, protrusions, burrs or metal smearing.
5. Dimensioning and tolerancing per ASME Y14.5M.

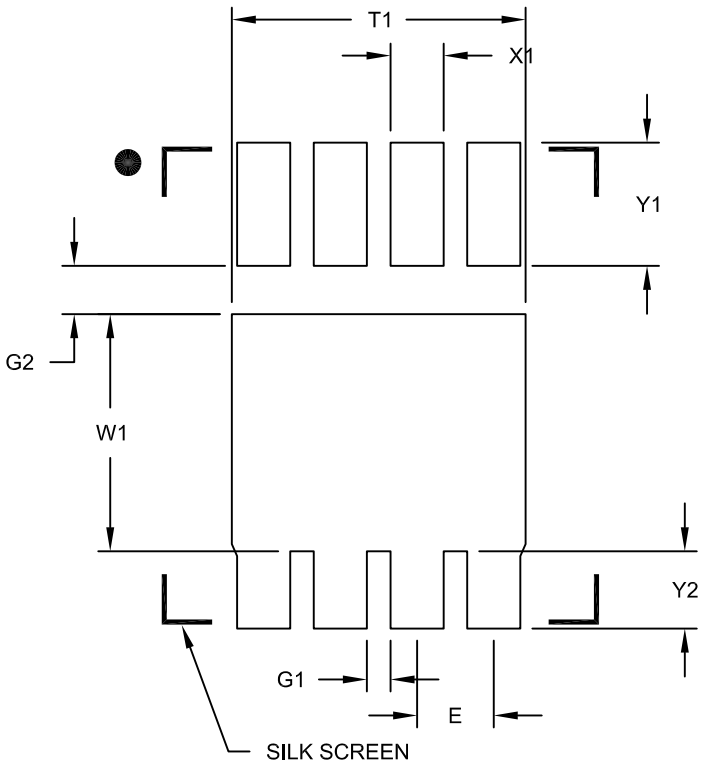
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-195A Sheet 2 of 2

8-Lead Power Dual Flatpack No Lead Package (LC) – 3.3x3.3x1.0 mm Body [PDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Center Pad Width	W1			2.01
Center Pad Length	T1			2.49
Distance Between Terminals	G1	0.20		
Terminal Edge to Center Pad	G2	0.41		
Terminal Pad Width (X8)	X1			0.45
Terminal Pad Length (X4)	Y1			1.05
Terminal Pad Length (X8)	Y2			0.66

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2195A

NOTES:

APPENDIX A: REVISION HISTORY

Revision B (November 2012)

- Updated the Gate-to-Source Charge value and the Gate Charge at VTH value in the **DC Electrical Characteristics** table.

Revision A (September 2012)

- Original Release of this Document.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XX
Device	Temperature Range	Package

Device:	MCP87055T:	High Speed N-Channel Power MOSFET (Tape and Reel)
Temperature Range:	U =	-55°C to +150°C (Ultra-High)
Package:	LC =	Power Dual Flatpack, No Lead Package (3.3x3.3x1.0 mm Body) (DFN), 8-lead

Examples:

a) MCP87055T-U/LC: Tape and Reel, Ultra-HighTemperature, 8LD DFN package

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QUALITY MANAGEMENT SYSTEM
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ISO/TS 16949

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