

P-Channel Enhancement-Mode Vertical DMOS FET

Features

- ▶ Free from secondary breakdown
- ▶ Low power drive requirement
- ▶ Ease of paralleling
- ▶ Low C_{ISS} and fast switching speeds
- ▶ High input impedance and high gain
- ▶ Excellent thermal stability
- ▶ Integral source-to-drain diode

Applications

- ▶ Motor controls
- ▶ Converters
- ▶ Amplifiers
- ▶ Switches
- ▶ Power supply circuits
- ▶ Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

General Description

The Supertex VP2450 is an enhancement-mode (normally-off) transistor that utilizes a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors, and the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Ordering Information

Device	Package Options		BV_{DSS}/BV_{DGS} (V)	$R_{DS(ON)}$ (max) (Ω)	$I_{D(ON)}$ (min) (mA)
	TO-92	TO-243AA (SOT-89)			
VP2450	VP2450N3-G	VP2450N8-G	-500	30	-200

-G indicates package is RoHS compliant ("Green")



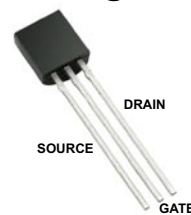
Absolute Maximum Ratings

Parameter	Value
Drain-to-Source voltage	BV_{DSS}
Drain-to-Gate voltage	BV_{DGS}
Gate-to-Source voltage	$\pm 20V$
Operating and storage temperature	$-55^{\circ}C$ to $+150^{\circ}C$
Soldering temperature*	$300^{\circ}C$

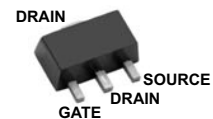
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

* Distance of 1.6mm from case for 10 seconds.

Pin Configurations

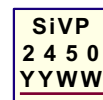


TO-92 (N3)



TO-243AA (SOT-89) (N8)

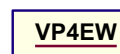
Product Marking



YY = Year Sealed
WW = Week Sealed
_____ = "Green" Packaging

Package may or may not include the following marks: Si or

TO-92 (N3)



W = Code for week sealed
_____ = "Green" Packaging

Packages may or may not include the following marks: Si or

TO-243AA (SOT-89) (N8)

Thermal Characteristics

Package	I_D (continuous) [†] (mA)	I_D (pulsed) (mA)	Power Dissipation @ $T_c = 25^\circ\text{C}$ (W)	θ_{jc} ($^\circ\text{C}/\text{W}$)	θ_{ja} ($^\circ\text{C}/\text{W}$)	I_{DR} [†] (mA)	I_{DRM} (mA)
TO-92	-100	-300	1.0	125	170	-100	-300
TO-243AA (SOT-89)	-160	-800	1.6 [‡]	15	78	-160	-800

[†] I_D (continuous) is limited by max rated T_j
[‡] Mounted on FR5 board, 25mm x 25mm x 1.57mm.

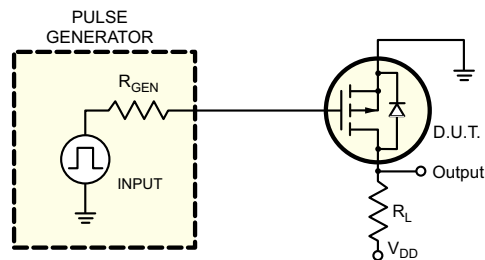
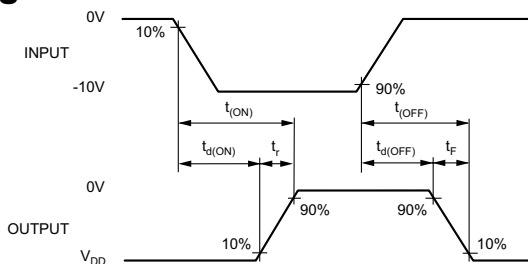
Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Sym	Parameter	Min	Typ	Max	Units	Conditions
BV_{DSS}	Drain-to-source breakdown voltage	-500	-	-	V	$V_{GS} = 0\text{V}, I_D = -250\mu\text{A}$
$V_{GS(th)}$	Gate threshold voltage	-1.5	-	-3.5	V	$V_{GS} = V_{DS}, I_D = -1.0\text{mA}$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with temperature	-	-	-4.8	mV/ $^\circ\text{C}$	$V_{GS} = V_{DS}, I_D = -1.0\text{mA}$
I_{GSS}	Gate body leakage	-	-	-100	nA	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$
I_{DSS}	Zero gate voltage drain current	-	-	-10	μA	$V_{GS} = 0\text{V}, V_{DS} = \text{Max Rating}$
		-	-	-1.0	mA	$V_{DS} = 0.8 \text{ Max Rating}, V_{GS} = 0\text{V}, T_A = 125^\circ\text{C}$
$I_{D(ON)}$	On-state drain current	-75	-	-	mA	$V_{GS} = -4.5\text{V}, V_{DS} = -15\text{V}$
		-200	-	-		$V_{GS} = -10\text{V}, V_{DS} = -15\text{V}$
$R_{DS(ON)}$	Static drain-to-source on-state resistance	-	-	35	Ω	$V_{GS} = -4.5\text{V}, I_D = -50\text{mA}$
		-	-	30		$V_{GS} = -10\text{V}, I_D = -100\text{mA}$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with temperature	-	-	0.75	%/ $^\circ\text{C}$	$V_{GS} = -10\text{V}, I_D = -100\text{mA}$
G_{FS}	Forward transconductance	150	320	-	mmho	$V_{DS} = -15\text{V}, I_D = -100\text{mA}$
C_{ISS}	Input capacitance	-	-	190	pF	$V_{GS} = 0\text{V}, V_{DS} = -25\text{V}, f = 1.0\text{MHz}$
C_{OSS}	Common source output capacitance	-	-	75		
C_{RSS}	Reverse transfer capacitance	-	-	20		
$t_{d(ON)}$	Turn-on delay time	-	-	10	ns	$V_{DD} = -25\text{V}, I_D = -200\text{mA}, R_{GEN} = 25\Omega$
t_r	Rise time	-	-	25		
$t_{d(OFF)}$	Turn-off delay time	-	-	45		
t_f	Fall time	-	-	25		
V_{SD}	Diode forward voltage drop	-	-	-1.8	V	$V_{GS} = 0\text{V}, I_{SD} = -100\text{mA}$
t_{rr}	Reverse recovery time	-	300	-	ns	$V_{GS} = 0\text{V}, I_{SD} = -100\text{mA}$

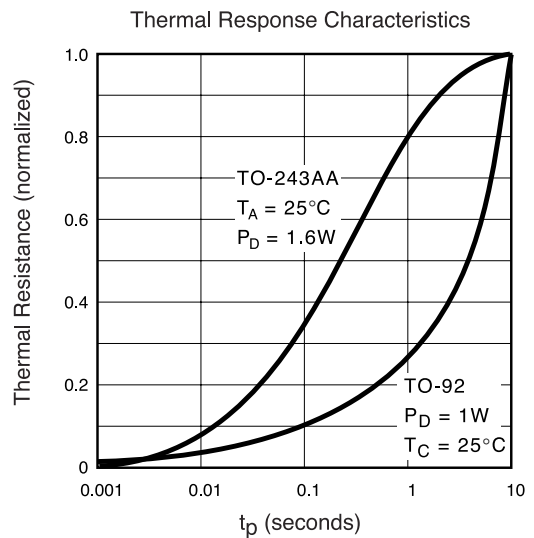
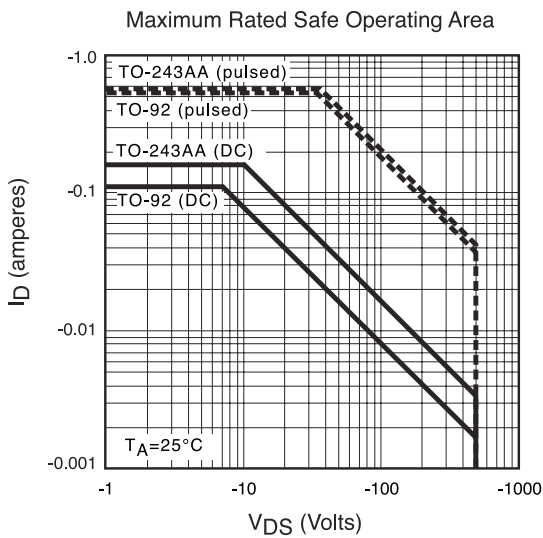
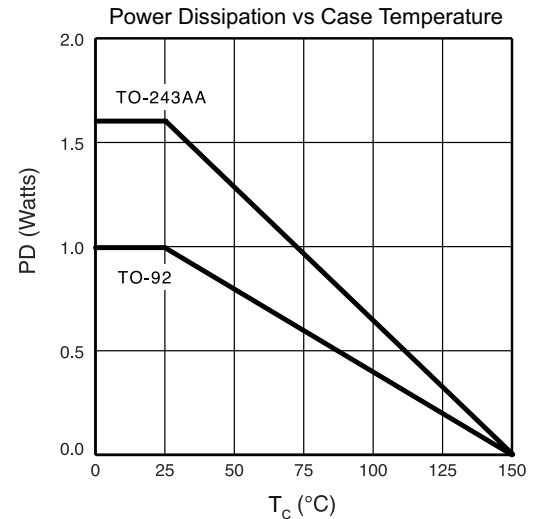
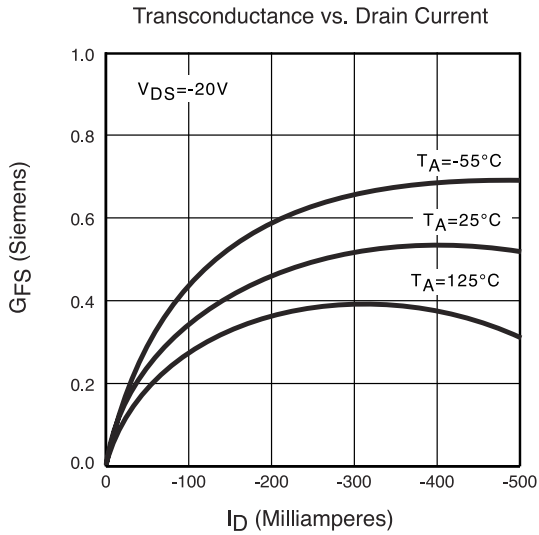
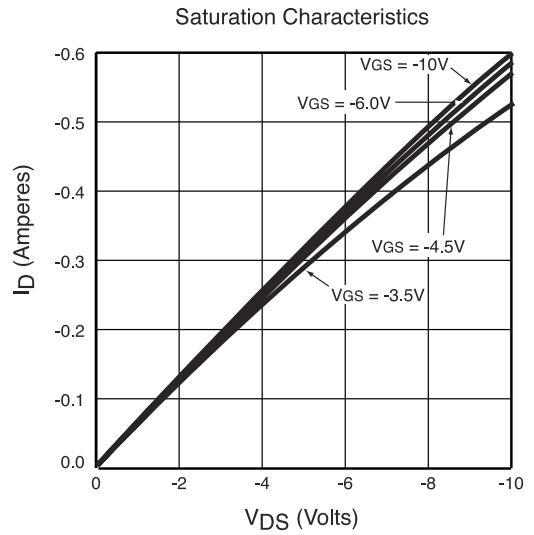
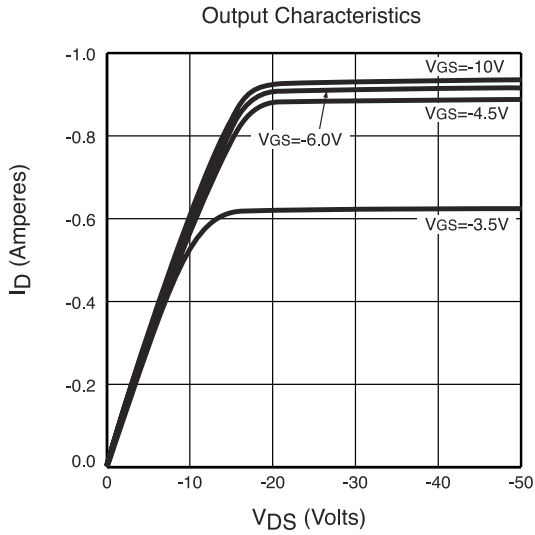
Notes:

1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300 μs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

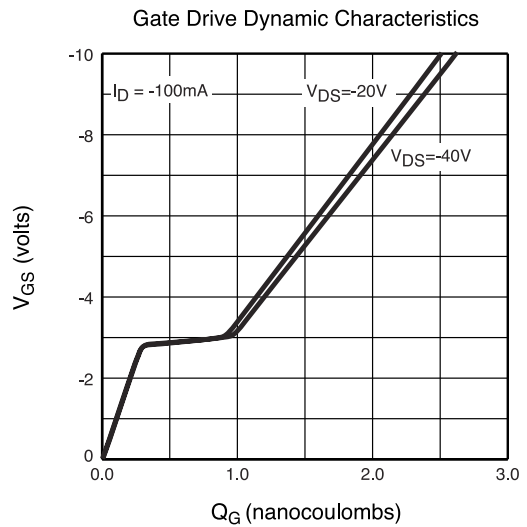
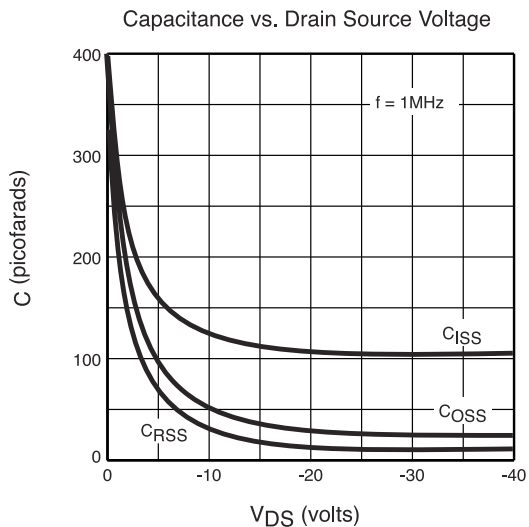
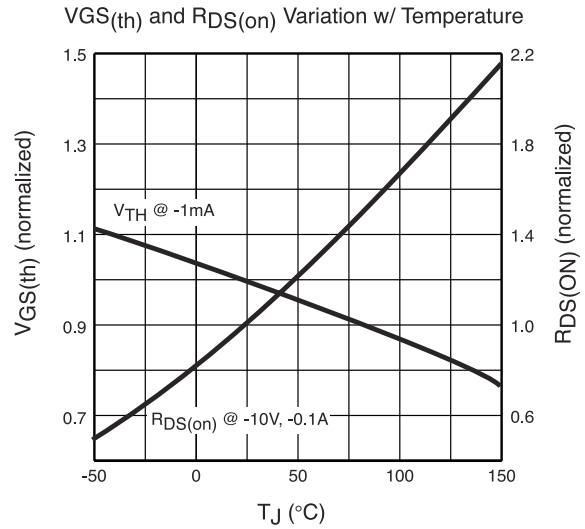
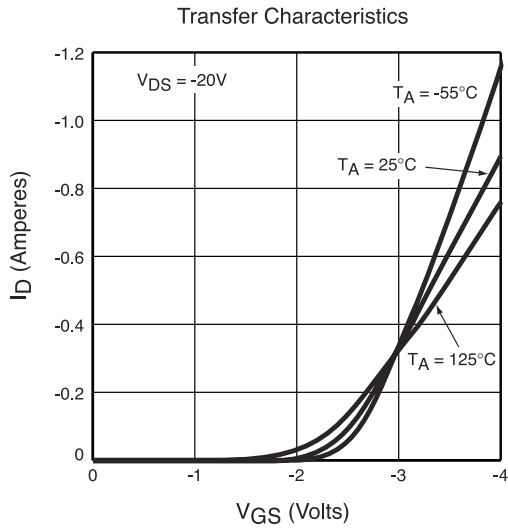
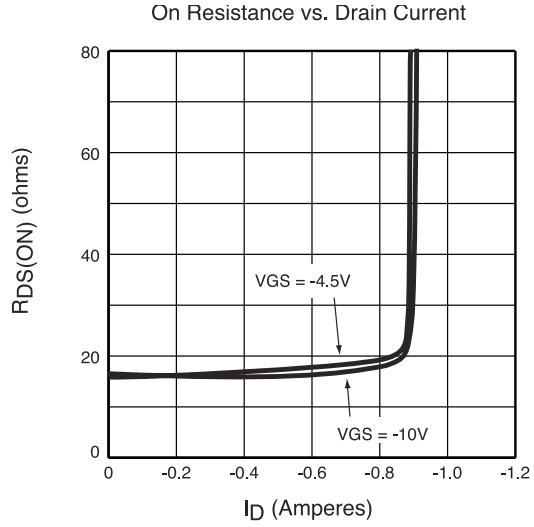
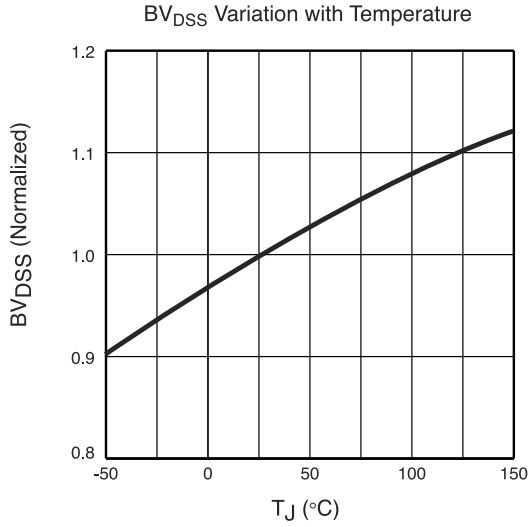
Switching Waveforms and Test Circuit



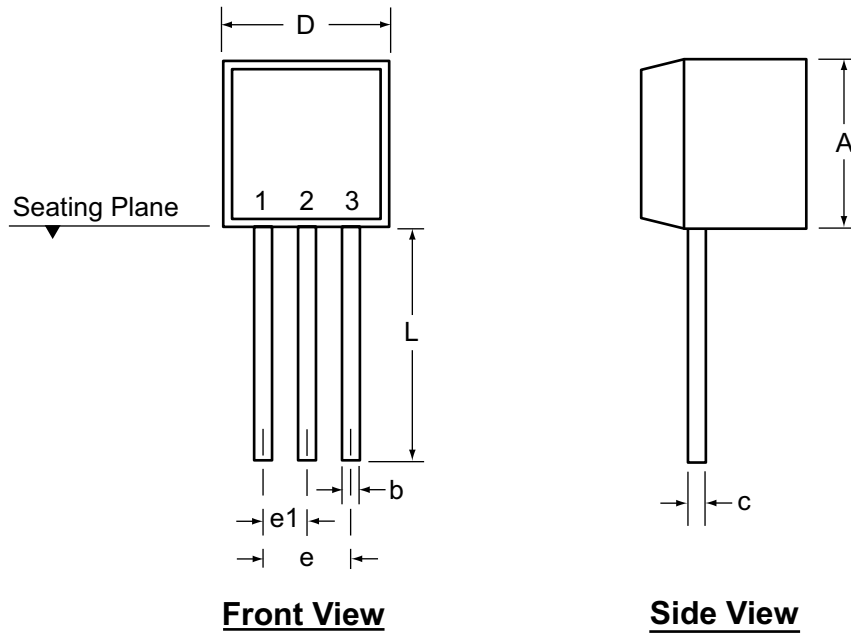
Typical Performance Curves



Typical Performance Curves (cont.)



3-Lead TO-92 Package Outline (N3)



Symbol		A	b	c	D	E	E1	e	e1	L
Dimensions (inches)	MIN	.170	.014 [†]	.014 [†]	.175	.125	.080	.095	.045	.500
	NOM	-	-	-	-	-	-	-	-	-
	MAX	.210	.022 [†]	.022 [†]	.205	.165	.105	.105	.055	.610*

JEDEC Registration TO-92.

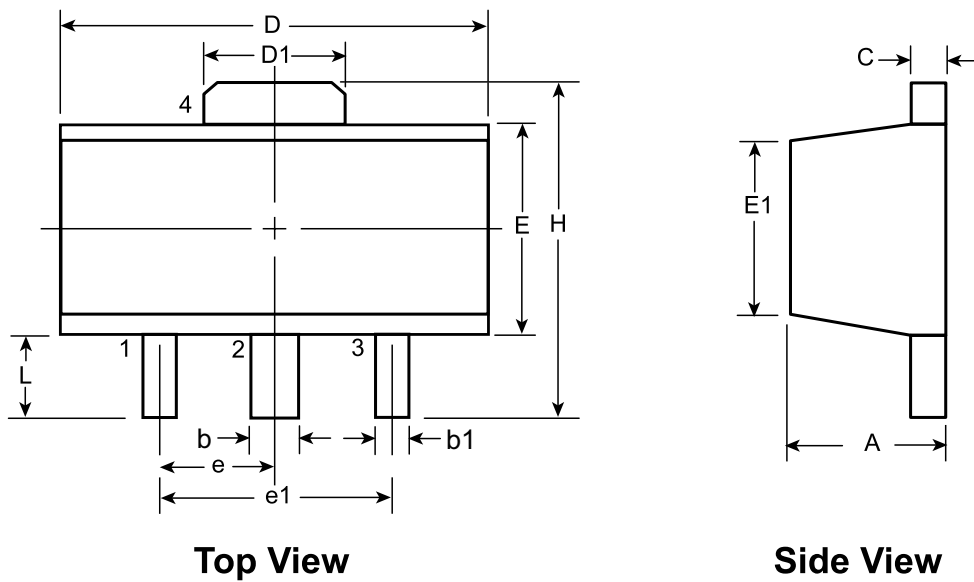
* This dimension is not specified in the original JEDEC drawing. The value listed is for reference only.

† This dimension is a non-JEDEC dimension.

Drawings not to scale.

Supertex Doc.#: DSPD-3TO92N3, Version D080408.

3-Lead TO-243AA (SOT-89) Package Outline (N8)



Top View

Side View

Symbol		A	b	b1	C	D	D1	E	E1	e	e1	H	L	
Dimensions (mm)	MIN	1.40	0.44	0.36	0.35	4.40	1.62	2.29	2.13	1.50 BSC	3.00 BSC	3.94	0.89	
	NOM	-	-	-	-	-	-	-	-			-	-	-
	MAX	1.60	0.56	0.48	0.44	4.60	1.83	2.60	2.29			4.25	1.20	

JEDEC Registration TO-243, Variation AA, Issue C, July 1986.

Drawings not to scale.

Supertex Doc. #: DSPD-3TO243AAN8, Version D070908.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

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