



PSMNR90-30BL

N-channel 30 V 1.0 m Ω logic level MOSFET in D2PAK

2 April 2014

Product data sheet

1. General description

Logic level N-channel MOSFET in D2PAK package qualified to 175 °C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

2. Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for logic level gate drive sources

3. Applications

- DC-to-DC converters
- Load switching
- Motor control
- Server power supplies

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
V _{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C	-	-	30	V	
I _D	drain current	T _{mb} = 25 °C; V _{GS} = 10 V; Fig. 2	[1]	-	120	A	
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 1	-	-	306	W	
T _j	junction temperature		-55	-	175	°C	
Static characteristics							
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 25 A; T _j = 25 °C; Fig. 12	-	0.89	1	m Ω	
		V _{GS} = 10 V; I _D = 25 A; T _j = 100 °C; Fig. 13 ; Fig. 12	-	1.19	1.5	m Ω	
Dynamic characteristics							
Q _{GD}	gate-drain charge	V _{GS} = 4.5 V; I _D = 75 A; V _{DS} = 15 V; Fig. 14 ; Fig. 15	-	37	-	nC	
Q _{G(tot)}	total gate charge		-	118	-	nC	



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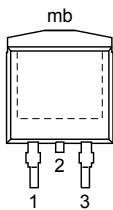
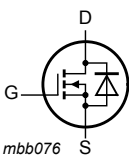


Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$; $T_{j(\text{init})} = 25\text{ °C}$; $I_D = 120\text{ A}$; $V_{\text{sup}} \leq 30\text{ V}$; $R_{GS} = 50\text{ }\Omega$; unclamped	-	-	1.9	J

[1] Continuous current is limited by package.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p>D2PAK (SOT404)</p>	 <p>mbb076</p>
2	D	drain[1]		
3	S	source		
mb	D	mounting base; connected to drain		

[1] It is not possible to make connection to pin 2

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMNR90-30BL	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMNR90-30BL	PSMNR90-30BL

8. Limiting values

Table 5. Limiting values

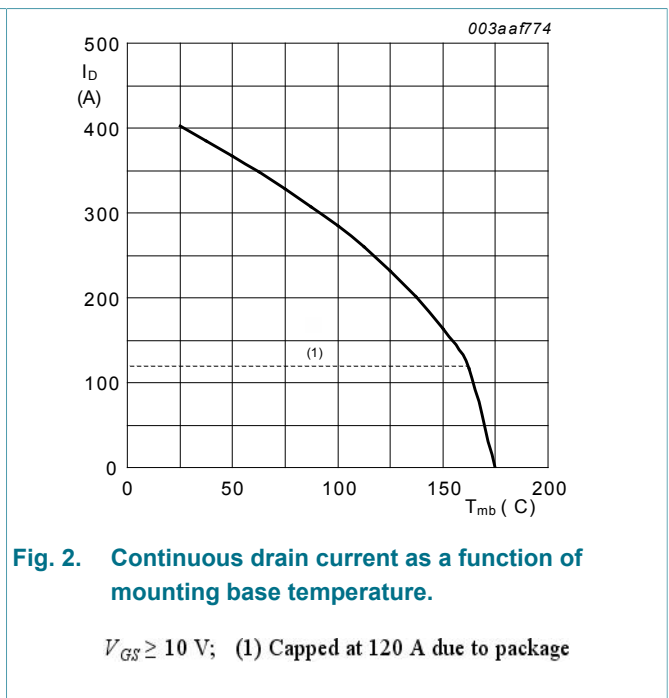
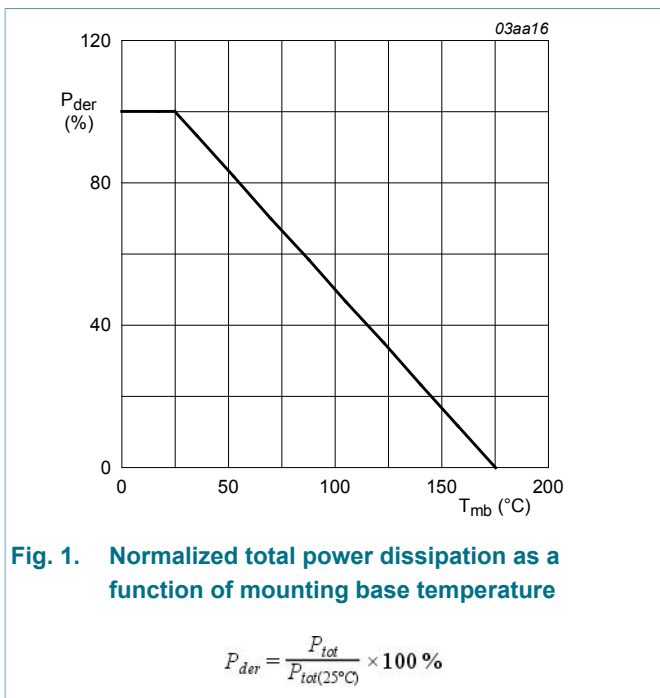
In accordance with the Absolute Maximum Rating System (IEC 60134).

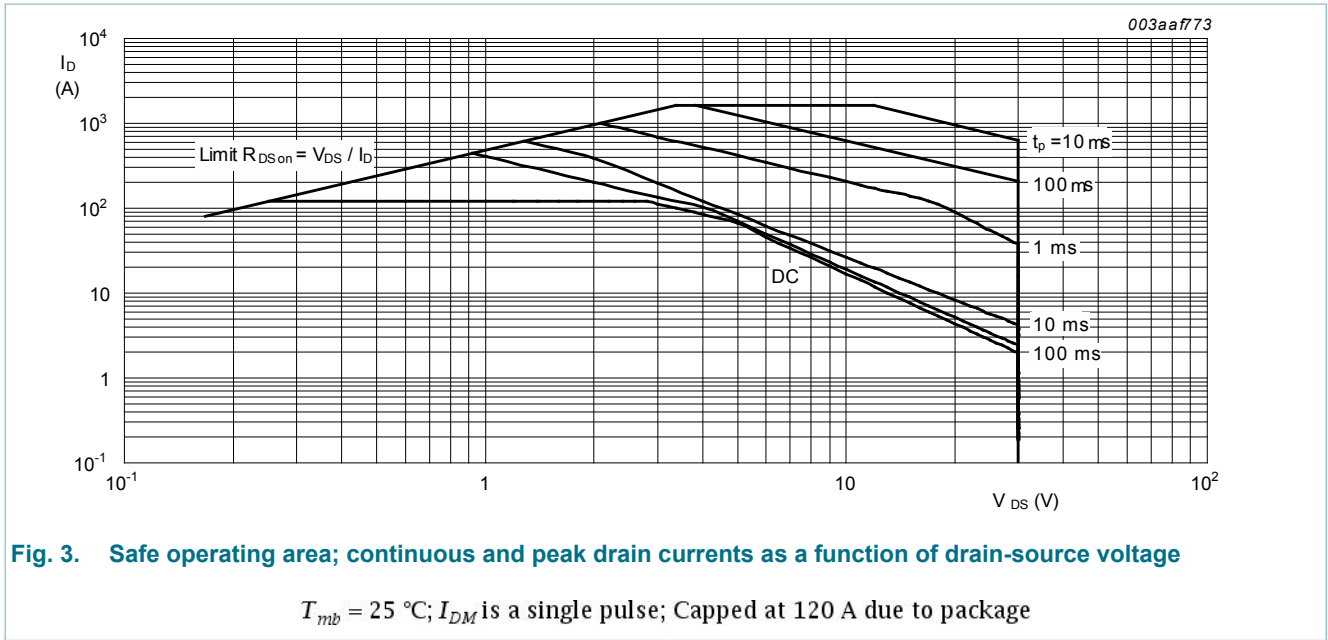
Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$	-	30	V
V_{DGR}	drain-gate voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	30	V

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Symbol	Parameter	Conditions		Min	Max	Unit
V _{GS}	gate-source voltage			-20	20	V
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 1		-	306	W
I _D	drain current	V _{GS} = 10 V; T _{mb} = 100 °C; Fig. 2	[1]	-	120	A
		V _{GS} = 10 V; T _{mb} = 25 °C; Fig. 2	[1]	-	120	A
I _{DM}	peak drain current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C; Fig. 3		-	1573	A
T _{stg}	storage temperature			-55	175	°C
T _j	junction temperature			-55	175	°C
T _{slid(M)}	peak soldering temperature			-	260	°C
Source-drain diode						
I _S	source current	T _{mb} = 25 °C	[1]	-	120	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C		-	1573	A
Avalanche ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	V _{GS} = 10 V; T _{j(init)} = 25 °C; I _D = 120 A; V _{sup} ≤ 30 V; R _{GS} = 50 Ω; unclamped		-	1.9	J

[1] Continuous current is limited by package.

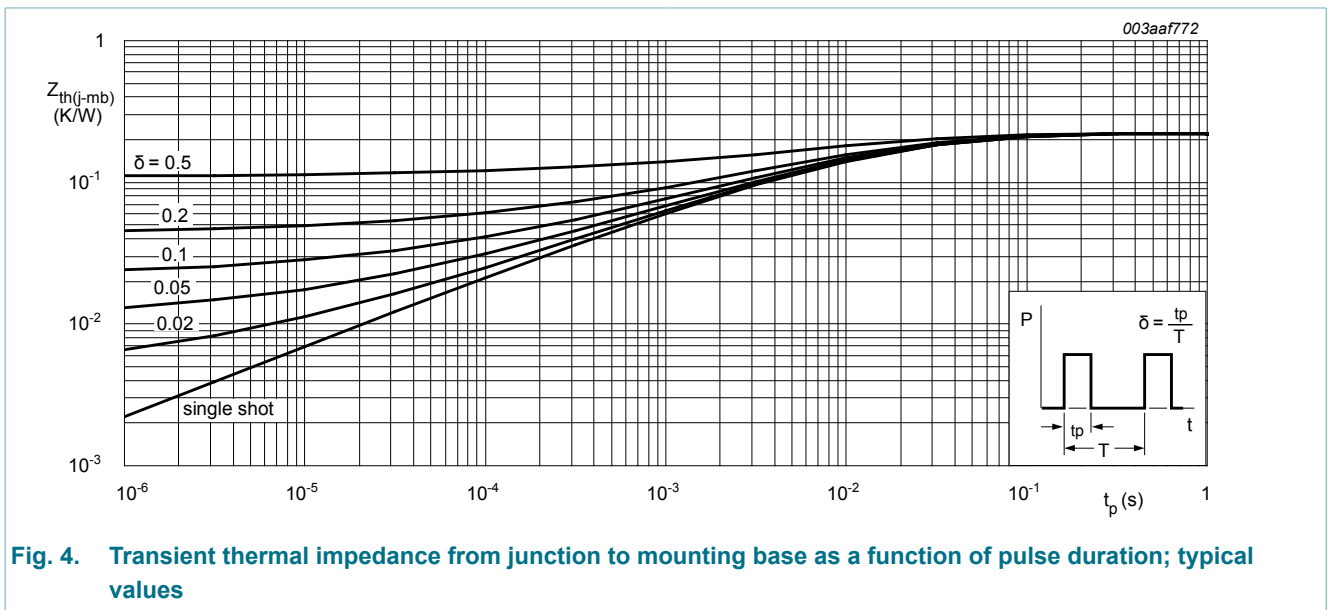




9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 4	-	0.22	0.49	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	minimum footprint; mounted on a printed-circuit board	-	50	-	K/W



10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	30	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C;$ Fig. 10; Fig. 11	1.3	1.7	2.2	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ C;$ Fig. 11	0.65	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ C;$ Fig. 11	-	-	2.5	V
I_{DSS}	drain leakage current	$V_{DS} = 30 V; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	0.02	10	μA
		$V_{DS} = 30 V; V_{GS} = 0 V; T_j = 175 \text{ }^\circ C$	-	-	500	μA
I_{GSS}	gate leakage current	$V_{GS} = 16 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	10	100	nA
		$V_{GS} = -16 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	10	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 V; I_D = 25 A; T_j = 25 \text{ }^\circ C;$ Fig. 12	-	0.89	1	mΩ
		$V_{GS} = 4.5 V; I_D = 25 A; T_j = 25 \text{ }^\circ C;$ Fig. 12	-	1.1	1.4	mΩ
		$V_{GS} = 10 V; I_D = 25 A; T_j = 175 \text{ }^\circ C;$ Fig. 13; Fig. 12	-	1.65	2	mΩ
		$V_{GS} = 10 V; I_D = 25 A; T_j = 100 \text{ }^\circ C;$ Fig. 13; Fig. 12	-	1.19	1.5	mΩ
R_G	gate resistance	$f = 1 \text{ MHz}$	-	1.1	-	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 75 A; V_{DS} = 15 V; V_{GS} = 10 V;$ Fig. 14; Fig. 15	-	243	-	nC
		$I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V$	-	222	-	nC
		$I_D = 75 A; V_{DS} = 15 V; V_{GS} = 4.5 V;$ Fig. 14; Fig. 15	-	118	-	nC
Q_{GS}	gate-source charge		-	39	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		-	22	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	17	-	nC
Q_{GD}	gate-drain charge		-	37	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 75 A; V_{DS} = 15 V;$ Fig. 14; Fig. 15	-	2.8	-	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{iss}	input capacitance	$V_{DS} = 15\text{ V}; V_{GS} = 0\text{ V}; f = 1\text{ MHz};$	-	14850	-	pF
C_{oss}	output capacitance	$T_j = 25\text{ }^\circ\text{C};$ Fig. 16	-	2799	-	pF
C_{rss}	reverse transfer capacitance		-	1215	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 15\text{ V}; R_L = 0.2\text{ }\Omega; V_{GS} = 5\text{ V};$ $R_{G(ext)} = 5\text{ }\Omega; I_D = 75\text{ A}; T_j = 25\text{ }^\circ\text{C}$	-	95	-	ns
t_r	rise time	$V_{DS} = 15\text{ V}; R_L = 0.2\text{ }\Omega; V_{GS} = 5\text{ V};$ $R_{G(ext)} = 5\text{ }\Omega; T_j = 25\text{ }^\circ\text{C}; I_D = 75\text{ A}$	-	213	-	ns
$t_{d(off)}$	turn-off delay time	$V_{DS} = 15\text{ V}; R_L = 0.2\text{ }\Omega; V_{GS} = 5\text{ V};$	-	199	-	ns
t_f	fall time	$R_{G(ext)} = 5\text{ }\Omega; I_D = 75\text{ A}; T_j = 25\text{ }^\circ\text{C}$	-	115	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 25\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C};$ Fig. 17	-	0.8	1.2	V
t_{rr}	reverse recovery time	$I_S = 25\text{ A}; di_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V};$	-	67	-	ns
Q_r	recovered charge	$V_{DS} = 15\text{ V}$	-	123	-	nC

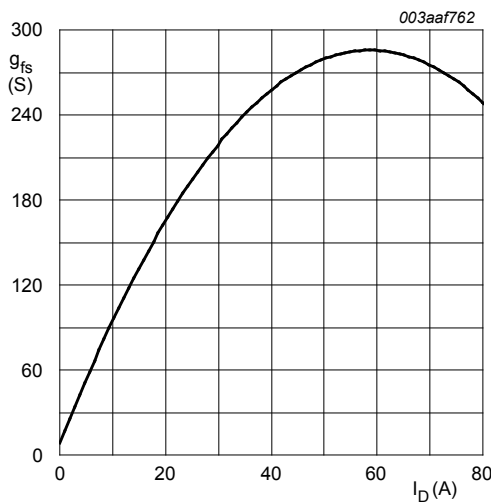


Fig. 5. Forward transconductance as a function of drain current; typical values

$$T_j = 25\text{ }^\circ\text{C}; V_{DS} = 15\text{ V}$$

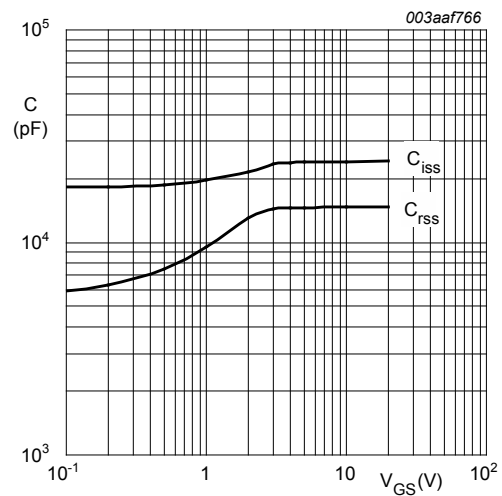


Fig. 6. Input and reverse transfer capacitances as a function of gate-source voltage; typical values

$$V_{DS} = 0\text{ V}; f = 1\text{ MHz}$$

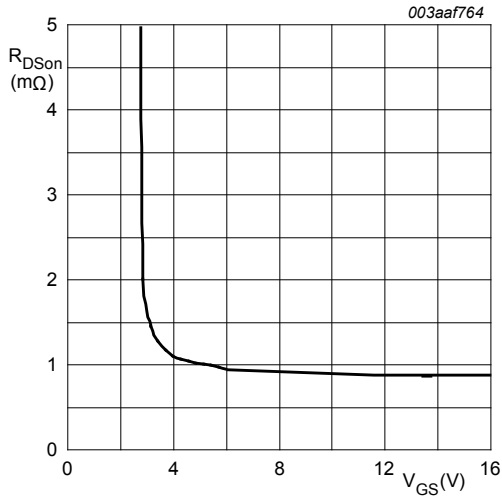


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

$T_j = 25\text{ }^\circ\text{C}; I_D = 25\text{ A}$

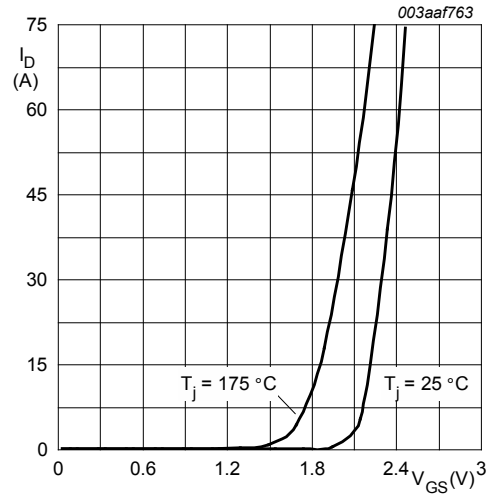


Fig. 8. Transfer characteristics: drain current as a function of gate-source voltage; typical values

$V_{DS} > I_D \times R_{DS(on)}$

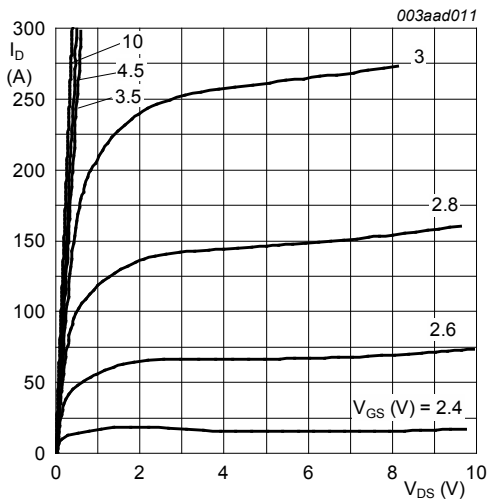


Fig. 9. Output characteristics: drain current as a function of drain-source voltage; typical values

$T_j = 25\text{ }^\circ\text{C}$

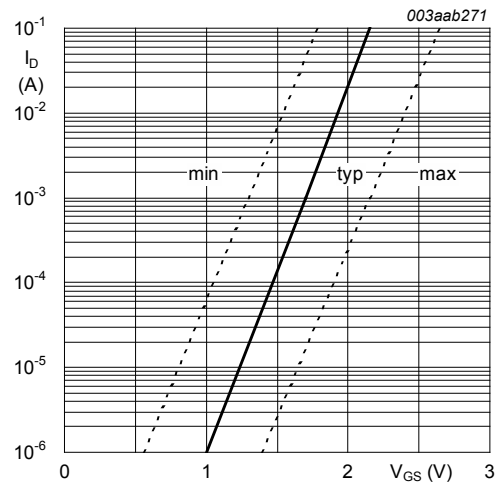


Fig. 10. Sub-threshold drain current as a function of gate-source voltage

$T_j = 25\text{ }^\circ\text{C}; V_{DS} = 5\text{ V}$

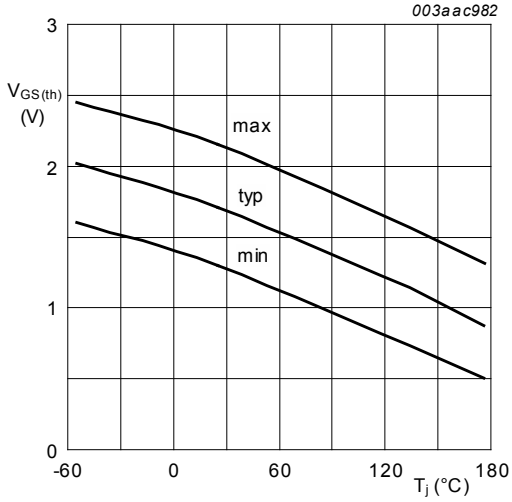


Fig. 11. Gate-source threshold voltage as a function of junction temperature

$$I_D = 1mA; V_{DS} = V_{GS}$$

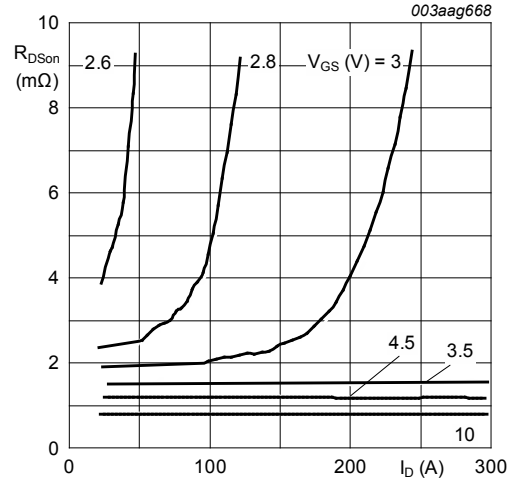


Fig. 12. Drain-source on-state resistance as a function of drain current; typical values

$$T_j = 25^\circ C$$

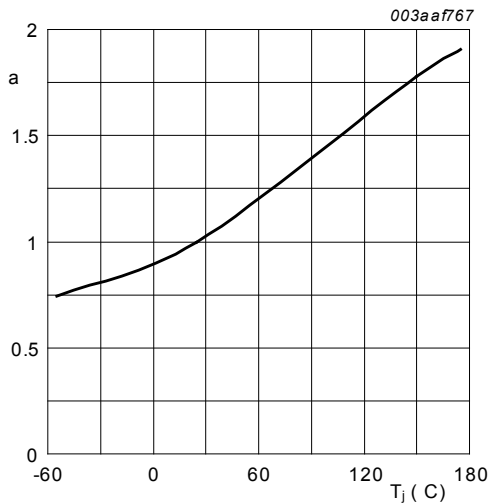


Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DS(on)}}{R_{DS(on)@25^\circ C}}$$

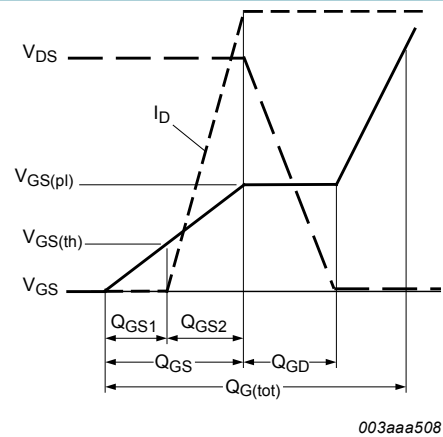


Fig. 14. Gate charge waveform definitions

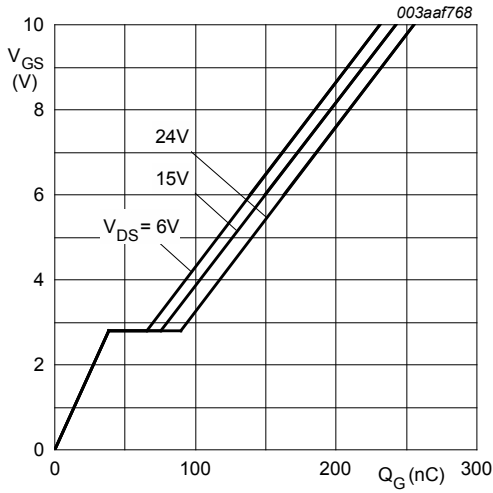


Fig. 15. Gate-source voltage as a function of gate charge; typical values

$T_j = 25\text{ }^\circ\text{C}; I_D = 75\text{ A}$

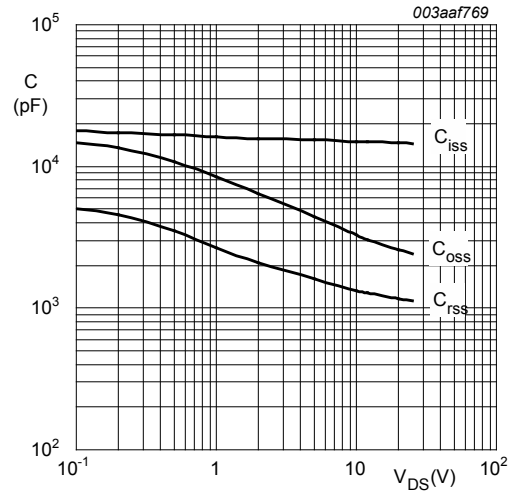


Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$V_{GS} = 0V; f = 1MHz$

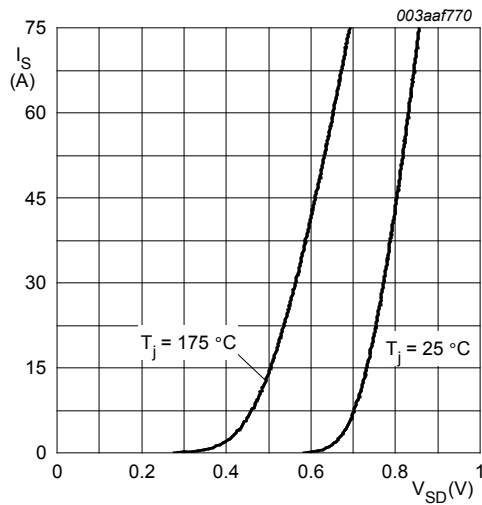


Fig. 17. Source current as a function of source-drain voltage; typical values

$V_{GS} = 0V$

11. Package outline

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped) SOT404



Dimensions (mm are the original dimensions)

Unit	A	A ₁	b	b ₂	c	D	D ₁	E	e	H _D	L _p	Q
max	4.5	1.40	0.85	1.45	0.64	11	1.6	10.3		15.8	2.9	2.6
nom									2.54			
min	4.1	1.27	0.60	1.05	0.46		1.2	9.7		14.8	2.1	2.2

sot404_po

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOT404					-06-03-16- 13-02-25

Fig. 18. Package outline D2PAK (SOT404)

12. Legal information

12.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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