C122F1G

Silicon Controlled Rectifiers

Reverse Blocking Thyristors

Designed primarily for full-wave ac control applications, such as motor controls, heating controls and power supplies; or wherever half−wave silicon gate−controlled, solid−state devices are needed.

Features

- Glass Passivated Junctions and Center Gate Fire for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermowatt Construction for Low Thermal Resistance, High Heat Dissipation and Durability
- Blocking Voltage to 50 Volts
- This is a Pb−Free Device*

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Repetitive Off−State Voltage (Note 1) (T_J = 25 to 100°C, Sine Wave, 50 to 60 Hz; Gate Open)	V_{DRM}, V_{RRM}	50	V
On-State RMS Current (180° Conduction Angles; T_C = 75°C)	$I_{T(RMS)}$	8.0	A
Peak Non-Repetitive Surge Current (1/2 Cycle, Sine Wave, 60 Hz, T_C = 75°C)	I_{TSM}	90	A
Circuit Fusing Considerations (t = 8.3 ms)	I^2t	34	A^2s
Forward Peak Gate Power (Pulse Width = 10 μs, T_C = 70°C)	P_{GM}	5.0	W
Forward Average Gate Power (t = 8.3 ms, T_C = 70°C)	$P_{G(AV)}$	0.5	W
Forward Peak Gate Current (Pulse Width = 10 μs, T_C = 70°C)	I_{GM}	2.0	A
Operating Junction Temperature Range	T_J	−40 to +125	°C
Storage Temperature Range	T_{stg}	−40 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. V_{DRM} and V_{RRM} for all types can be applied on a continuous basis. Ratings apply for zero or negative gate voltage; however, positive gate voltage shall not be applied concurrent with negative potential on the anode. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the devices are exceeded.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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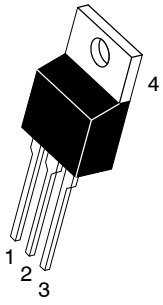
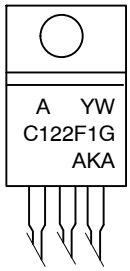
SCRs
8 AMPERES RMS
50 VOLTS



TO−220AB
CASE 221A
STYLE 3

MARKING DIAGRAM



A	= Assembly Location
Y	= Year
W	= Work Week
C122F1	= Device Code
G	= Pb−Free Package
AKA	= Diode Polarity

PIN ASSIGNMENT	
1	Cathode
2	Anode
3	Gate
4	Anode

ORDERING INFORMATION

Device	Package	Shipping
C122F1G	TO220AB (Pb−Free)	500 Units / Box

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	1.8	°C/W
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	62.5	°C/W
Maximum Lead Temperature for Soldering Purposes 1/8 in. from Case for 10 Seconds	T_L	260	°C

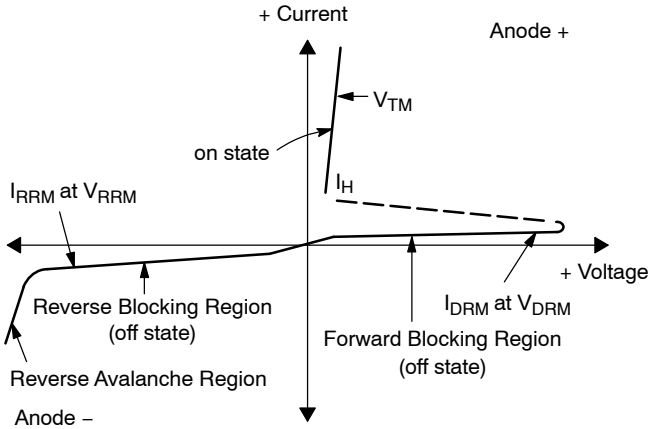
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Peak Repetitive Forward or Reverse Blocking Current (V_{AK} = Rated V_{DRM} or V_{RRM}, Gate Open)	T_C = 25°C	I_{DRM}, I_{RRM}	–	–	10	μA
	T_C = 125°C		–	–	0.5	mA
ON CHARACTERISTICS						
Peak On−State Voltage (Note 2) (I_{TM} = 16 A Peak, T_C = 25°C)		V_{TM}	–	–	1.83	V
Gate Trigger Current (Continuous dc) (V_{AK} = 12 V, R_L = 100 Ω)		I_{GT}				mA
	T_C = 25°C		–	–	25	
	T_C = −40°C		–	–	40	
Gate Trigger Voltage (Continuous dc) (V_{AK} = 12 V, R_L = 100 Ω)		V_{GT}				V
	T_C = 25°C		–	–	1.5	
	T_C = −40°C		–	–	2.0	
Gate Non−Trigger Voltage (Continuous dc) (V_{AK} = 12 V, R_L = 100 Ω, T_C = 125°C)		V_{GD}	0.2	–	–	V
Holding Current (V_{AK} = 12 Vdc, Initiating Current = 200 mA, Gate Open)		I_H				mA
	T_C = 25°C		–	–	30	
	T_C = −40°C		–	–	60	
Turn-Of f Time (V_D = Rated V_{DRM}) (I_{TM} = 8 A, I_R = 8 A)		t_q	–	50	–	μs
DYNAMIC CHARACTERISTICS						
Critical Rate−of−Rise of Off−State Voltage (V_{AK} = Rated V_{DRM}, Exponential Waveform, Gate Open, T_C = 100°C)		dv/dt	–	50	–	V/μs

2. Pulse Test: Pulse Width ≤ 1 ms, Duty Cycle ≤ 2%.

Voltage Current Characteristic of SCR

Symbol	Parameter
V_{DRM}	Peak Repetitive Off State Forward Voltage
I_{DRM}	Peak Forward Blocking Current
V_{RRM}	Peak Repetitive Off State Reverse Voltage
I_{RRM}	Peak Reverse Blocking Current
V_{TM}	Peak On State Voltage
I_H	Holding Current



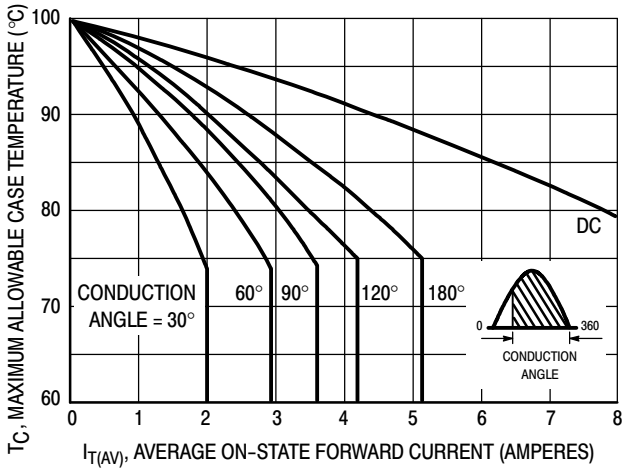


Figure 1. Current Derating (Half−Wave)

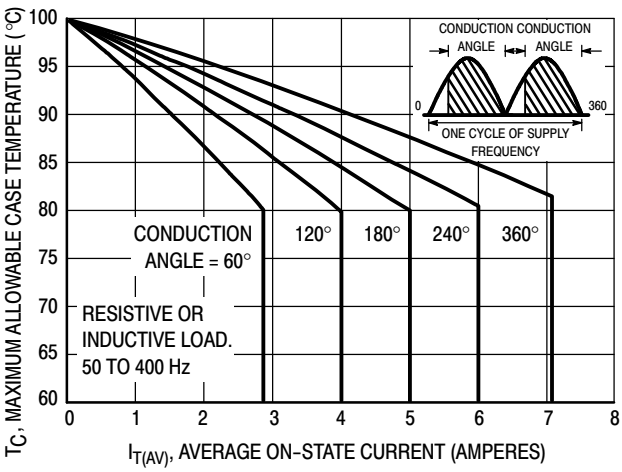


Figure 2. Current Derating (Full−Wave)

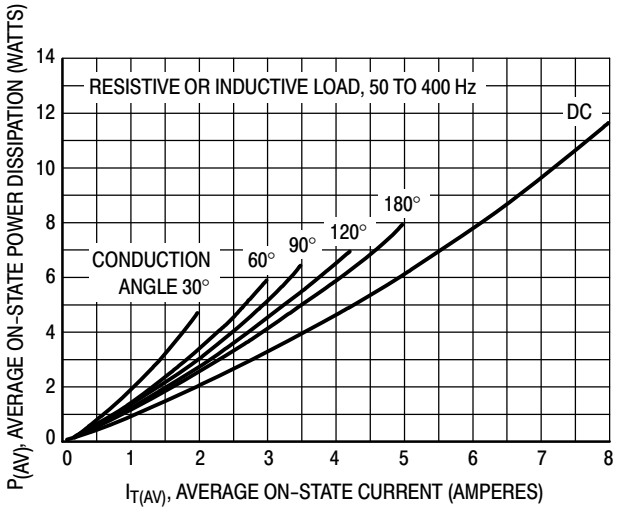


Figure 3. Maximum Power Dissipation (Half−Wave)

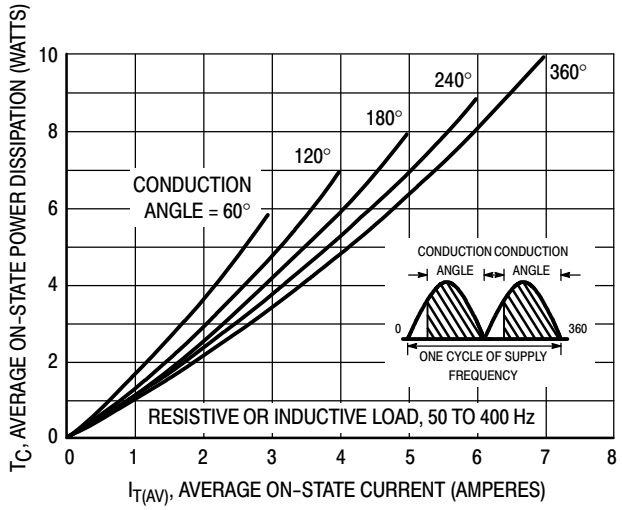
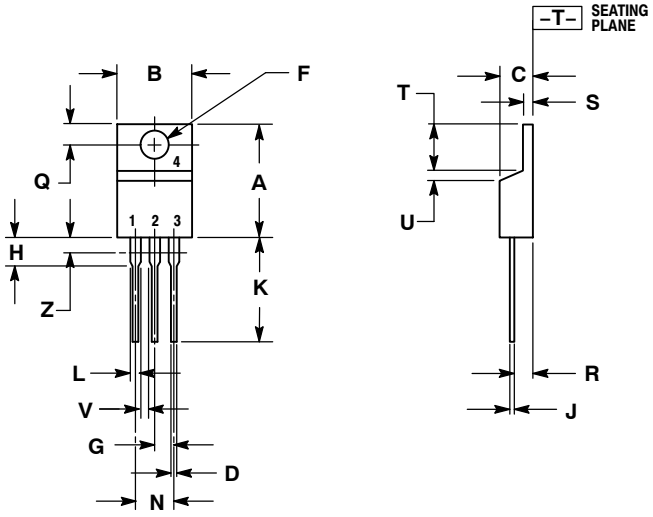


Figure 4. Maximum Power Dissipation (Full−Wave)

C122F1G

PACKAGE DIMENSIONS

TO−220AB
CASE 221A−07
ISSUE AA



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.014	0.022	0.36	0.55
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

STYLE 3:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

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