

NTMFS5844NL, NVMFS5844NL

Power MOSFET

60 V, 61 A, 12 mΩ, Single N-Channel

Features

- Small Footprint (5x6 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- NVMFS5844NLWF – Wettable Flanks Product
- NVMFS Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Value	Unit	
Drain-to-Source Voltage	V _{DS}	60	V	
Gate-to-Source Voltage	V _{GS}	±20	V	
Continuous Drain Current R _{ψJ-mb} (Notes 1, 2, 3, 4)	Steady State	T _{mb} = 25°C	I _D 61	A
		T _{mb} = 100°C	43	
Power Dissipation R _{ψJ-mb} (Notes 1, 2, 3)	Steady State	T _{mb} = 25°C	P _D 107	W
		T _{mb} = 100°C	54	
Continuous Drain Current R _{θJA} (Notes 1, 3, 4)	Steady State	T _A = 25°C	I _D 11.2	A
		T _A = 100°C	8.0	
Power Dissipation R _{θJA} (Notes 1 & 3)	Steady State	T _A = 25°C	P _D 3.7	W
		T _A = 100°C	1.8	
Pulsed Drain Current	T _A = 25°C, t _p = 10 μs	I _{DM}	247	A
Current Limited by Package (Note 4)	T _A = 25°C	I _{DmaxPkg}	80	A
Operating Junction and Storage Temperature	T _J , T _{stg}	-55 to 175	°C	
Source Current (Body Diode)	I _S	60	A	
Single Pulse Drain-to-Source Avalanche Energy (T _J = 25°C, V _{DD} = 50 V, V _{GS} = 10 V, I _{L(pk)} = 31 A, L = 0.1 mH, R _G = 25 Ω)	E _{AS}	48	mJ	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T _L	260	°C	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Mounting Board (top) – Steady State (Notes 2, 3)	R _{ψJ-mb}	1.4	°C/W
Junction-to-Ambient – Steady State (Note 3)	R _{θJA}	41	

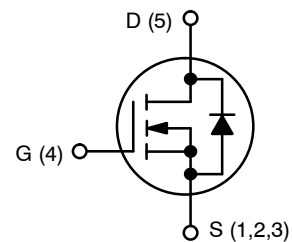
1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Psi (Ψ) is used as required per JESD51-12 for packages in which substantially less than 100% of the heat flows to single case surface.
3. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
4. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.



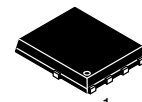
ON Semiconductor®

<http://onsemi.com>

V _{(BR)DSS}	R _{DS(ON)} MAX	I _D MAX
60 V	12 mΩ @ 10 V	61 A
	16 mΩ @ 4.5 V	

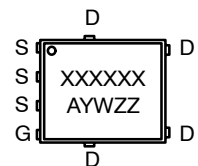


N-CHANNEL MOSFET



DFN5
(SO-8FL)
CASE 488AA
STYLE 1

MARKING DIAGRAM



- A = Assembly Location
- Y = Year
- W = Work Week
- ZZ = Lot Traceability

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

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ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	60			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			57		mV/ $^\circ\text{C}$
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 60\text{ V}$	$T_J = 25\ ^\circ\text{C}$		1	μA
			$T_J = 125^\circ\text{C}$		100	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA

ON CHARACTERISTICS (Note 5)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	1.5		2.3	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			6.2		mV/ $^\circ\text{C}$
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 10\text{ A}$		10.2	12	m Ω
		$V_{GS} = 4.5\text{ V}, I_D = 10\text{ A}$		13	16	
Forward Transconductance	g_{FS}	$V_{DS} = 5\text{ V}, I_D = 10\text{ A}$		27		S

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 25\text{ V}$		1460		pF	
Output Capacitance	C_{OSS}			150			
Reverse Transfer Capacitance	C_{RSS}			96			
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DS} = 48\text{ V}; I_D = 10\text{ A}$		30		nC	
Total Gate Charge	$Q_{G(TOT)}$			15			
Threshold Gate Charge	$Q_{G(TH)}$			1.0			
Gate-to-Source Charge	Q_{GS}			4.0			
Gate-to-Drain Charge	Q_{GD}			8.0			
Plateau Voltage	V_{GP}		$V_{GS} = 4.5\text{ V}, V_{DS} = 48\text{ V}; I_D = 10\text{ A}$		3.0		V
Gate Resistance	R_G				0.62		Ω

SWITCHING CHARACTERISTICS (Note 6)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 48\text{ V}, I_D = 10\text{ A}, R_G = 2.5\ \Omega$		12		ns
Rise Time	t_r			25		
Turn-Off Delay Time	$t_{d(OFF)}$			20		
Fall Time	t_f			10		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = 10\text{ A}$	$T_J = 25^\circ\text{C}$		0.79	1.2	V
			$T_J = 125^\circ\text{C}$		0.65		
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, dI_S/dt = 100\text{ A}/\mu\text{s}, I_S = 10\text{ A}$		19		ns	
Charge Time	t_a			13			
Discharge Time	t_b			6.0			
Reverse Recovery Charge	Q_{RR}			15			nC

5. Pulse Test: pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

6. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

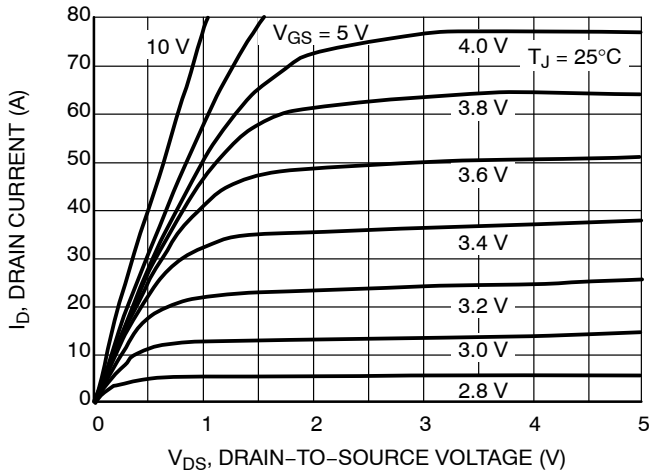


Figure 1. On-Region Characteristics

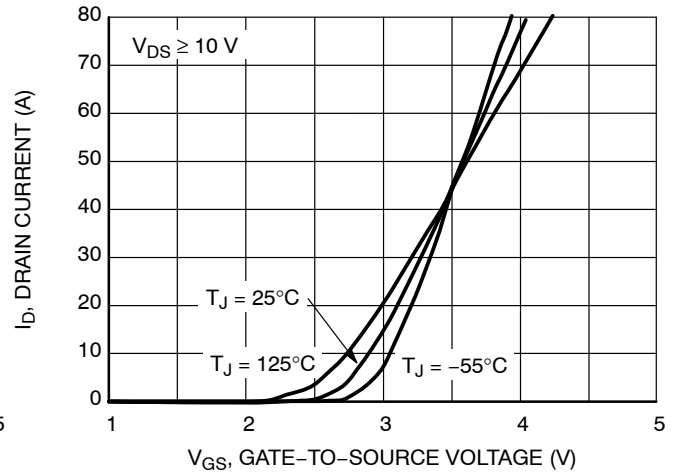


Figure 2. Transfer Characteristics

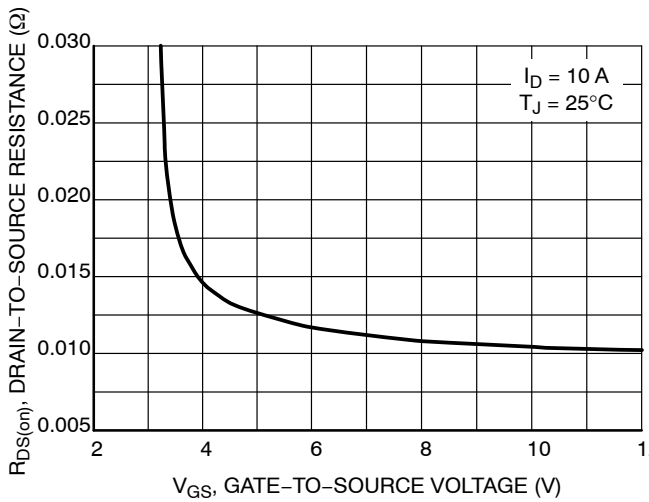


Figure 3. On-Resistance vs. Gate-to-Source Voltage

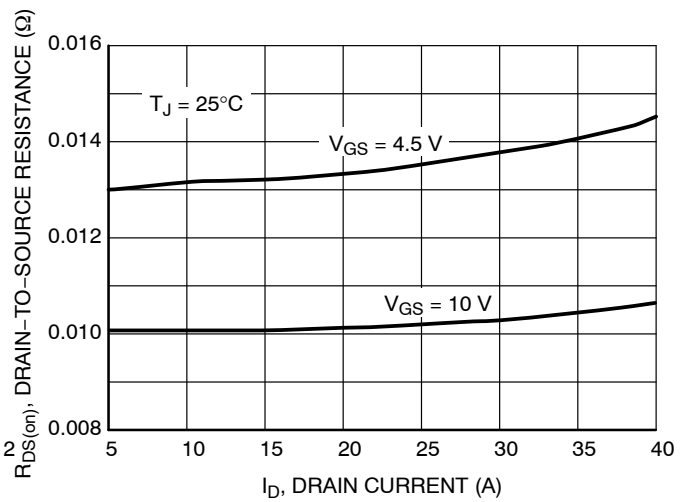


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

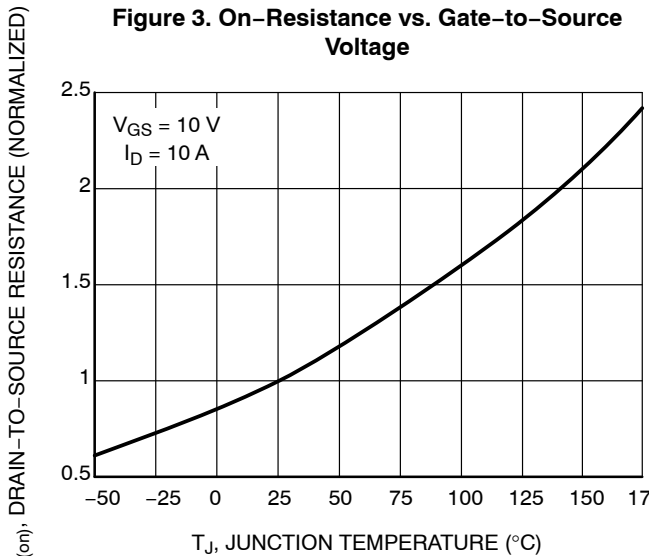


Figure 5. On-Resistance Variation with Temperature

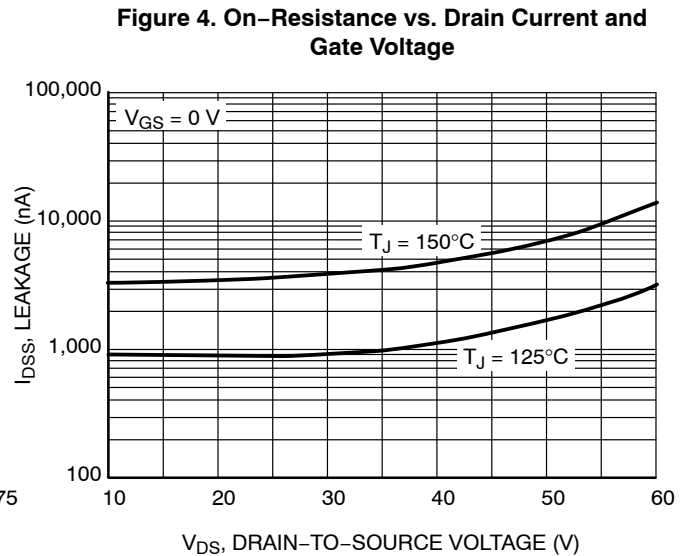


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

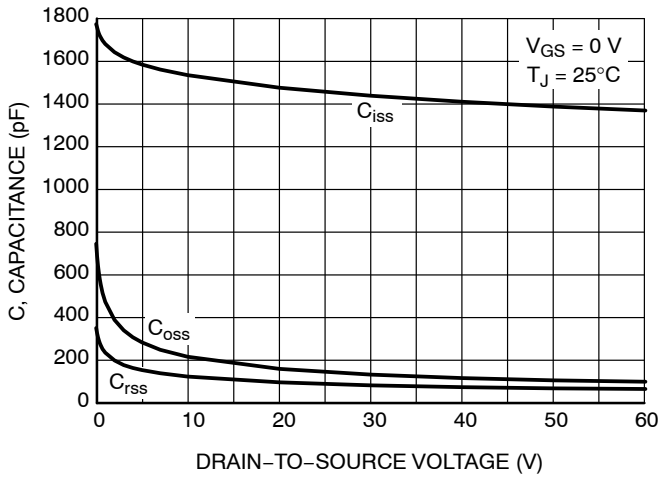


Figure 7. Capacitance Variation

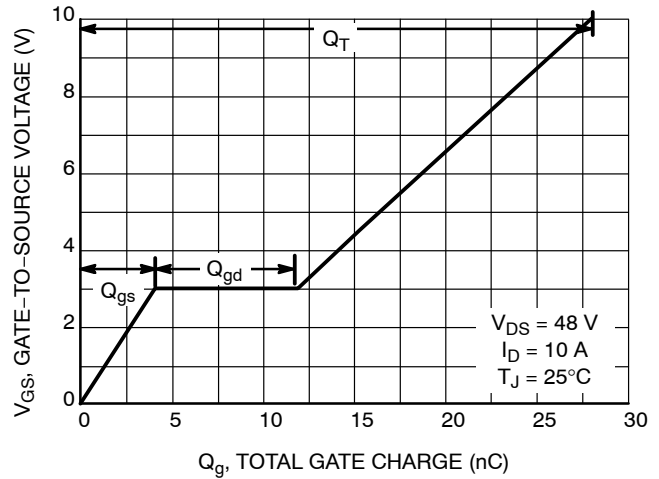


Figure 8. Gate-to-Source Voltage vs. Total Charge

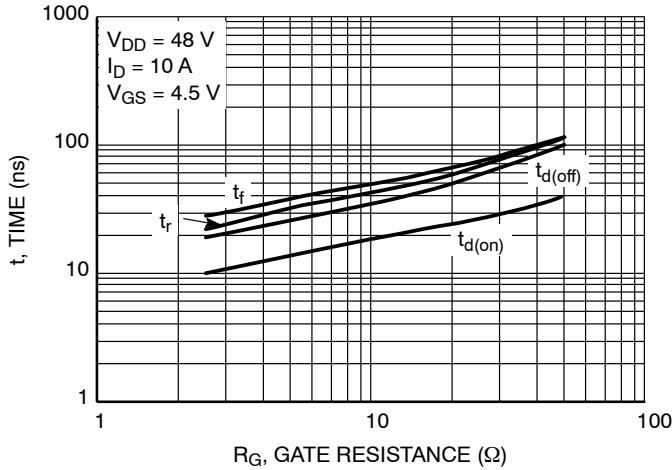


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

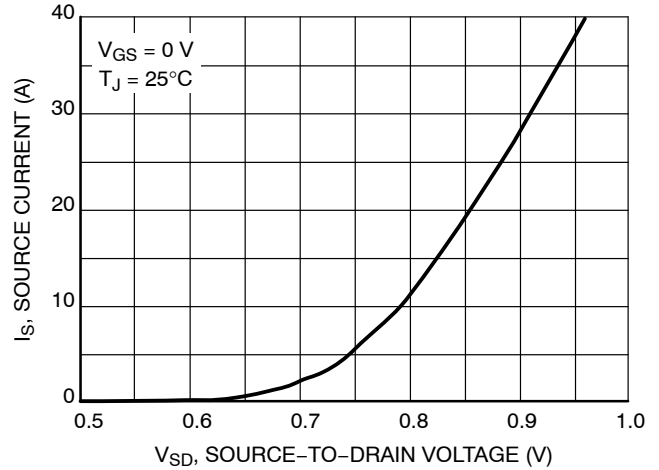


Figure 10. Diode Forward Voltage vs. Current

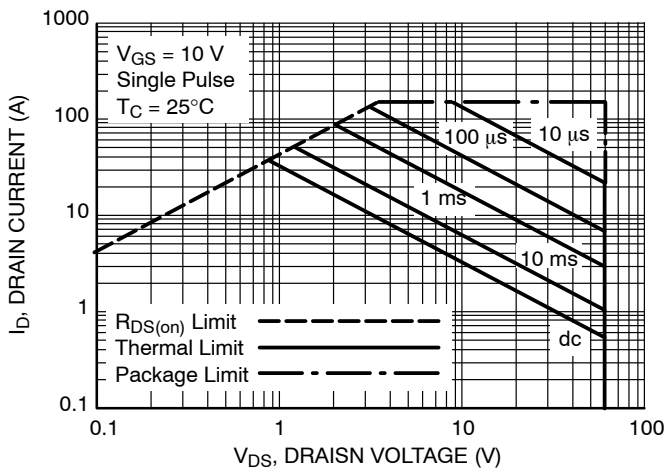


Figure 11. Maximum Rated Forward Biased Safe Operating Area

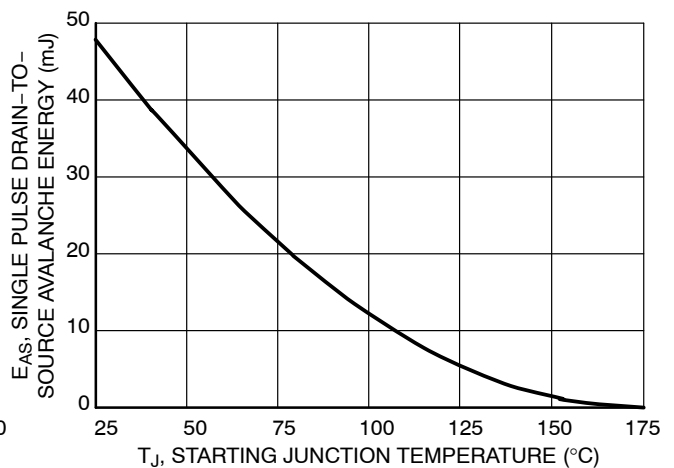


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

NTMFS5844NL, NVMFS5844NL

TYPICAL CHARACTERISTICS

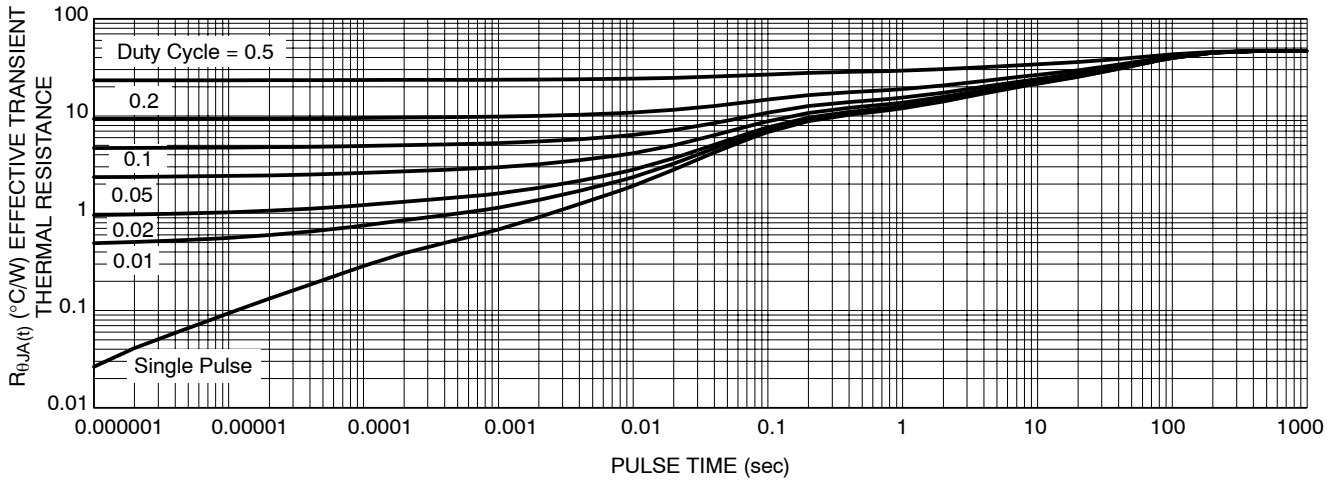


Figure 13. Thermal Response

DEVICE ORDERING INFORMATION

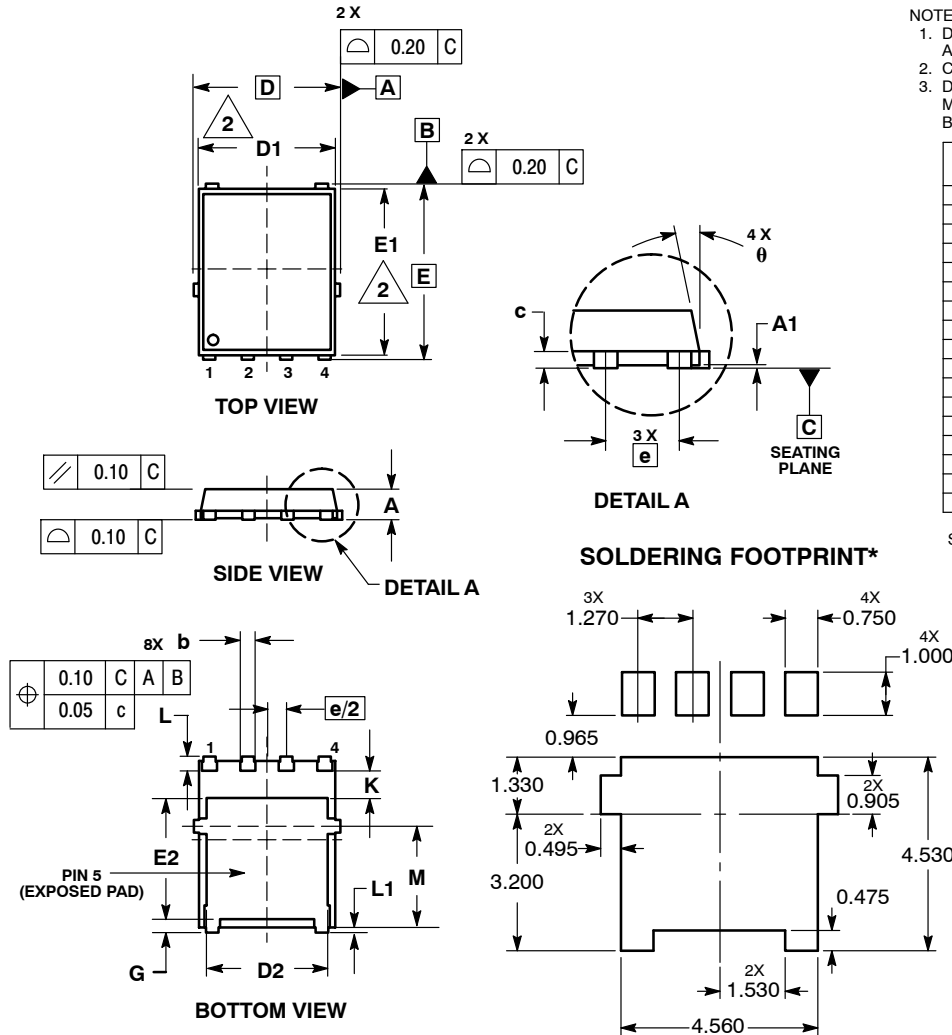
Device	Marking	Package	Shipping [†]
NTMFS5844NLT1G	5844NL	DFN5 (Pb-Free)	1500 / Tape & Reel
NVMFS5844NLT1G	V5844L	DFN5 (Pb-Free)	1500 / Tape & Reel
NVMFS5844NLWFT1G	5844LW	DFN5 (Pb-Free)	1500 / Tape & Reel
NVMFS5844NLT3G	V5844L	DFN5 (Pb-Free)	5000 / Tape & Reel
NVMFS5844NLWFT3G	5844LW	DFN5 (Pb-Free)	5000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NTMFS5844NL, NVMFS5844NL

PACKAGE DIMENSIONS

DFN5 5x6, 1.27P
(SO-8FL)
CASE 488AA
ISSUE H



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.15 BSC		
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.15 BSC		
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
e	1.27 BSC		
G	0.51	0.61	0.71
K	1.20	1.35	1.50
L	0.51	0.61	0.71
L1	0.05	0.17	0.20
M	3.00	3.40	3.80
θ	0 °	---	12 °

STYLE 1:

1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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