## DC Brush Motor Drivers (36V Max)

## BD62321HFP

## General Description

BD62321HFP is a full bridge driver for brush motor applications. This IC can operate at a wide range of power-supply voltages (from 6 V to 32 V ) with output currents of up to 3A. MOS transistors in the output stage allow PWM speed control. The BD62321HFP is pin compatible with the BD623xHFP series.

## Features

- Built-in One Channel Driver
- Cross-Conduction Prevention Circuit
- Four Protection Circuits Provided: OCP, OVP, TSD, UVLO and SAP


## Applications

VTR; CD/DVD players; audio-visual equipment; optical disc drives; PC peripherals; OA equipments

## Key Specifications

■ Supply Voltage Range:
36V(Max)

- Maximum Output Current:
3.0A

■ Output ON-Resistance:
$1.0 \Omega$

- PWM Input Frequency Range:
- Standby Current: 20 kHz to 100 kHz
- Operating Temperature Range:
$0 \mu \mathrm{~A}$ (Тур)

Package HRP7
$W($ Typ $) \times D(T y p) \times H(T y p)$
$9.395 \mathrm{~mm} \times 10.540 \mathrm{~mm} \times 2.005 \mathrm{~mm}$


## Ordering Information



## Lineup

| Voltage rating <br> (Max) | Channels | Output current (Max) | Package |  | Ordering <br> Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 36 V | 1 ch | 3.0 A | HRP7 | Reel of 2000 | BD62321HFP-TR |

## Block Diagram



Pin Configuration


Pin Descriptions

| Pin No. | Name | Function |
| :---: | :---: | :--- |
| 1 | VCC | Power supply |
| 2 | OUT1 | Driver output |
| 3 | FIN | Control input (forward) |
| 4 | GND | Ground |
| 5 | RIN | Control input (reverse) |
| 6 | OUT2 | Driver output |
| 7 | VCC | Power supply |
| FIN | GND | Ground |

(Note) Use all VCC pin by the same voltage.

Absolute Maximum Ratings ( $\mathrm{Ta}=25^{\circ} \mathrm{C}$, All voltages are with respect to ground)

| Parameter | Symbol | Rating | Unit |
| :--- | :---: | :---: | :---: |
| Supply Voltage | $\mathrm{V}_{\mathrm{cc}}$ | 36 | V |
| Output Current | $\mathrm{I}_{\mathrm{max}}$ | $3.0^{(\text {Note } 1)}$ | A |
| All Other Input Pins | $\mathrm{V}_{\mathrm{IN}}$ | $-0.3^{\text {to }} \mathrm{V}$ cc | V |
| Operating Temperature | Topr | -40 to +85 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature | Tstg | -55 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Power Dissipation | Pd | $1.6^{(\text {Note } 2)}$ | W |
| Junction Temperature | Tjmax | 150 | ${ }^{\circ} \mathrm{C}$ |

(Note 1) Do not exceed Pd or ASO.
(Note 2) HRP7 package. Mounted on a $70 \mathrm{~mm} \times 70 \mathrm{~mm} \times 1.6 \mathrm{~mm}$ glass-epoxy board. Derate by $12.8 \mathrm{~mW} /{ }^{\circ} \mathrm{C}$ for Ta above $25^{\circ} \mathrm{C}$
Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions ( $\mathrm{Ta}=25^{\circ} \mathrm{C}$ )

| Parameter | Symbol | Rating | Unit |
| :---: | :---: | :---: | :---: |
| Supply Voltage | $\mathrm{V}_{\mathrm{cc}}$ | 6 to 32 | V |

Electrical Characteristics (Unless otherwise specified, $\mathrm{Ta}=25^{\circ} \mathrm{C}$ and $\mathrm{V}_{\mathrm{cc}}=24 \mathrm{~V}$ )

| Parameter | Symbol | Limit |  |  | Unit | Conditions |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |  |
| Supply Current | Icc | 0.7 | 1.4 | 2.2 | mA | Forward / Reverse / Brake |
| Stand-by Current | Istby | - | 0 | 10 | $\mu \mathrm{A}$ | Stand-by |
| Input High Voltage | $\mathrm{V}_{\mathrm{IH}}$ | 2.0 | - | - | V |  |
| Input Low Voltage | VIL | - | - | 0.8 | V |  |
| Input Bias Current | ІІн | 30 | 50 | 100 | $\mu \mathrm{A}$ | V in $=5.0 \mathrm{~V}$ |
| Output ON-Resistance | Ron | 0.5 | 1.0 | 1.5 | $\Omega$ | lout=1.0A, vertically total |
| Input Frequency Range | $\mathrm{f}_{\text {max }}$ | 20 | - | 100 | kHz | FIN / RIN |

## Typical Performance Curves (Reference Data)



Figure 1. Supply Current vs Supply Voltage


Figure 3. Internal Logic vs Input Voltage (Input Threshold Voltage)


Figure 2. Stand-by Current vs Supply Voltage


Figure 4. Input Bias Current vs Input Voltage

Typical Performance Curves (Reference Data) - Continued


Figure 5. Internal Signal vs Supply Voltage (Under Voltage Lock Out)


Figure 7. Output High Voltage vs Output Current


Figure 6. Internal Signal vs Supply Voltage (Over Voltage Protection)


Figure 8. Output Voltage vs Output Current (High Side Body Diode)

Fig. 5 Input threshold voltage

Typical Performance Curves (Reference Data) - continued


Figure 9. Internal Logic vs Load Current
(Over-Current Protection, H side)
Fig. 5 Input threshold voltage


Figure 11. Output Voltage vs Output Current (Low Side Body Diode)


Figure 12. Internal Logic vs Load Current (Over- Current Protection, L side)

Fig. 5 Input threshold voltage

## Application Information

## 1. Description of Functions

(1) Operation Modes

Table 1 Logic table

| Mode | FIN | RIN | OUT1 | OUT2 | Operation |
| :---: | :---: | :---: | :---: | :---: | :--- |
| a | L | L | Hi-Z ${ }^{\text {(Note) }}$ | Hi-Z ${ }^{\text {(Note) }}$ | Stand-by (idling) |
| b | H | L | H | L | Forward (OUT1 > OUT2) |
| c | L | H | L | H | Reverse (OUT1 < OUT2) |
| d | H | H | L | L | Brake (stop) |
| e | PWM | L | H | $\overline{\text { PWM }}$ | Forward (PWM control) |
| f | L | PWM | $\overline{\text { PWM }}$ | H | Reverse (PWM control) |

Please note that this is the state of the connected diodes, which differs from that of the mechanical relay.
Mode (a) Stand-by Mode
In stand-by mode, all internal circuits are turned off, including the output power transistors. Motor output goes to high impedance. When the system is switched to stand-by mode while the motor is running, the system enters an idling state because of the body diodes. However, when the system switches to stand-by from any other mode (except the brake mode), the control logic remains in the high state for at least $50 \mu \mathrm{~s}$ before shutting down all circuits.

Mode (b) Forward Mode
This operating mode is defined as the forward rotation of the motor when OUT1 pin is high and OUT2 pin is low. When the motor is connected between OUT1 and OUT2 pins, the current flows from OUT1 to OUT2.

Mode (c) Reverse Mode
This operating mode is defined as the reverse rotation of the motor when OUT1 pin is low and OUT2 pin is high. When the motor is connected between the OUT1 and OUT2 pins, the current flows from OUT2 to OUT1.

Mode
(d) Brake Mode

This operating mode is used to quickly stop the motor (short circuit brake). It differs from the stand-by mode because the internal control circuit is operating in the brake mode. Please switch to stand-by mode (rather than the brake mode) to save power and reduce consumption.


Figure 13. Four Basic Operations (Output Stage)

Mode (e),(f) PWM Control Mode
The rotational speed of the motor can be controlled by the duty cycle of the PWM signal fed to the FIN pin or the RIN pin. In this mode, the high side output is fixed and the low side output is switching, corresponding to the input signal. The state of the output toggles between LOW and high impedance.

The frequency of the input PWM signal can be between 20 kHz and 100 kHz . The circuit may not operate properly for PWM frequencies below 20 kHz and above 100 kHz . Note that control may not be attained by switching on duty at frequencies lower than 20 kHz , since the operation functions via the stand-by mode. To operate in this mode, connect the VREF pin to the VCC pin. In addition, establish a current path for the recovery current from the motor, by connecting a bypass capacitor ( $10 \mu \mathrm{~F}$ or higher is recommended) between VCC and ground.


Figure 14. PWM Control Operation (Output Stage)


Figure 15. PWM Control Operation (Timing Chart)
(2) Cross-Conduction Protection Circuit

In the full bridge output stage, when the upper and lower transistors are turned on at the same time during high to low or low to high transition, an inrush current flows from the power supply to ground, resulting to a loss. This circuit eliminates the inrush current by providing a dead time (about 800ns, nominal) during the transition.
(3) Output Protection Circuits
(a) Under Voltage Lock Out (UVLO) Circuit

To ensure the lowest power supply voltage necessary to operate the controller, and to prevent under voltage malfunctions, a UVLO circuit has been built into this driver. When the power supply voltage falls to 5.3 V (nominal) or below, the controller forces all driver outputs to high impedance. When the voltage rises to 5.5 V (nominal) or above, the UVLO circuit ends the lockout operation and returns the chip to normal operation.
(b) Over Voltage Protection (OVP) Circuit

When the power supply voltage exceeds 45 V (nominal), the controller forces all driver outputs to high impedance. The OVP circuit is released and its operation ends when the voltage drops back to 40 V (nominal) or below. This protection circuit does not work in the stand-by mode. Also, note that this circuit is supplementary, and thus if it is asserted, the absolute maximum rating will have been exceeded. Therefore, do not continue to use the IC after this circuit is activated, and do not operate the IC in an environment where activation of the circuit is assumed.
(c) Thermal Shutdown (TSD) Circuit The TSD circuit operates when the junction temperature of the driver exceeds the preset temperature $\left(175^{\circ} \mathrm{C}\right.$ nominal). At this time, the controller forces all driver outputs to high impedance. Since thermal hysteresis is provided in the TSD circuit, the chip returns to normal operation when the junction temperature falls below the preset temperature $\left(150^{\circ} \mathrm{C}\right.$ nominal). Thus, it is a self-resetting circuit.
The TSD circuit is designed only to shut the IC off to prevent thermal runaway. It is not designed to protect the IC or guarantee its operation in the presence of extreme heat. Do not continue to use the IC after the TSD circuit is activated, and do not operate the IC in an environment where activation of the circuit is assumed.
(d) Over Current Protection (OCP) Circuit To protect this driver IC from ground faults, power supply line faults and load short circuits, the OCP circuit monitors the output current for the circuit's monitoring time ( $10 \mu \mathrm{~s}$, nominal). When the protection circuit detects an over current, the controller forces all driver outputs to high impedance during the off time ( $290 \mu \mathrm{~s}$, nominal). The IC returns to normal operation after the off time period has elapsed (self-returning type). At the two channels type, this circuit works independently for each channel.


Figure 16. Over-Current Protection (Timing Chart)
(e) Safe Area Protection (SAP) Circuit

To protect the output MOS transistors from exceeding ASO, ground faults, power supply line faults and load short circuits, the SAP circuit monitors the conditions for the circuit's monitoring time ( $10 \mu \mathrm{~s}$, nominal). When the protection circuit detects to exceed ASO, the controller forces all driver outputs to high impedance and latches this state. It is released from standby mode during $150 \mu \mathrm{~s}$ or more by the control inputs FIN and RIN.

## I/O Equivalent Circuits



Figure 17. FIN / RIN


Figure 18. OUT1 / OUT2

## Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.
2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

## 3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

## 4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

## 5. Thermal Consideration

Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.
6. Recommended Operating Conditions

These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

## 7. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.
8. Operation Under Strong Electromagnetic Field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.
9. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.
10. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.
11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

## Operational Notes - continued

## 12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the $P$ layers with the $N$ layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

> When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
> When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the $P$ substrate) should be avoided.


Figure 19. Example of monolithic IC structure
13. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).
14. Power supply lines 2

Return current generated by the motor's Back-EMF requires countermeasures, such as providing a return current path by inserting capacitors across the power supply and GND ( $10 \mu \mathrm{~F}$, ceramic capacitor is recommended). In this case, it is important to conclusively confirm that none of the negative effects sometimes seen with electrolytic capacitors - including a capacitance drop at low temperatures - occurs. Also, the connected power supply must have sufficient current absorbing capability. Otherwise, the regenerated current will increase voltage on the power supply line, which may in turn cause problems with the product, including peripheral circuits exceeding the absolute maximum rating. To help protect against damage or degradation, physical safety measures should be taken, such as providing a voltage clamping diode across the power supply and GND.
15. Capacitor Between Output and Ground

If a large capacitor is connected between the output pin and ground pin, current from the charged capacitor can flow into the output pin and may destroy the IC when the VCC or VIN pin is shorted to ground or pulled down to OV. Use a capacitor smaller than $10 \mu \mathrm{~F}$ between output and ground.

## 16. Switching Noise

When the operation mode is in PWM control or VREF control, PWM switching noise may affect the control input pins and cause IC malfunctions. In this case, insert a pull down resistor ( $10 \mathrm{k} \Omega$ is recommended) between each control input pin and ground.

## Marking Diagram



Physical Dimension, Tape and Reel Information


## Revision History

| Date | Revision | Changes |
| :---: | :---: | :--- |
| 10.Apr.2012 | 001 | New Release |
| 25.Dec.2012 | 002 | Improved the statement in all pages. <br> Deleted "Status of this document" in page 11. |
| 06.Aug.2014 | 003 | Applied the ROHM Standard Style. <br> Improved Operational Notes. |

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