

1.5V Drive Nch MOSFET

TT8K1

● Structure

Silicon N-channel MOSFET

● Features

- 1) Low On-resistance.
- 2) High power package.
- 3) 1.5V drive.

● Application

Switching

● Packaging specifications

Type	Package	Taping
	Code	TR
	Basic ordering unit (pieces)	3000
TT8K1		○

● Absolute maximum ratings (Ta = 25°C)

<It is the same ratings for the Tr1 and Tr2.>

Parameter	Symbol	Limits	Unit
Drain-source voltage	V_{DSS}	20	V
Gate-source voltage	V_{GSS}	± 10	V
Drain current	Continuous	I_D	± 2.5 A
	Pulsed	I_{DP}^{*1}	± 10 A
Source current (Body Diode)	Continuous	I_S	0.8 A
	Pulsed	I_{SP}^{*1}	10 A
Power dissipation	P_D^{*2}	1.25	W / TOTAL
		1.0	W / ELEMENT
Channel temperature	T_{ch}	150	°C
Range of storage temperature	T_{stg}	-55 to +150	°C

*1 $P_w \leq 10\mu s$, Duty cycle $\leq 1\%$

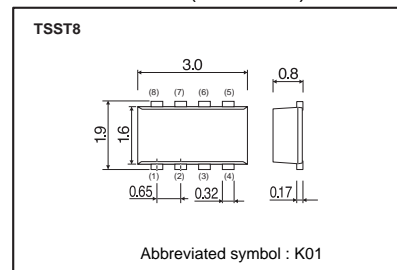
*2 Mounted on a ceramic board.

● Thermal resistance

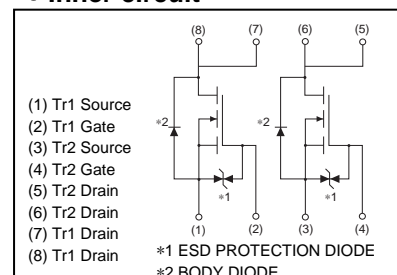
Parameter	Symbol	Limits	Unit
Channel to Ambient	$R_{th}(ch-a)^*$	100	°C / W / TOTAL
		125	°C / W / ELEMENT

*Mounted on a ceramic board.

● Dimensions (Unit : mm)



● Inner circuit



● **Electrical characteristics** (Ta = 25°C)

<It is the same characteristics for the Tr1 and Tr2.>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	-	-	±10	μA	$V_{GS}=\pm 10V, V_{DS}=0V$
Drain-source breakdown voltage	$V_{(BR)DSS}$	20	-	-	V	$I_D=1mA, V_{GS}=0V$
Zero gate voltage drain current	I_{DSS}	-	-	1	μA	$V_{DS}=20V, V_{GS}=0V$
Gate threshold voltage	$V_{GS(th)}$	0.3	-	1	V	$V_{DS}=10V, I_D=1mA$
Static drain-source on-state resistance	$R_{DS(on)}^*$	-	52	72	mΩ	$I_D=2.5A, V_{GS}=4.5V$
		-	65	90		$I_D=2.5A, V_{GS}=2.5V$
		-	85	120		$I_D=1.2A, V_{GS}=1.8V$
		-	100	140		$I_D=0.5A, V_{GS}=1.5V$
Forward transfer admittance	$ Y_{fs} ^*$	2.7	-	-	S	$I_D=2.5A, V_{DS}=10V$
Input capacitance	C_{iss}	-	260	-	pF	$V_{DS}=10V$
Output capacitance	C_{oss}	-	65	-	pF	$V_{GS}=0V$
Reverse transfer capacitance	C_{rss}^*	-	35	-	pF	$f=1MHz$
Turn-on delay time	$t_{d(on)}^*$	-	9	-	ns	$I_D=1.2A, V_{DD}\approx 10V$
Rise time	t_r^*	-	17	-	ns	$V_{GS}=4.5V$
Turn-off delay time	$t_{d(off)}^*$	-	28	-	ns	$R_L\approx 8.3\Omega$
Fall time	t_f^*	-	17	-	ns	$R_G=10\Omega$
Total gate charge	Q_g^*	-	3.6	-	nC	$I_D=2.5A, V_{DD}\approx 10V$
Gate-source charge	Q_{gs}^*	-	0.7	-	nC	$V_{GS}=4.5V, R_L\approx 4\Omega$
Gate-drain charge	Q_{gd}^*	-	0.6	-	nC	$R_G=10\Omega$

*Pulsed

● **Body diode characteristics** (Source-Drain) (Ta = 25°C)

<It is the same characteristics for the Tr1 and Tr2.>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward Voltage	V_{SD}	-	-	1.2	V	$I_s=2.5A, V_{GS}=0V$

*Pulsed

● Electrical characteristic curves

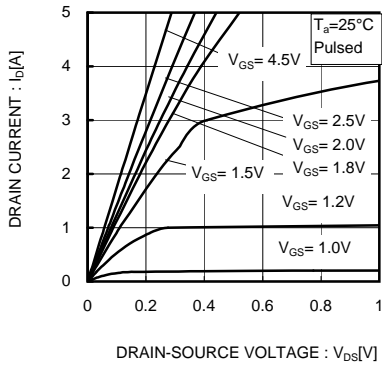


Fig.1 Typical Output Characteristics(I)

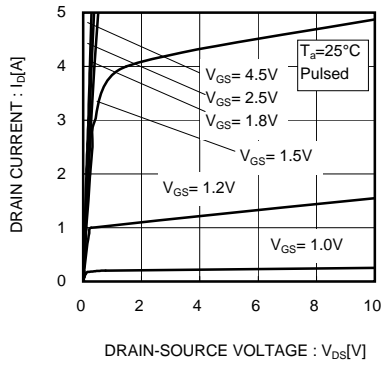


Fig.2 Typical Output Characteristics(II)

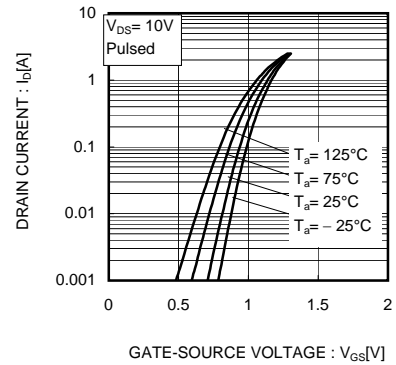


Fig.3 Typical Transfer Characteristics

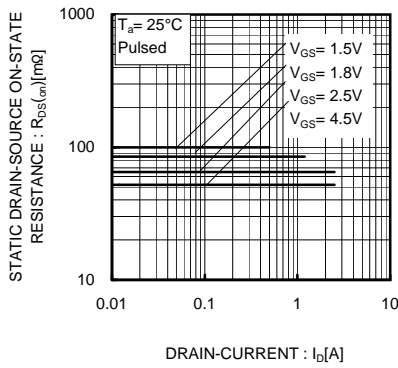


Fig.4 Static Drain-Source On-State Resistance vs. Drain Current(I)

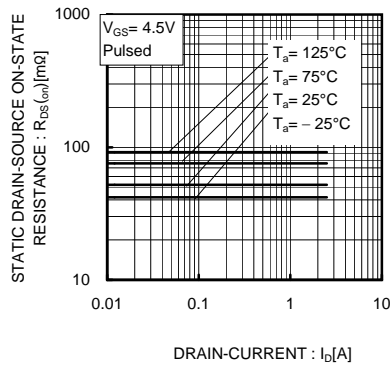


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current(II)

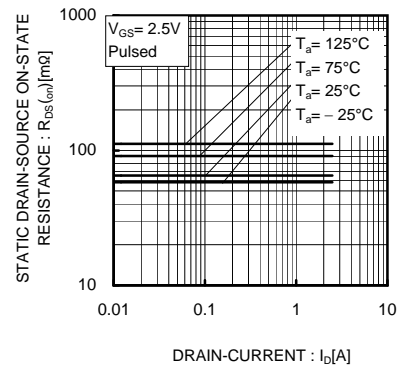


Fig.6 Static Drain-Source On-State Resistance vs. Drain Current(III)

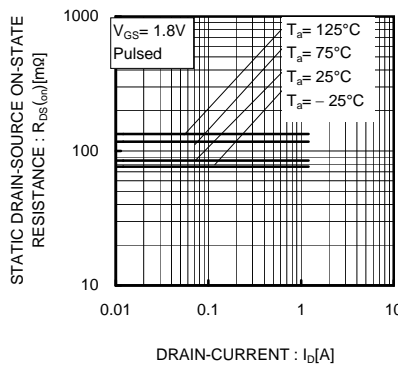


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current(IV)

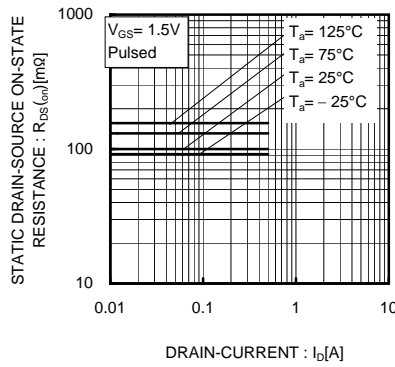


Fig.8 Static Drain-Source On-State Resistance vs. Drain Current(V)

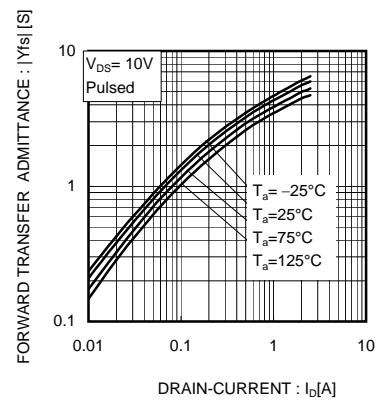
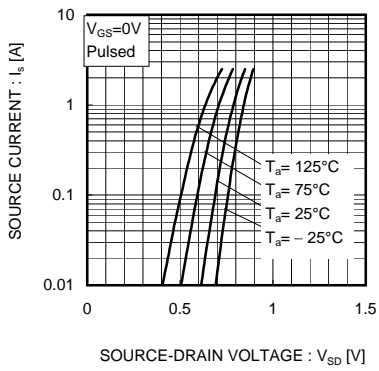
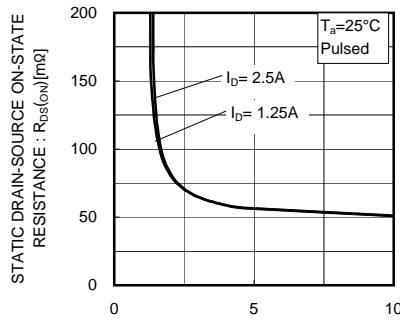


Fig.9 Forward Transfer Admittance vs. Drain Current



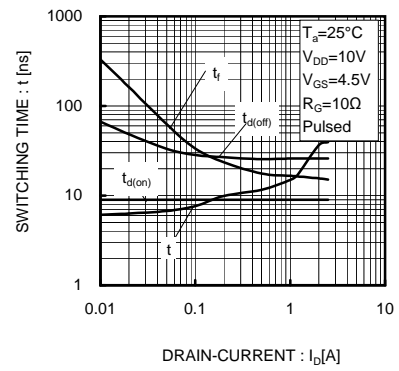
SOURCE-DRAIN VOLTAGE : V_{SD} [V]

Fig.10 Reverse Drain Current vs. Source-Drain Voltage



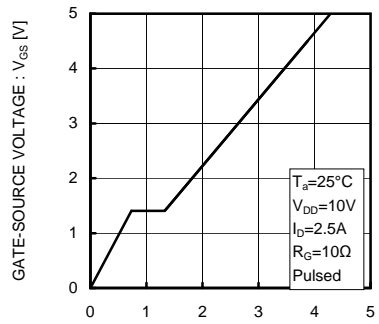
GATE-SOURCE VOLTAGE : V_{GS} [V]

Fig.11 Static Drain-Source On-State Resistance vs. Gate Source Voltage



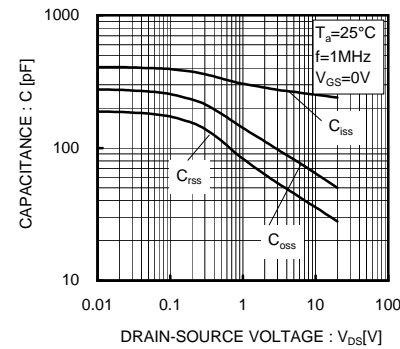
DRAIN-CURRENT : I_D [A]

Fig.12 Switching Characteristics



TOTAL GATE CHARGE : Q_g [nC]

Fig.13 Dynamic Input Characteristics



DRAIN-SOURCE VOLTAGE : V_{DS} [V]

Fig.14 Typical Capacitance vs. Drain-Source Voltage

● Measurement circuits

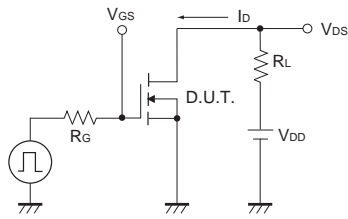


Fig.1-1 Switching time measurement circuit

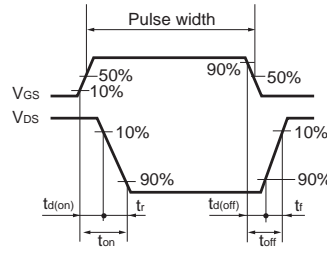


Fig.1-2 Switching waveforms

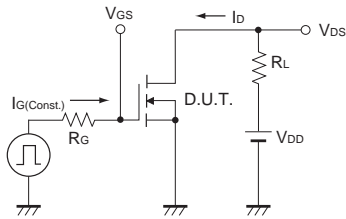


Fig.2-1 Gate charge measurement circuit

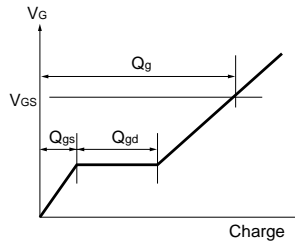


Fig.2-2 Gate Charge Waveform

● Notice

This product might cause chip aging and breakdown under the large electrified environment. Please consider to design ESD protection circuit.

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