LCDP1521

Dual-line programmable transient voltage suppressor for SLIC protection

Features

- dual-line programmable transient voltage suppressor
- wide negative firing voltage range
- V_{MGL} = -150 V max.
- low dynamic switching voltages: V_{FP} and V_{DGL}
- low gate triggering current: I_{GT} = 5 mA max.
- peak pulse current: I_{PP} = 20 A (10/1000 µs)
- holding current: I_H = 150 mA min.

Benefits

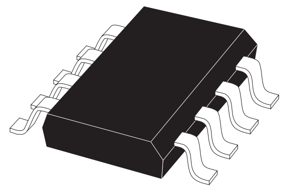
- A Trisil™ is not subject to ageing and provides a fail safe mode in short circuit for better protection.
- Trisils are used to help equipment meet various standards such as UL1950, IEC 950 / CSA C22.2, UL1459 and FCC part68.
- Trisils have UL94 V0 approved resin.
- Trisils are UL497B approved (file: E136224).

Description

This device has been designed to protect 2 new high voltage, as well as classical SLICs against transient overvoltages.

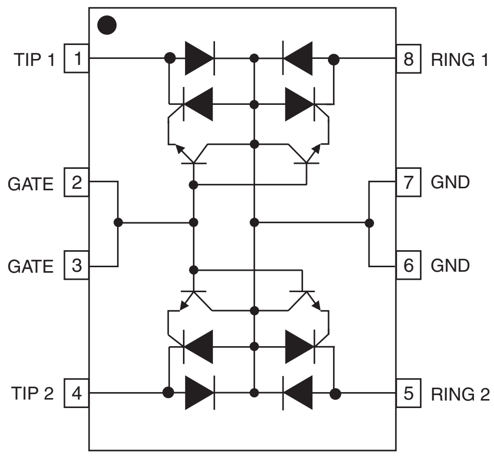
Positive overvoltages are clamped by 2 diodes. Negative surges are suppressed by 2 thyristors, their breakdown voltage being referenced to $-V_{BAT}$ through the gate.

This component presents a very low gate triggering current (I_{GT}) to reduce the current consumption on printed circuit boards during the firing phase.



SO-8

Figure 1. Functional diagram



TM: Trisil is a trademark of STMicroelectronics

1 Compliant with the following standards

Table 1. Compliant with the following standards

Standard	Peak surge voltage (V)	Voltage waveform	Required peak current (A)	Current waveform	Minimum serial resistor to meet standard (Ω)
GR-1089 Core First level	2500 1000	2/10 µs 10/1000 µs	500 100	2/10 µs 10/1000 µs	31 40
GR-1089 Core Second level	5000	2/10 µs	500	2/10 µs	62
GR-1089 Core Intra-building	1500	2/10 µs	100	2/10 µs	7
ITU-T-K20/K21	6000 1500	10/700 µs	150 37.5	5/310 µs	200 20
ITU-T-K20 (IEC 61000-4-2)	8000 15000	1/60 ns	ESD contact discharge ESD air discharge		0 0
VDE0433	4000 2000	10/700 µs	100 50	5/310 µs	120 40
VDE0878	4000 2000	1.2/50 µs	100 50	1/20 µs	27 0
IEC 61000-4-5	4000 4000	10/700 µs 1.2/50 µs	100 100	5/310 µs 8/20 µs	120 27
FCC Part 68, lightning surge type A	1500 800	10/160 µs 10/560 µs	200 100	10/160 µs 10/560 µs	43 32
FCC Part 68, lightning surge type B	1000	9/720 µs	25	5/320 µs	0

2 Characteristics

Table 2. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{th\ (j-a)}$	Junction to ambient	170	°C/W

Figure 2. Electrical characteristics (T_{amb} = 25 °C)

Symbol	Parameter
I_{GT}	Gate triggering current
I_H	Holding current
I_{RM}	Reverse leakage current line / GND
I_{RG}	Reverse leakage current gate / line
V_{RM}	Reverse voltage line / GND
V_{GT}	Gate triggering voltage
V_F	Forward drop voltage line / GND
V_{FP}	Peak forward voltage line / GND
V_{DGL}	Dynamic switching voltage gate / Line
V_{GATE}	Gate / Gnd voltage
V_{RG}	Reverse voltage gate / Line
C	Capacitance line / GND

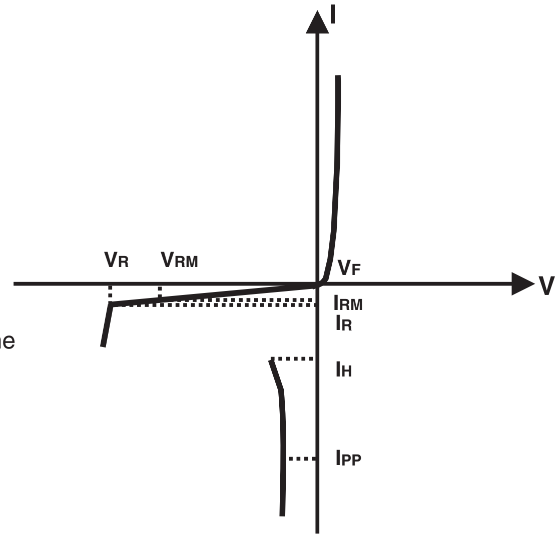


Table 3. Absolute ratings (T_{amb} = 25 °C, unless otherwise specified)

Symbol	Parameter		Value	Unit
I_{PP}	Peak pulse current(1)	10/1000 µs 8/20 µs 10/560 µs 5/310 µs 10/160 µs 1/20 µs 2/10 µs	20 60 20 25 30 60 70	A
I_{TSM}	Non repetitive surge peak on-state current (50 Hz sinusoidal)	t = 10 ms t = 1 s	5 3.5	A
I^2t	I^2t value for fusing (50 Hz sinusoidal)	t = 10 ms	0.125	A^2s
I_{GSM}	Maximum gate current (50 Hz sinusoidal)	t = 10 ms	2	A
V_{MLG} V_{MGL}	Maximum voltage LINE/GND Maximum voltage GATE/LINE	-40 °C < T_{amb} < +85 °C -40 °C < T_{amb} < +85 °C	-150 -150	V
T_{stg} T_j	Storage temperature range Maximum junction temperature		- 55 to + 150 150	°C
T_L	Maximum lead temperature for soldering during 10 s		260	°C

1. For pulse waveform see *Figure 3*.

Figure 3. Repetitive peak pulse current

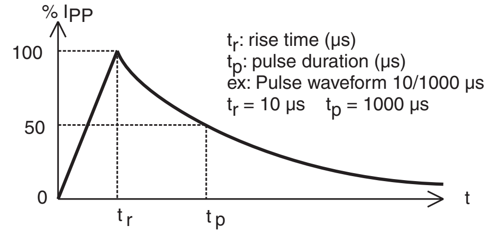


Table 4. Parameters related to the diode line / GND (T_{amb} = 25 °C)

Symbol	Test conditions				Max	Unit
V_F	I_F = 1 A		t = 500 µs		2	V
V_{FP}(1)	10/700 µs	1.5 kV	R_S = 110 Ω	I_{PP} = 10 A	5	V
	1.2/50 µs	1.5 kV	R_S = 60 Ω	I_{PP} = 15 A	10	
	2/10 µs	2.5 kV	R_S = 245 Ω	I_{PP} = 10 A	20	

1. See *Figure 5: Test circuit for V_{FP} and V_{DGL} parameters*. R_S is the protection resistor located on the line card.

Table 5. Parameters related to the protection thyristor (T_{amb} = 25°C unless otherwise specified)

Symbol	Test conditions				Min	Max	Unit
I_{GT}	$V_{GND / LINE}$ = -48 V				0.1	5	mA
I_H	V_{GATE} = -48 V(1)				150		mA
V_{GT}	At I_{GT}					2.5	V
I_{RG}	V_{RG} = -150 V			T_c = 25 °C		5	µA
	V_{RG} = -150 V			T_c = 85 °C		50	
V_{DGL}	V_{GATE} = -48 V(2)						V
	10/700 µs	1.5 kV	R_S = 110 Ω	I_{PP} = 10 A		5	
	1.2/50 µs	1.5 kV	R_S = 60 Ω	I_{PP} = 15 A		10	
	2/10 µs	2.5 kV	R_S = 245 Ω	I_{PP} = 10 A		20	

1. See *Figure 4: Functional holding current (I_H) test circuit: go no-go test*
2. See *Figure 5: Test circuit for V_{FP} and V_{DGL} parameters*. The oscillations with a time duration lower than 50 ns are not taken into account

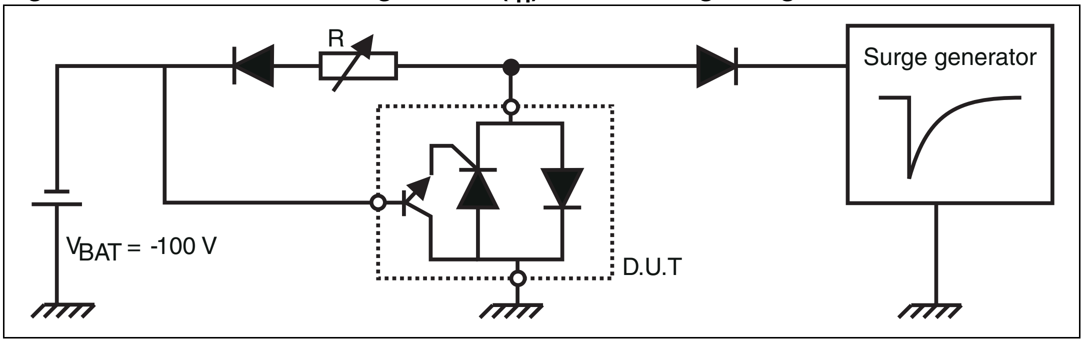
Table 6. Parameters related to diode and protection thyristor (T_{amb} = 25 °C, unless otherwise specified)

Symbol	Test conditions		Typ.	Max.	Unit
I_{RM}	$V_{GATE / LINE}$ = -1 V V_{RM} = -150 V	T_c = 25 °C		5	µA
	$V_{GATE / LINE}$ = -1 V V_{RM} = -150 V	T_c = 85 °C		50	
C	V_R = 50 V bias, V_{RMS} = 1 V, F = 1 MHz		20		pF
	V_R = 2 V bias, V_{RMS} = 1 V, F = 1 MHz		48		

3 Test circuits

3.1 Functional holding current (I_H): go no-go test

Figure 4. Functional holding current (I_H) test circuit: go no-go test



This is a go no-go test, which confirms the holding current (IH) level in a functional test circuit.

3.1.1 Test procedure

- Adjust the current level at the I_H value by short circuiting the D.U.T.
- Fire the D.U.T. with a surge current: I_{PP} = 10 A, 10/1000 µs.

The D.U.T. will come back to the off-state within a duration of 50 ms max.

3.2 Test circuit for V_{FP} and V_{DGL} parameters

Figure 5. Test circuit for V_{FP} and V_{DGL} parameters

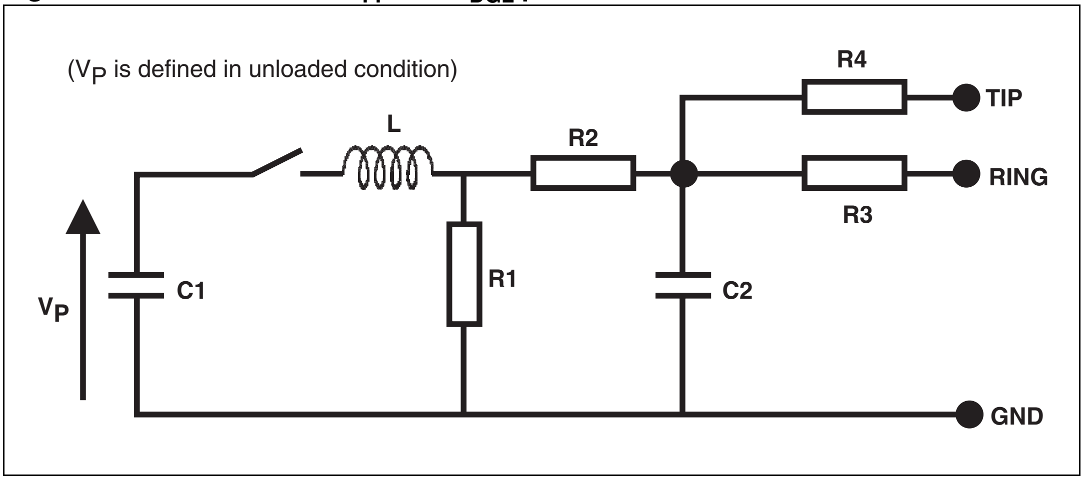


Table 7. Test circuit component values

Pulse (µs)		V_p	C_1	C_2	L	R_1	R_2	R_3	R_4	I_{PP}	R_s
t_r	t_p	(V)	(µF)	(nF)	(µH)	(Ω)	(Ω)	(Ω)	(Ω)	(A)	(Ω)
10	700	1500	20	200	0	50	15	25	25	10	110
1.2	50	1500	1	33	0	76	13	25	25	15	60
2	10	2500	10	0	1.1	1.3	0	3	3	10	245

4 Technical information

Figure 6. LCDP1521 concept behavior

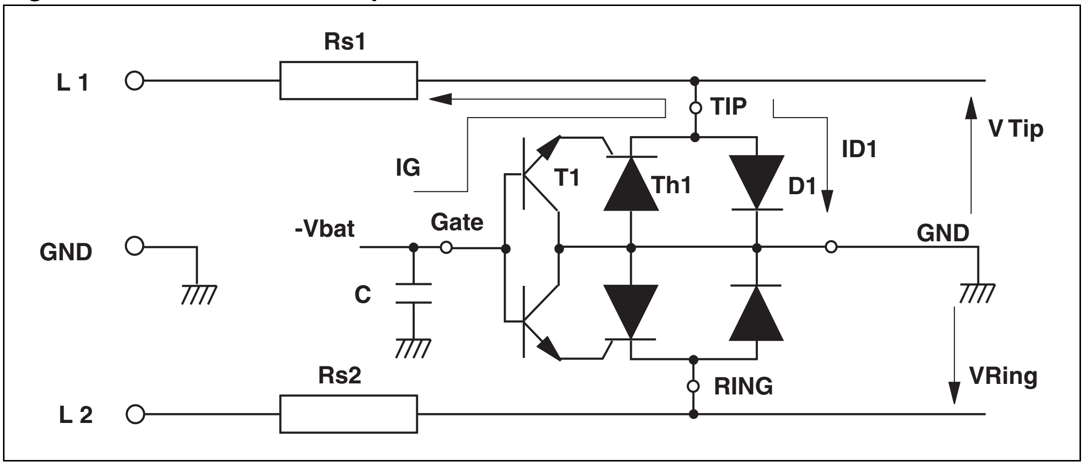


Figure 6 shows the classic protection circuit using the LCDP1521 crowbar concept. This topology has been developed to protect the new high voltage SLICs. This supports the programming of the negative firing threshold while the positive clamping value is fixed at GND.

When a negative surge occurs on one wire (L1 for example), a current I_G flows through the base of the transistor T1 and then injects a current in the gate of the thyristor Th1. Th1 fires and all the surge current flows through the ground. After the surge when the current flowing through Th1 becomes less negative than the holding current I_H, then Th1 switches off.

When a positive surge occurs on one wire (L1 for example), the diode D1 conducts and the surge current flows through the ground.

The capacitor C is used to speed up the crowbar structure firing during the fast surge edges.

This minimizes the dynamic breakover voltage at the SLIC Tip and Ring inputs during fast strikes. Note that this capacitor is generally present around the SLIC - V_{BAT} pin.

So, to be efficient, it has to be as close as possible to the LCDP1521 Gate pin and to the reference ground track (or plan). The optimized value for C is 220 nF.

The series resistors Rs1 and Rs2 in *Figure 6* represent the fuse resistors or the PTC which are mandatory to withstand the power contact or the power induction tests imposed by the various country standards. Taking into account this fact, the actual lightning surge current flowing through the LCDP is equal to:

$I_{surge} = V_{surge} / (Rg + Rs)$

With:

V_{surge} = peak surge voltage imposed by the standard.

Rg = series resistor of the surge generator

Rs = series resistor of the line card (equivalent to PTC + R in *Figure 7*)

Example: For a line card with 60 Ω of series resistors, which has to be qualified under GR-1089 Core 1000 V, 10/1000µs surge, the actual current through the LCDP1521 is equal to:

I_{surge} = 1000 / (10 + 60) = **14 A**

The LCDP1521 is particularly optimized for the new telecom applications such as the fiber in the loop, the WLL, and the remote central office. In this case the operating voltages are smaller than in the classic system. This makes the high voltage SLICs particularly suitable. The schematics of *Figure 7* show the topologies most frequently used for these applications.

Figure 7. Protection of high voltage SLICs

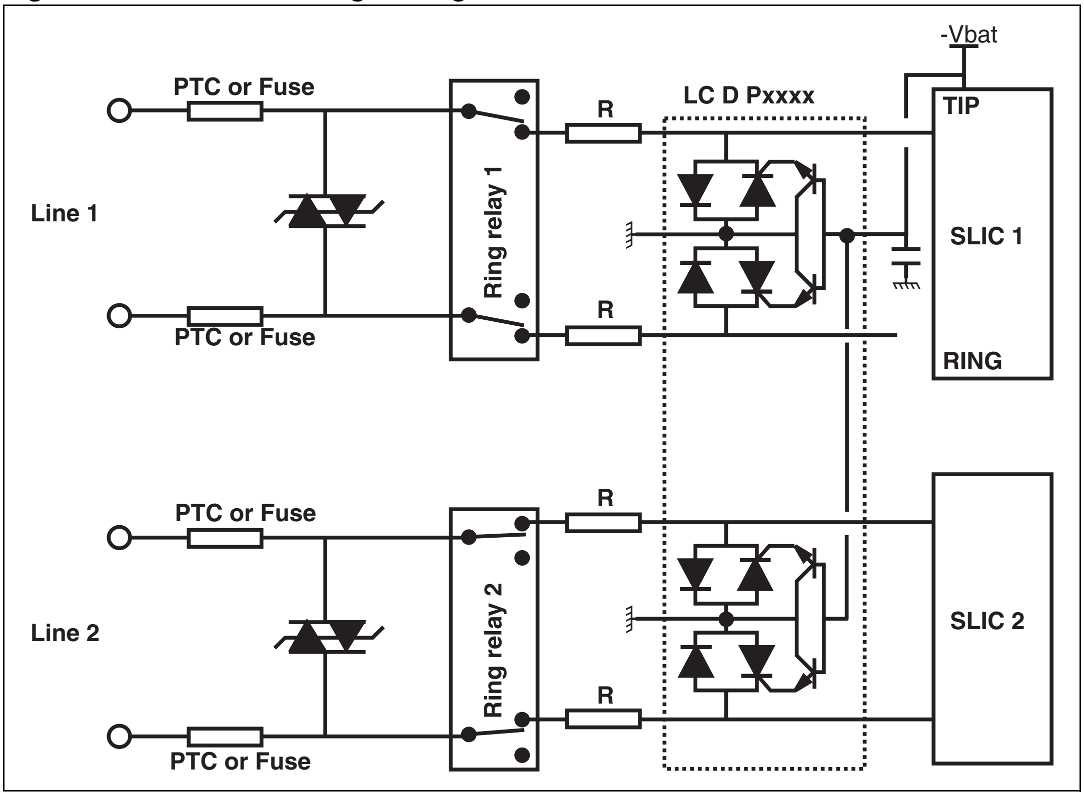


Figure 8. Surge peak current versus overload duration.

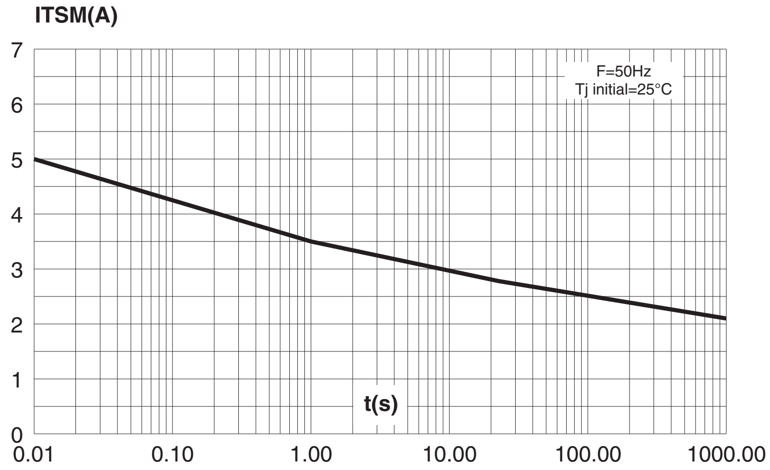
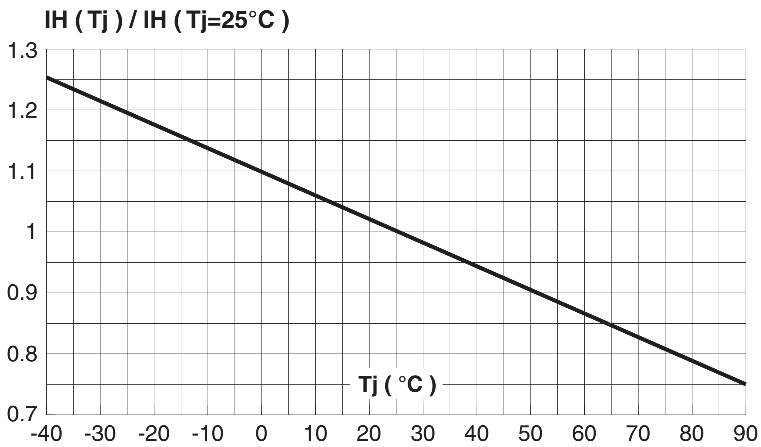
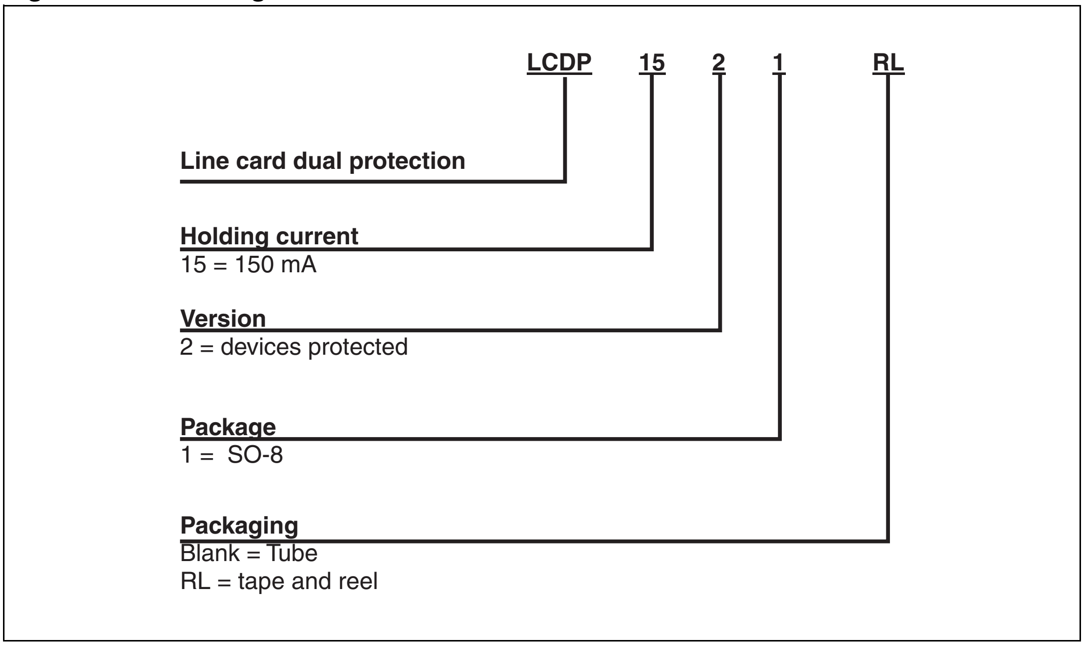


Figure 9. Relative variation of holding current versus junction temperature



5 Ordering information scheme

Figure 10. Ordering information scheme

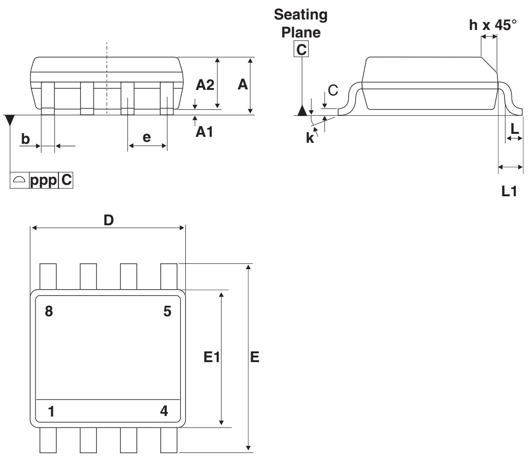


6 Package information

- Epoxy meets UL94, V0
- Lead-free package

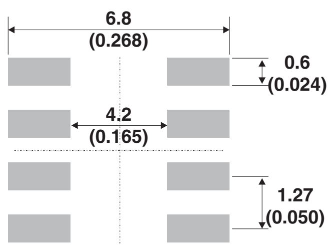
In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Table 8. SO-8 dimensions



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
A1	0.1		0.25	0.004		0.010
A2	1.25			0.049		
b	0.28		0.48	0.011		0.019
C	0.17		0.23	0.007		0.009
D	4.80	4.90	5.00	0.189	0.193	0.197
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e		1.27			0.050	
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
L1		1.04			0.041	
k	0°		8°	0°		8°
ppp			0.10			0.004

Figure 11. Footprint, dimensions in mm (inches)



7 Ordering Information

Table 9. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
LCDP1521	CDP152	SO-8	0.08 g	100	Tube
LCDP1521RL[1]				2500	Tape and reel

1. Preferred device

8 Revision history

Table 10. Document revision history

Date	Revision	Changes
March 2002	1	Initial release.
24-Jun-2005	2	Peak pulse current changed from 15 to 20 A (10/1000 µs)
07-Feb-2006	3	Added footnote to ordering information table
20-Oct-2010	4	Updated ECOPACK statement. Updated trademark statement.

Please Read Carefully: