

N-channel 100 V, 8 mΩ typ., 120 A, STripFET™ DeepGATE™
Power MOSFETs in D²PAK and TO-220 packages

Datasheet – production data

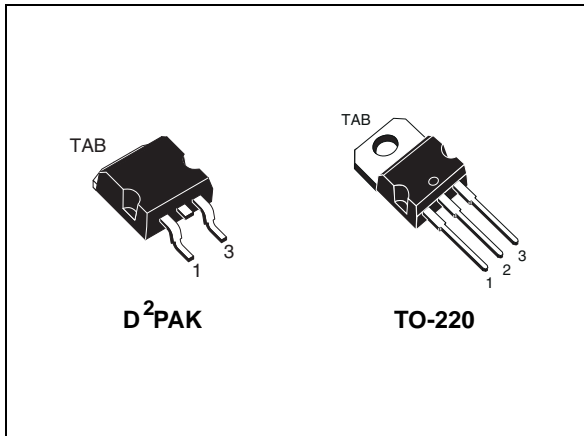
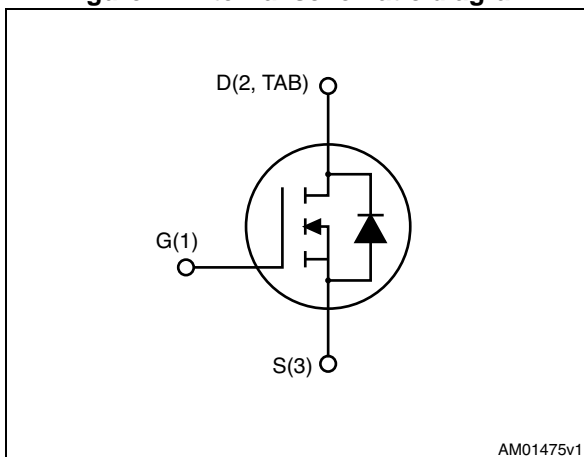


Figure 1. Internal schematic diagram



Features

Order codes	V _{DS}	R _{DS(on)} max.	I _D
STB120N10F4	100 V	10 mΩ	120 A
STP120N10F4			

- N-channel enhancement mode
- Very low on-resistance
- Low gate charge
- 100% avalanche rated

Applications

- Switching applications

Description

These devices are N-channel Power MOSFETs developed using ST's STripFET™ DeepGATE™ technology. The devices have a new gate structure and are specially designed to minimize on-state resistance to provide superior switching performance.

Table 1. Device summary

Order codes	Marking	Packages	Packaging
STB120N10F4	120N10F4	D ² PAK	Tape and reel
STP120N10F4		TO-220	Tube

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	100	V
V_{GS}	Gate-source voltage	± 20	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	120	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	85	A
$I_{DM}^{(1)}$	Drain current (pulsed)	390	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	300	W
	Derating factor	2	W/ $^\circ\text{C}$
$E_{AS}^{(2)}$	Single pulse avalanche energy	215	mJ
T_{stg}	Storage temperature	- 55 to 175	$^\circ\text{C}$
T_j	Max. operating junction temperature		

1. Pulse width limited by safe operating area
2. Starting $T_j = 25\text{ }^\circ\text{C}$, $I_D = 65\text{ A}$, $V_{DD} = 50\text{ V}$

Table 3. Thermal data

Symbol	Parameter	Value		Unit
		D ² PAK	TO-220	
$R_{thj-case}$	Thermal resistance junction-case max	0.5		$^\circ\text{C/W}$
$R_{thj-pcb}$	Thermal resistance junction-pcb max	35		$^\circ\text{C/W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max		62.5	$^\circ\text{C/W}$

2 Electrical characteristics

($T_{CASE} = 25\text{ °C}$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown voltage	$I_D = 250\ \mu\text{A}, V_{GS} = 0$	100			V
I_{DSS}	Zero gate voltage Drain current ($V_{GS} = 0$)	$V_{DS} = 100\ \text{V}$			1	μA
		$V_{DS} = 100\ \text{V}, T_C = 125\text{ °C}$			100	μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20\ \text{V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	2		4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\ \text{V}, I_D = 60\ \text{A}$		8	10	m Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 25\ \text{V}, f = 1\ \text{MHz}, V_{GS} = 0$	-	7290	-	pF
C_{oss}	Output capacitance		-	568	-	pF
C_{rss}	Reverse transfer capacitance		-	387	-	pF
Q_g	Total gate charge	$V_{DD} = 50\ \text{V}, I_D = 120\ \text{A}, V_{GS} = 10\ \text{V}$ (see Figure 14)	-	131	-	nC
Q_{gs}	Gate-source charge		-	40	-	nC
Q_{gd}	Gate-drain charge		-	37	-	nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 50\ \text{V}, I_D = 60\ \text{A}, R_G = 4.7\ \Omega, V_{GS} = 10\ \text{V}$ (see Figure 13)	-	32	-	ns
t_r	Rise time		-	116	-	ns
$t_{d(off)}$	Turn-off-delay time	$V_{DD} = 50\ \text{V}, I_D = 60\ \text{A}, R_G = 4.7\ \Omega, V_{GS} = 10\ \text{V}$ (see Figure 13)	-	111	-	ns
t_f	Fall time		-	79	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		120	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		390	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 60 \text{ A}$, $V_{GS} = 0$	-		1.2	V
t_{rr}	Reverse recovery time	$I_{SD} = 120 \text{ A}$, $V_{DD} = 80 \text{ V}$ $di/dt = 100 \text{ A}/\mu\text{s}$, $T_j = 150 \text{ }^\circ\text{C}$ <i>(see Figure 15)</i>	-	72		ns
Q_{rr}	Reverse recovery charge		-	215		nC
I_{RRM}	Reverse recovery current		-	6		A

1. Pulse width limited by safe operating area.

2. Pulsed: Pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

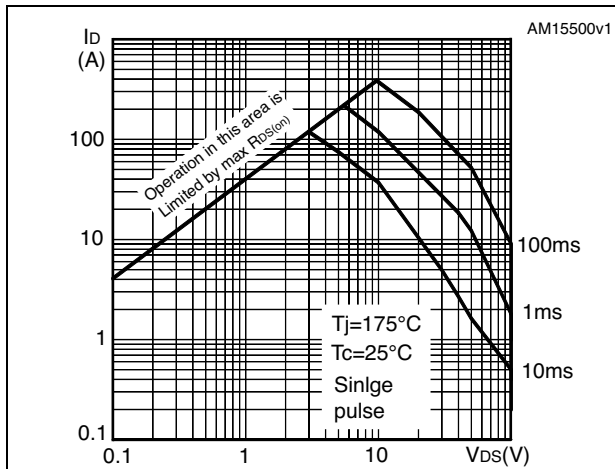


Figure 3. Thermal impedance

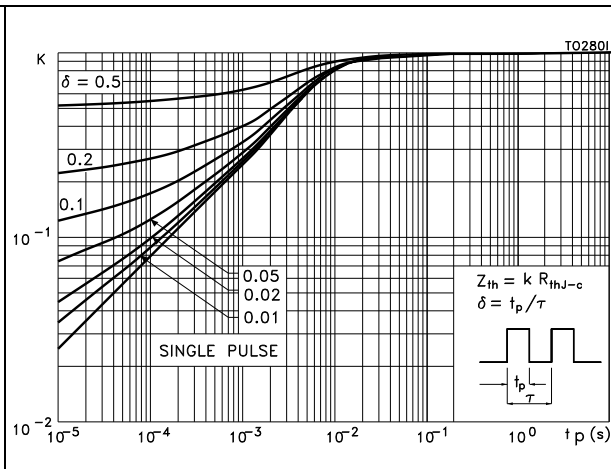


Figure 4. Output characteristics

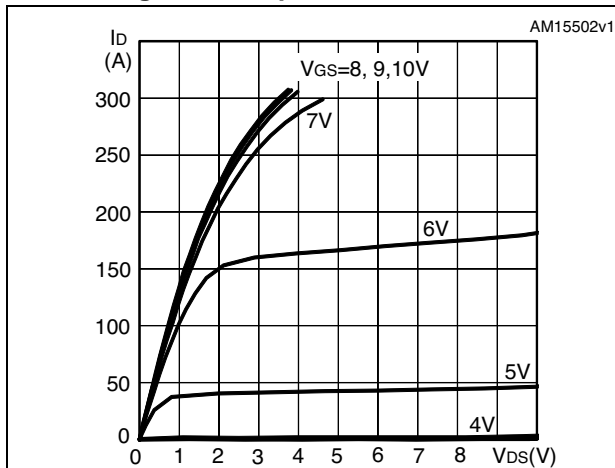


Figure 5. Transfer characteristics

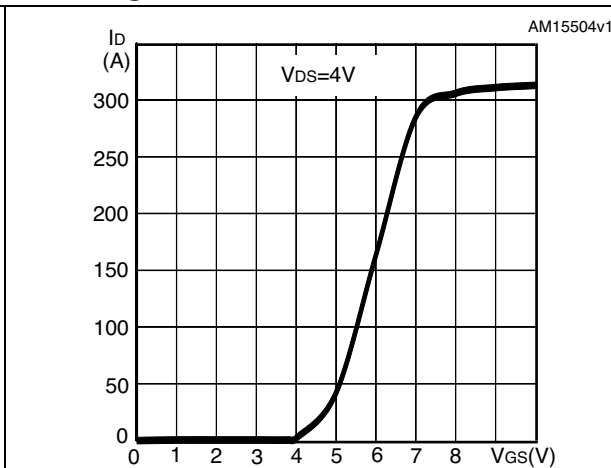


Figure 6. Gate charge vs gate-source voltage

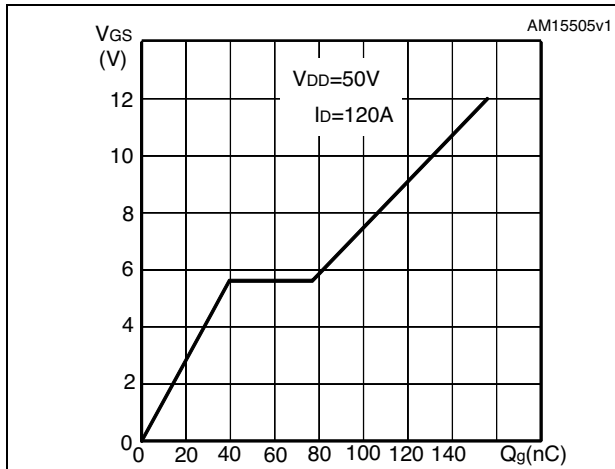


Figure 7. Static drain-source on-resistance

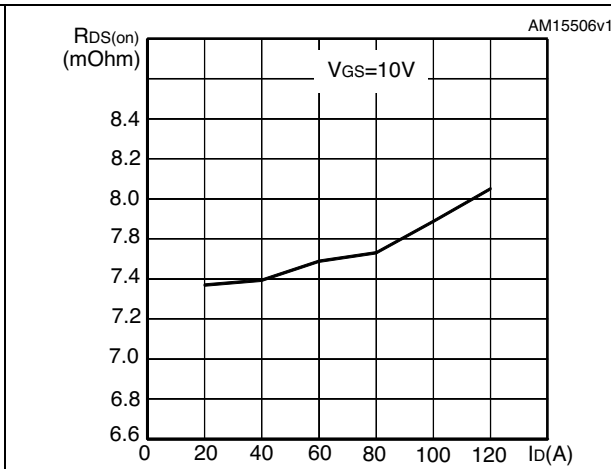


Figure 8. Capacitance variations

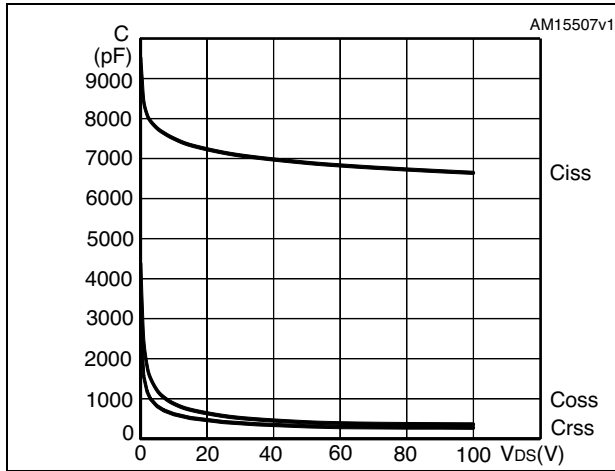


Figure 9. Source-drain diode forward characteristics

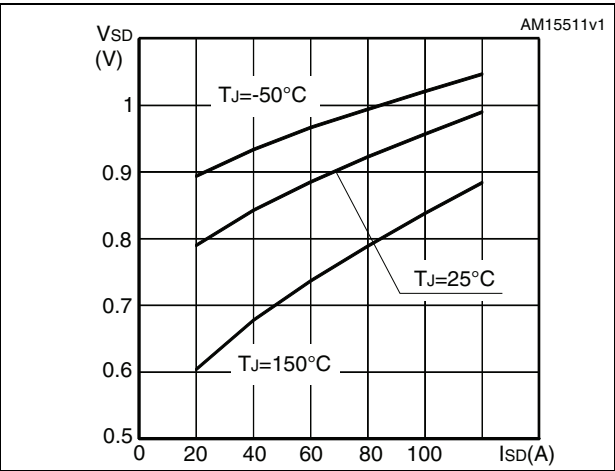


Figure 10. Normalized gate threshold voltage vs temperature

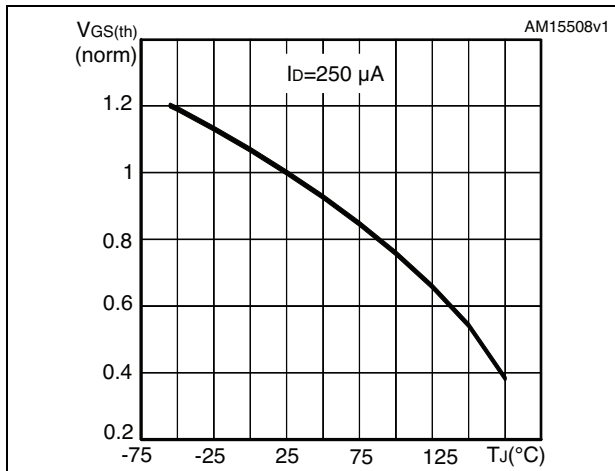


Figure 11. Normalized on-resistance vs temperature

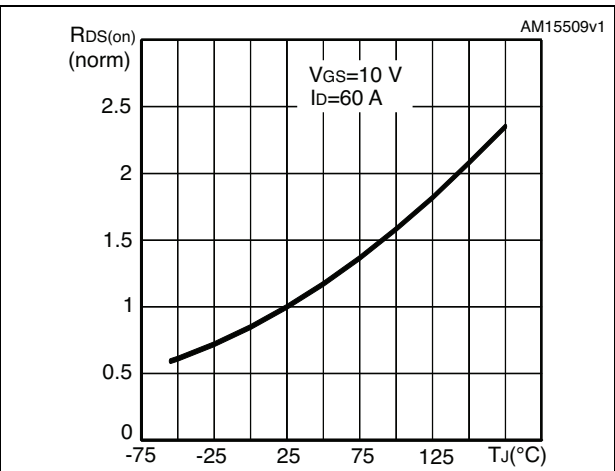
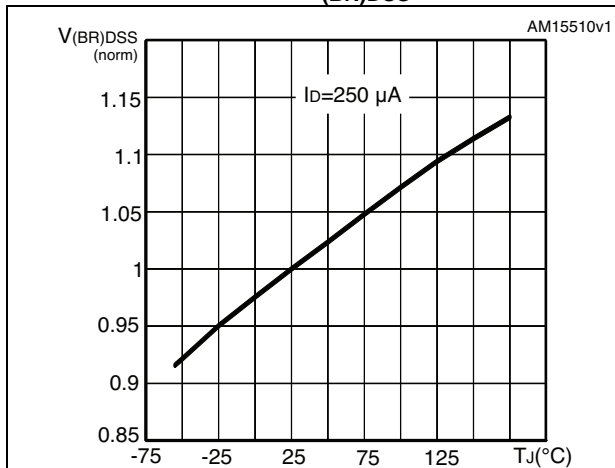


Figure 12. Normalized $V_{(BR)DSS}$ vs temperature



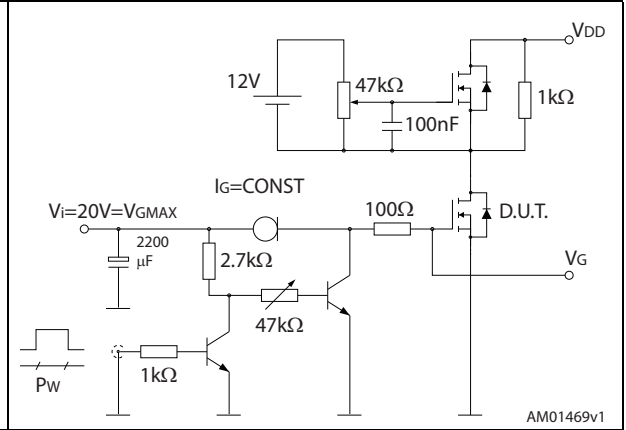
3 Test circuits

Figure 13. Switching times test circuit for resistive load



AM01468v1

Figure 14. Gate charge test circuit



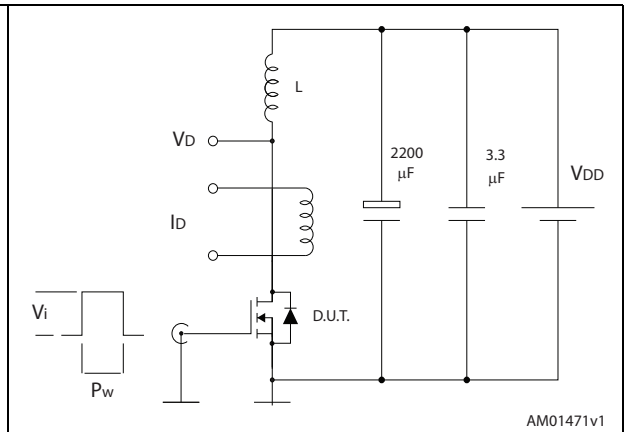
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Figure 15. Test circuit for inductive load switching and diode recovery times



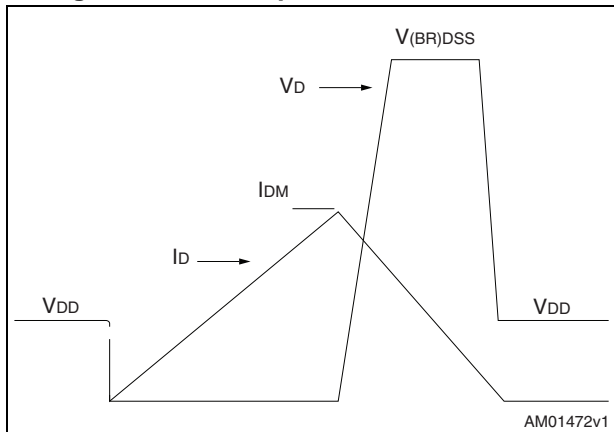
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Figure 16. Unclamped inductive load test circuit



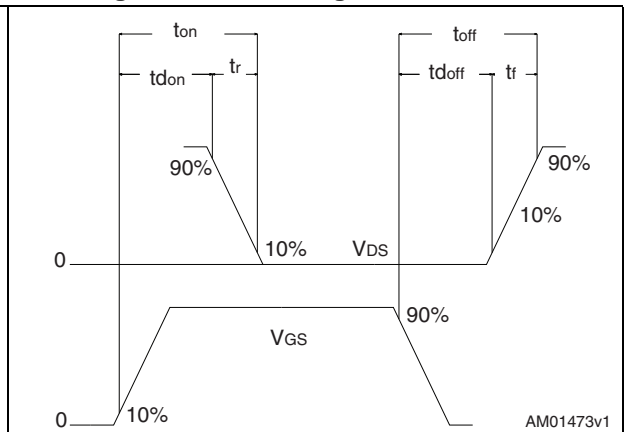
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Figure 17. Unclamped inductive waveform



AM01472v1

Figure 18. Switching time waveform



AM01473v1

4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

4.1 D²PAK, STB120N10F4

Figure 19. D²PAK (TO-263) drawing

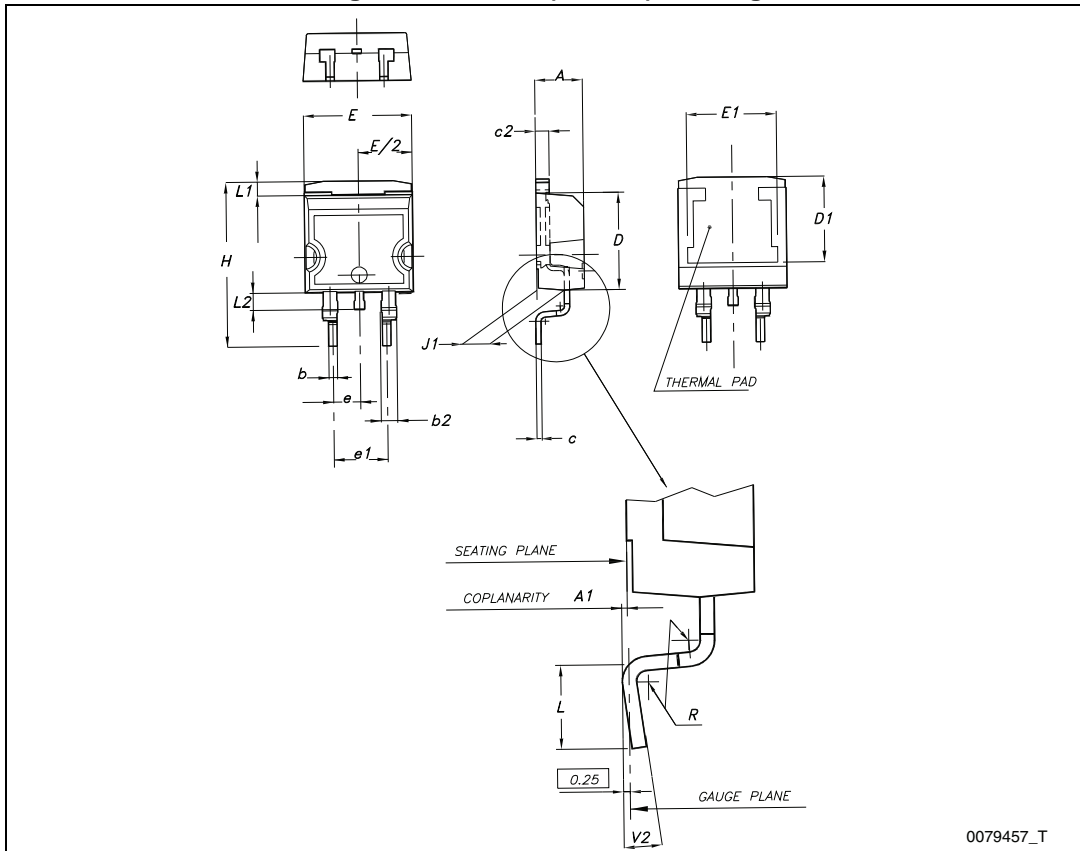
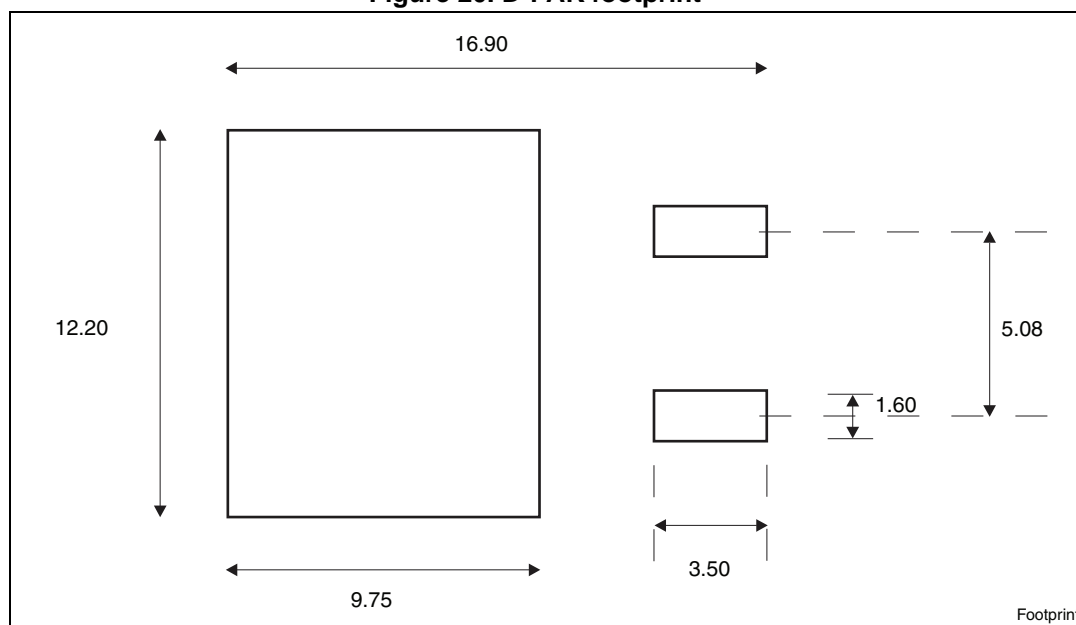


Table 8. D²PAK (TO-263) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50		
E	10		10.40
E1	8.50		
e		2.54	
e1	4.88		5.28
H	15		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.4	
V2	0°		8°

Figure 20. D²PAK footprint^(a)



a. All dimension are in millimeters

4.2 TO-220, STP120N10F4

Figure 21. TO-220 type A drawing

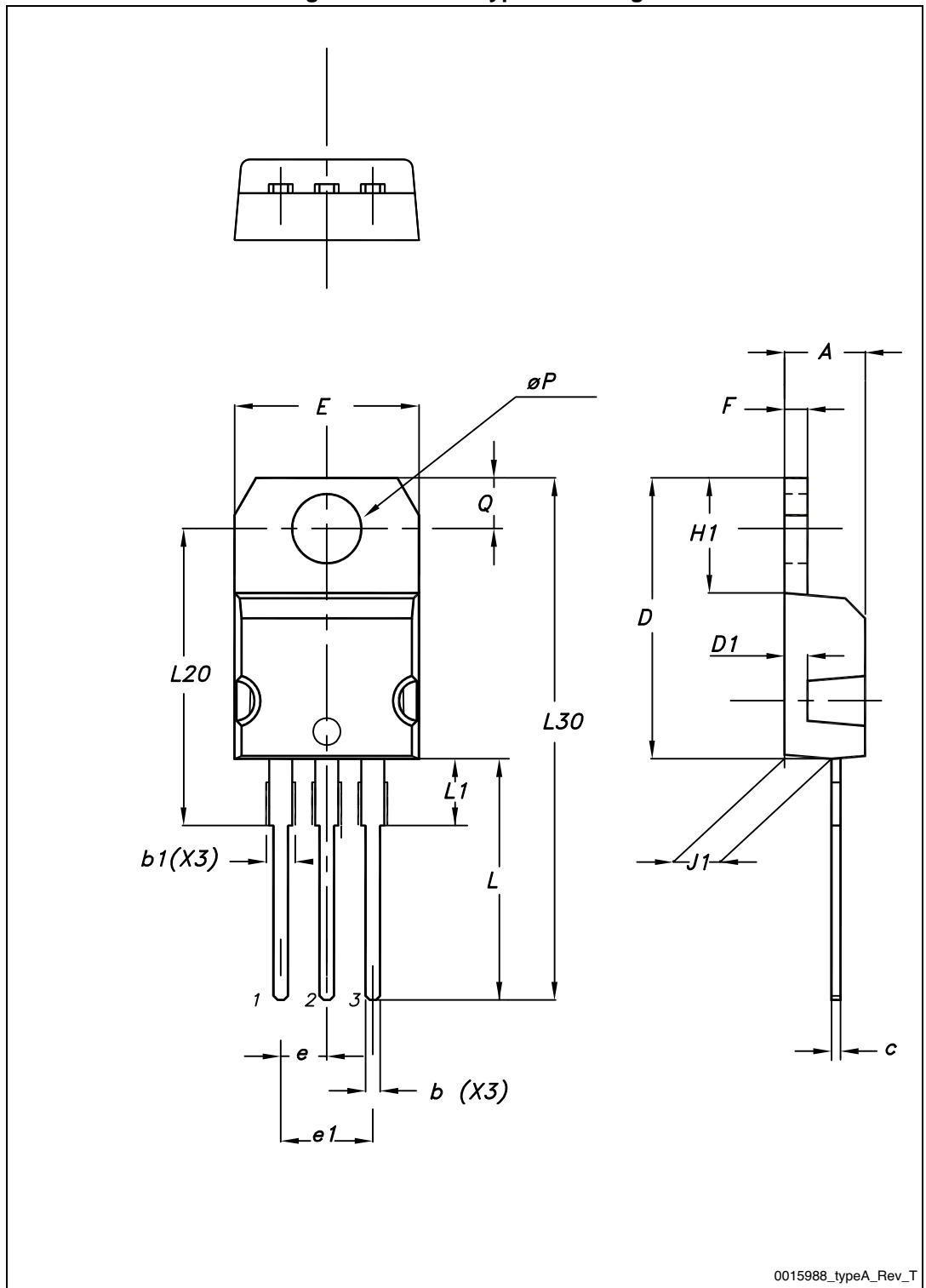


Table 9. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
\overline{AEP}	3.75		3.85
Q	2.65		2.95

5 Packaging mechanical data

Figure 22. Tape

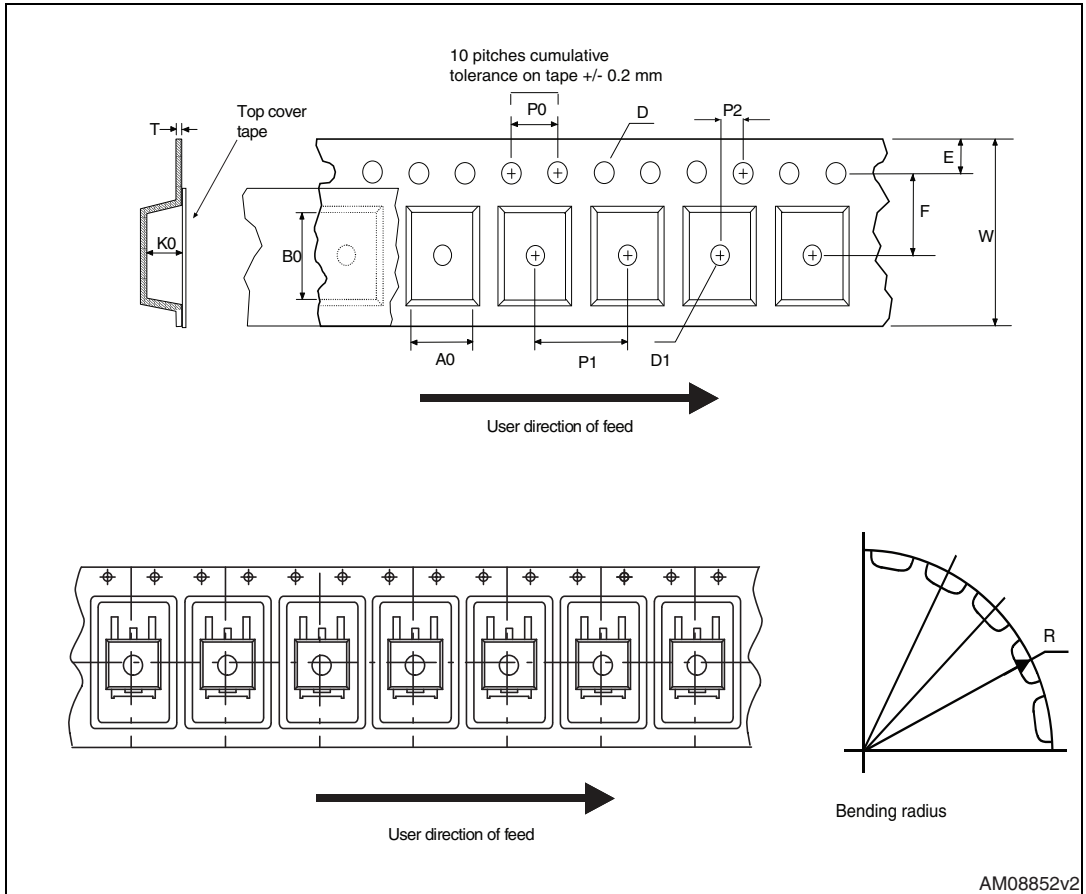


Figure 23. Reel

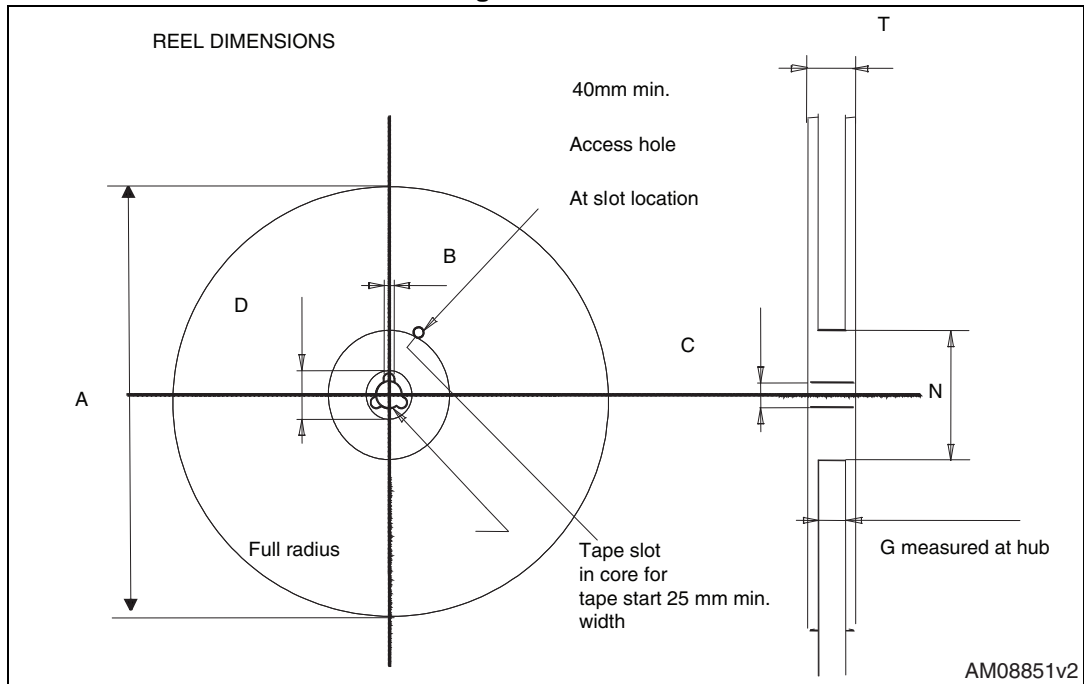


Table 10. D²PAK (TO-263) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base qty		1000
P2	1.9	2.1	Bulk qty		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

6 Revision history

Table 11. Document revision history

Date	Revision	Changes
02-Apr-2014	1	First release.

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