

N-channel 650 V, 0.79  $\Omega$  typ., 5 A MDmesh M2 Power MOSFETs  
in DPAK, TO-220FP, TO-220 and IPAK packages

Datasheet - production data

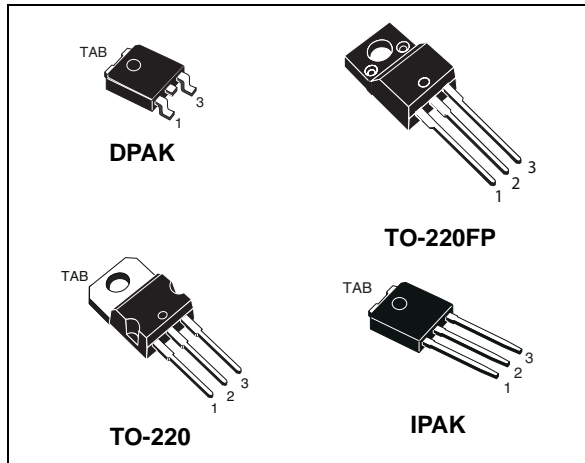
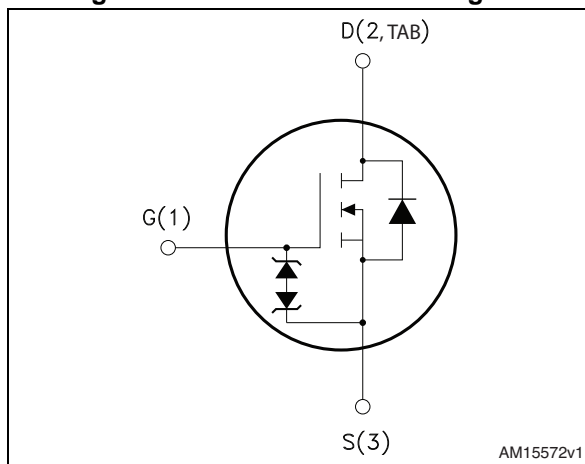


Figure 1. Internal schematic diagram



## Features

Order codes	$V_{DS}$	$R_{DS(on)max}$	$I_D$
STD9N65M2	650 V	0.9 $\Omega$	5 A
STF9N65M2			
STP9N65M2			
STU9N65M2			

- Extremely low gate charge
- Excellent output capacitance ( $C_{OSS}$ ) profile
- 100% avalanche tested
- Zener-protected

## Applications

- Switching applications

## Description

These devices are N-channel Power MOSFETs developed using the MDmesh™ M2 technology. Thanks to the strip layout associated to an improved vertical structure, the devices exhibit both low on-resistance and optimized switching characteristics. They are therefore suitable for the most demanding high efficiency converters.

Table 1. Device summary

Order codes	Marking	Package	Packaging
STD9N65M2	9N65M2	DPAK	Tape and reel
STF9N65M2		TO-220FP	Tube
STP9N65M2		TO-220	
STU9N65M2		IPAK	

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value		Unit
		DPAK, TO-220, IPAK	TO-220FP	
V <sub>GS</sub>	Gate-source voltage	± 25		V
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> = 25 °C	5	5 <sup>(1)</sup>	A
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> = 100 °C	3.2	3.2 <sup>(1)</sup>	A
I <sub>DM</sub> <sup>(2)</sup>	Drain current (pulsed)	20		A
P <sub>TOT</sub>	Total dissipation at T <sub>C</sub> = 25 °C	60	20	W
V <sub>ISO</sub>	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1 s; T <sub>C</sub> =25 °C)		2500	V
dv/dt <sup>(3)</sup>	Peak diode recovery voltage slope	15		V/ns
dv/dt <sup>(4)</sup>	MOSFET dv/dt ruggedness	50		
T <sub>stg</sub>	Storage temperature	- 55 to 150		°C
T <sub>j</sub>	Max. operating junction temperature	150		

1. Current limited by package.
2. Pulse width limited by safe operating area.
3. I<sub>SD</sub> ≤ 5 A, di/dt ≤ 400 A/μs; V<sub>DS peak</sub> < V<sub>(BR)DSS</sub>, V<sub>DD</sub>=400 V
4. V<sub>DS</sub> ≤ 520 V

**Table 3. Thermal data**

Symbol	Parameter	Value				Unit
		DPAK	TO-220FP	TO-220	IPAK	
R <sub>thj-case</sub>	Thermal resistance junction-case max	2.08	6.25	2.08		°C/W
R <sub>thj-pcb</sub> <sup>(1)</sup>	Thermal resistance junction-pcb max	50				°C/W
R <sub>thj-amb</sub>	Thermal resistance junction-ambient max		62.5		100	°C/W

1. When mounted on 1 inch<sup>2</sup> FR-4, 2 Oz copper board

**Table 4. Avalanche characteristics**

Symbol	Parameter	Value	Unit
I <sub>AR</sub>	Avalanche current, repetitive or not repetitive (pulse width limited by T <sub>jmax</sub> )	1	A
E <sub>AS</sub>	Single pulse avalanche energy (starting T <sub>j</sub> =25°C, I <sub>D</sub> = I <sub>AR</sub> ; V <sub>DD</sub> =50)	105	mJ

## 2 Electrical characteristics

( $T_C = 25\text{ °C}$  unless otherwise specified)

**Table 5. On /off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0, I_D = 1\text{ mA}$	650			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0, V_{DS} = 650\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0, V_{DS} = 650\text{ V}, T_C = 125\text{ °C}$			100	$\mu\text{A}$
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0, V_{GS} = \pm 25\text{ V}$			$\pm 10$	$\mu\text{A}$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}, I_D = 2.5\text{ A}$		0.79	0.9	$\Omega$

**Table 6. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 100\text{ V}, f = 1\text{ MHz}, V_{GS} = 0$	-	315	-	pF
$C_{oss}$	Output capacitance		-	18	-	pF
$C_{riss}$	Reverse transfer capacitance		-	1	-	pF
$C_{oss\ eq}^{(1)}$	Equivalent output capacitance	$V_{GS} = 0, V_{DS} = 0\text{ to }520\text{ V}$	-	109	-	pF
$R_G$	Intrinsic gate resistance	$f = 1\text{ MHz open drain}$	-	6.6	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 520\text{ V}, I_D = 5\text{ A}, V_{GS} = 10\text{ V}$ (see <a href="#">Figure 19</a> )	-	10	-	nC
$Q_{gs}$	Gate-source charge		-	2.5	-	nC
$Q_{gd}$	Gate-drain charge		-	5	-	nC

1.  $C_{oss\ eq}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

**Table 7. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 325\text{ V}, I_D = 2.5\text{ A}, R_G = 4.7\text{ }\Omega, V_{GS} = 10\text{ V}$ (see <a href="#">Figure 18</a> and <a href="#">Figure 23</a> )	-	7.5	-	ns
$t_r$	Rise time		-	6.6	-	ns
$t_{d(off)}$	Turn-off delay time		-	22.5	-	ns
$t_f$	Fall time		-	18	-	ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		5	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		20	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0, I_{SD} = 5 \text{ A}$	-		1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 5 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 60 \text{ V}$ (see <a href="#">Figure 20</a> )	-	276		ns
$Q_{rr}$	Reverse recovery charge		-	1.7		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	12.5		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 5 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 60 \text{ V}, T_j = 150 \text{ }^\circ\text{C}$ (see <a href="#">Figure 20</a> )	-	312		ns
$Q_{rr}$	Reverse recovery charge		-	1.9		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	12.4		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for DPAK and IPAK

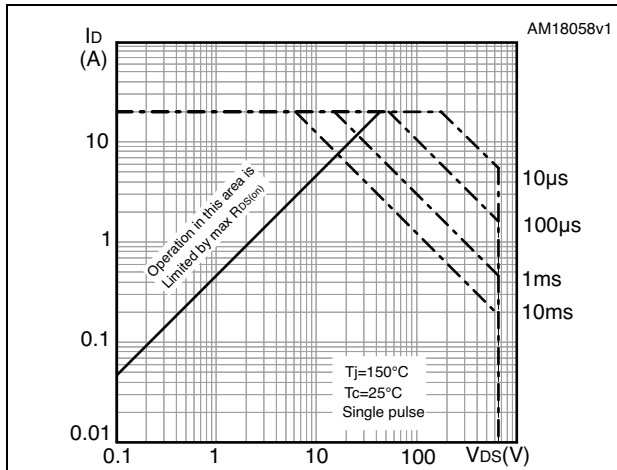


Figure 3. Thermal impedance for DPAK and IPAK

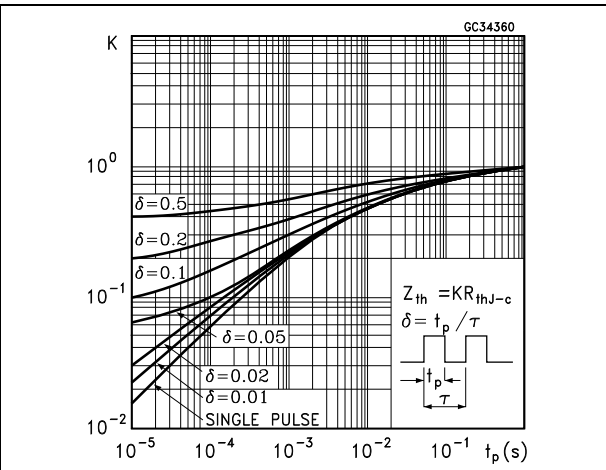


Figure 4. Safe operating area for TO-220FP

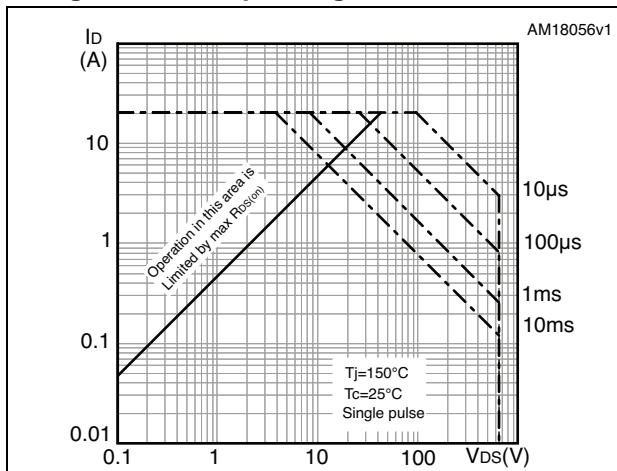


Figure 5. Thermal impedance for TO-220FP

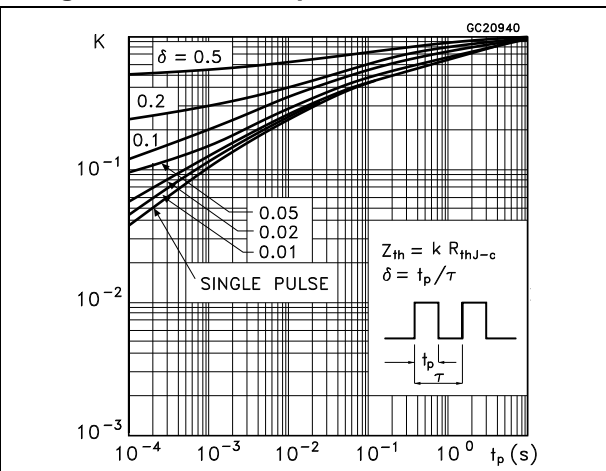


Figure 6. Safe operating area for TO-220

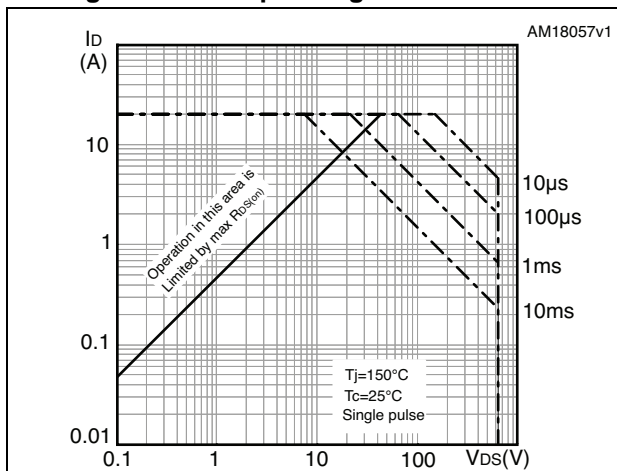


Figure 7. Thermal impedance for TO-220

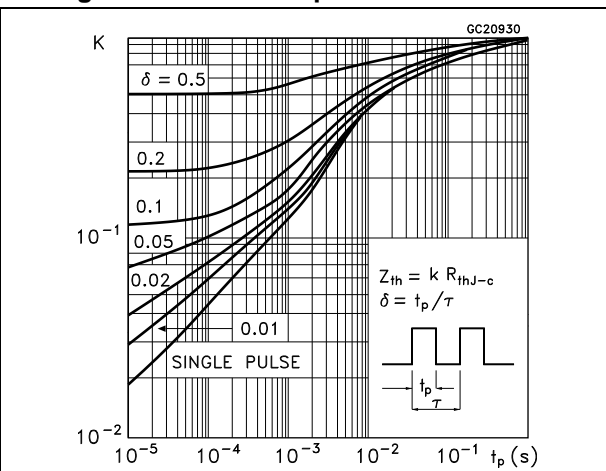


Figure 8. Output characteristics

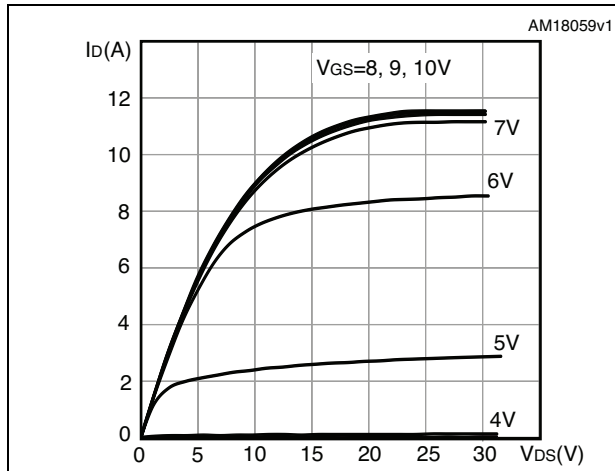


Figure 9. Transfer characteristics

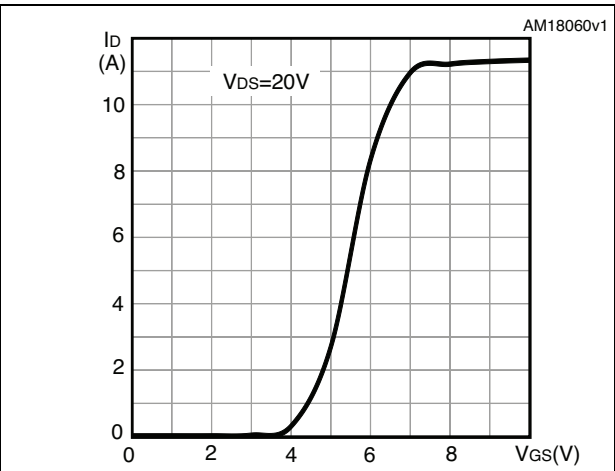


Figure 10. Gate charge vs gate-source voltage

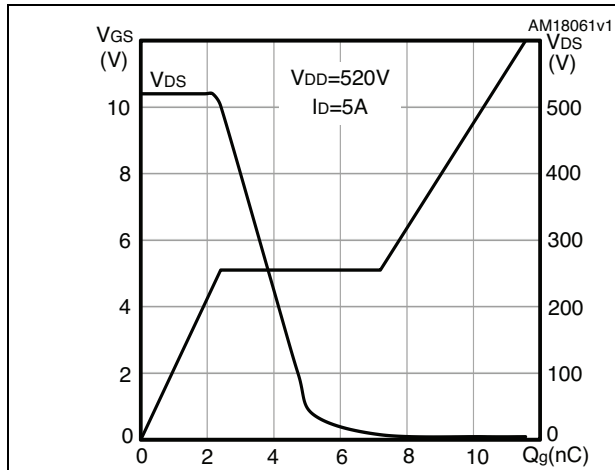


Figure 11. Static drain-source on-resistance

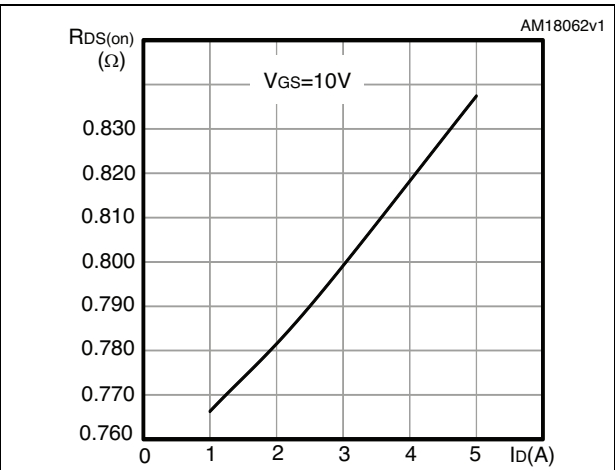


Figure 12. Capacitance variations

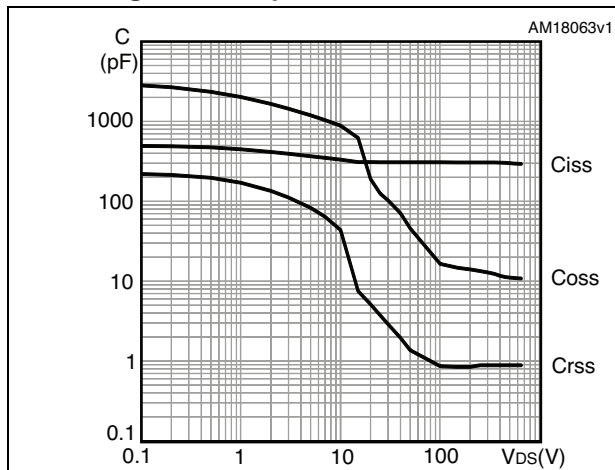


Figure 13. Output capacitance stored energy

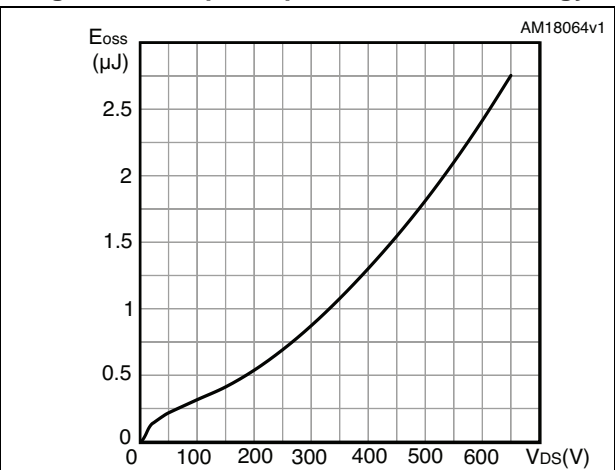


Figure 14. Normalized gate threshold voltage vs temperature

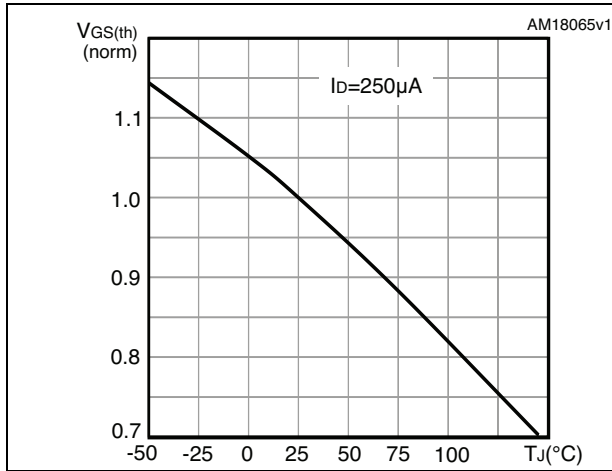


Figure 15. Normalized on-resistance vs temperature

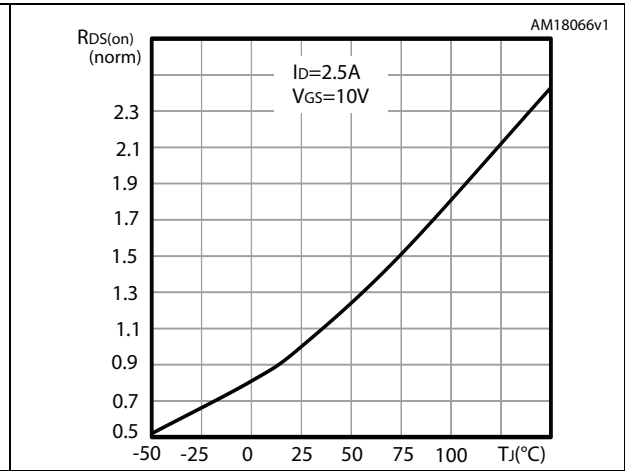


Figure 16. Source-drain diode forward characteristics

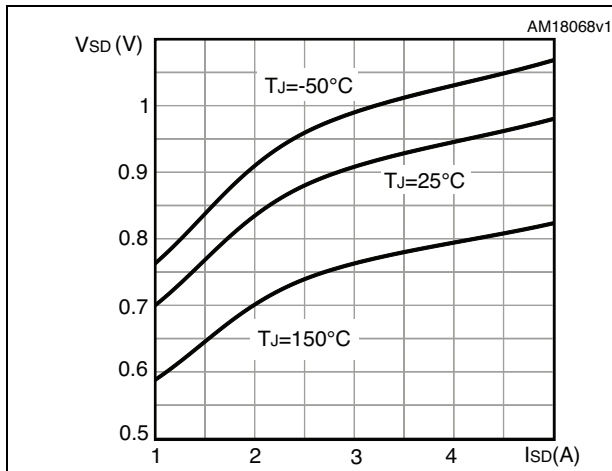
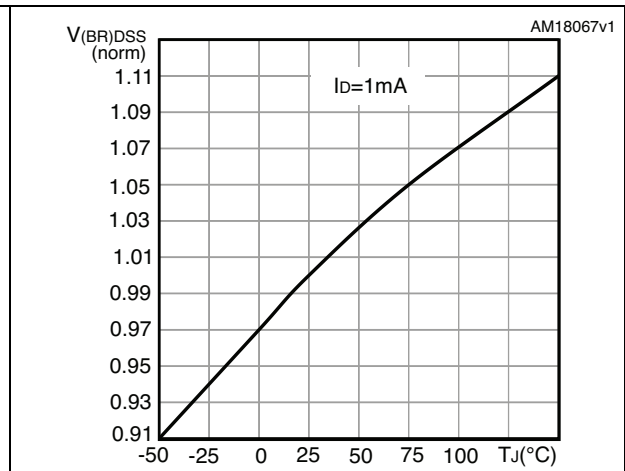


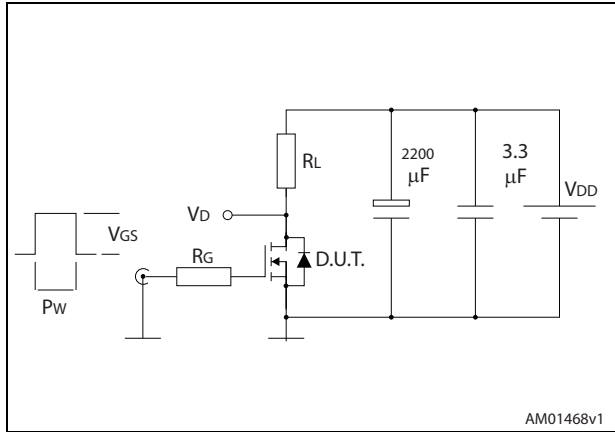
Figure 17. Normalized V<sub>(BR)DSS</sub> vs temperature





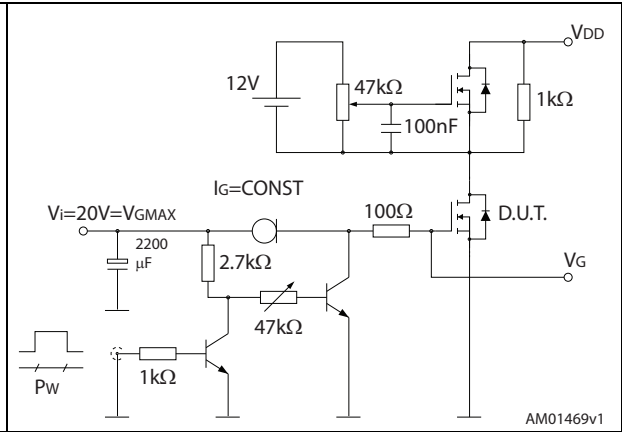
### 3 Test circuits

Figure 18. Switching times test circuit for resistive load



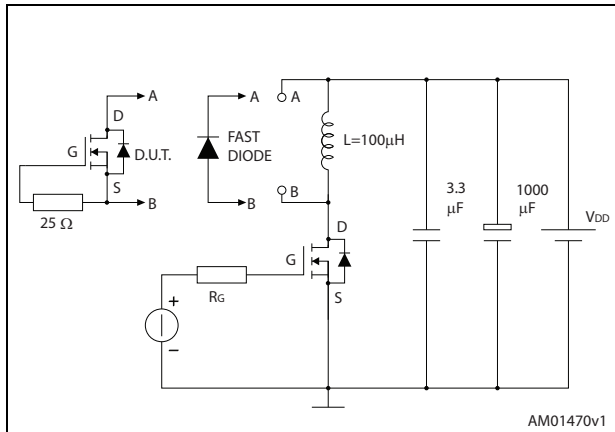
AM01468v1

Figure 19. Gate charge test circuit



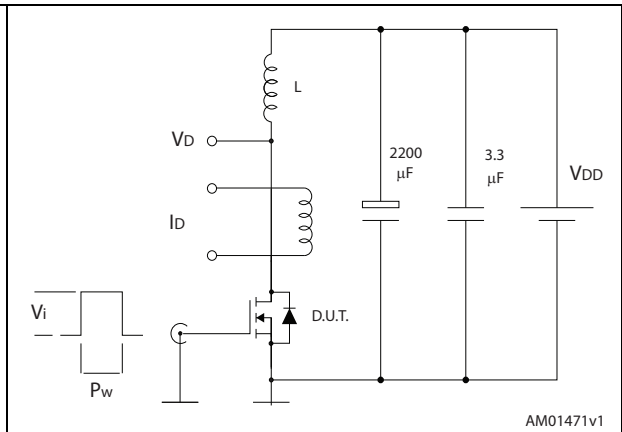
AM01469v1

Figure 20. Test circuit for inductive load switching and diode recovery times



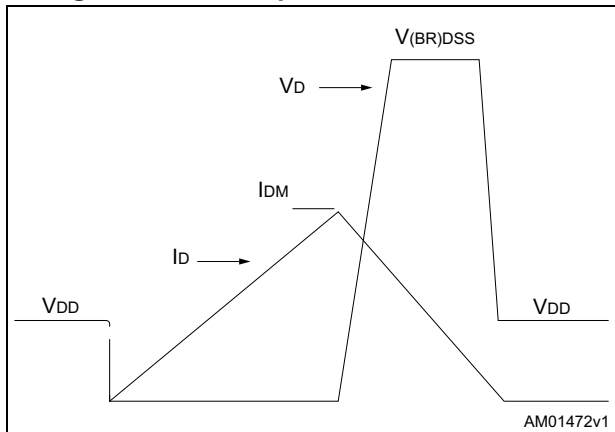
AM01470v1

Figure 21. Unclamped inductive load test circuit



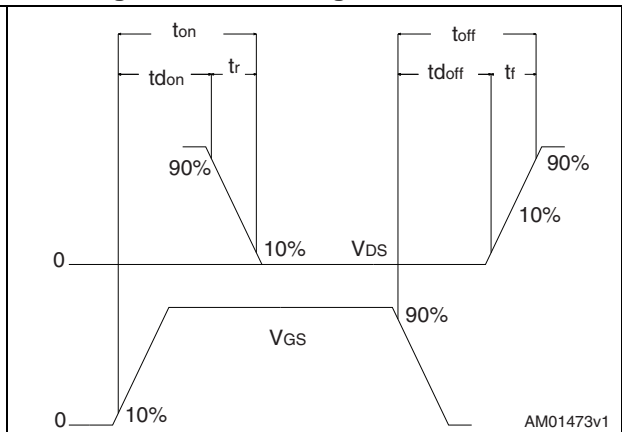
AM01471v1

Figure 22. Unclamped inductive waveform



AM01472v1

Figure 23. Switching time waveform



AM01473v1

## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

4.1 DPAK, STD9N65M2

Figure 24. DPAK (TO-252) type A drawing

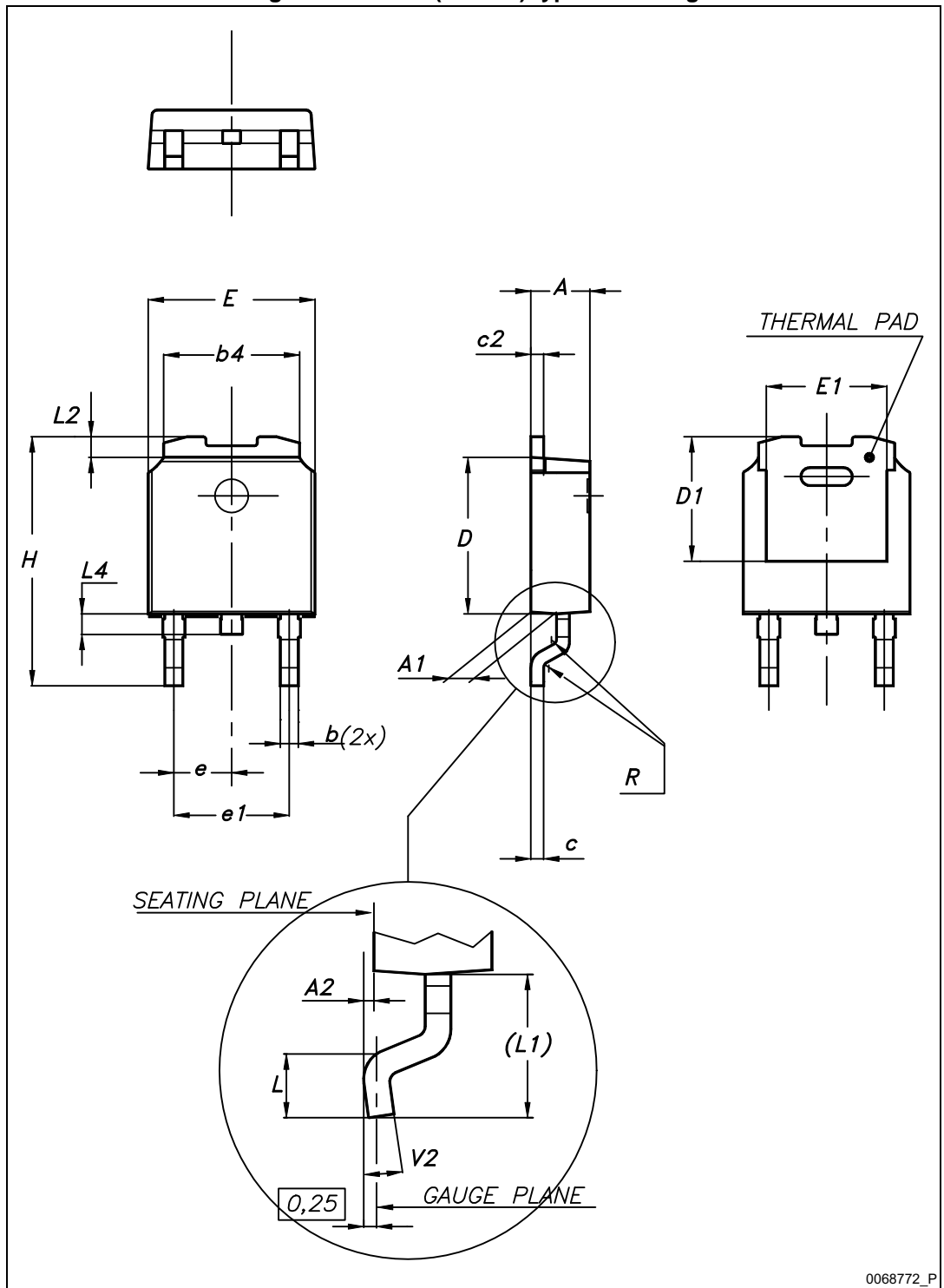
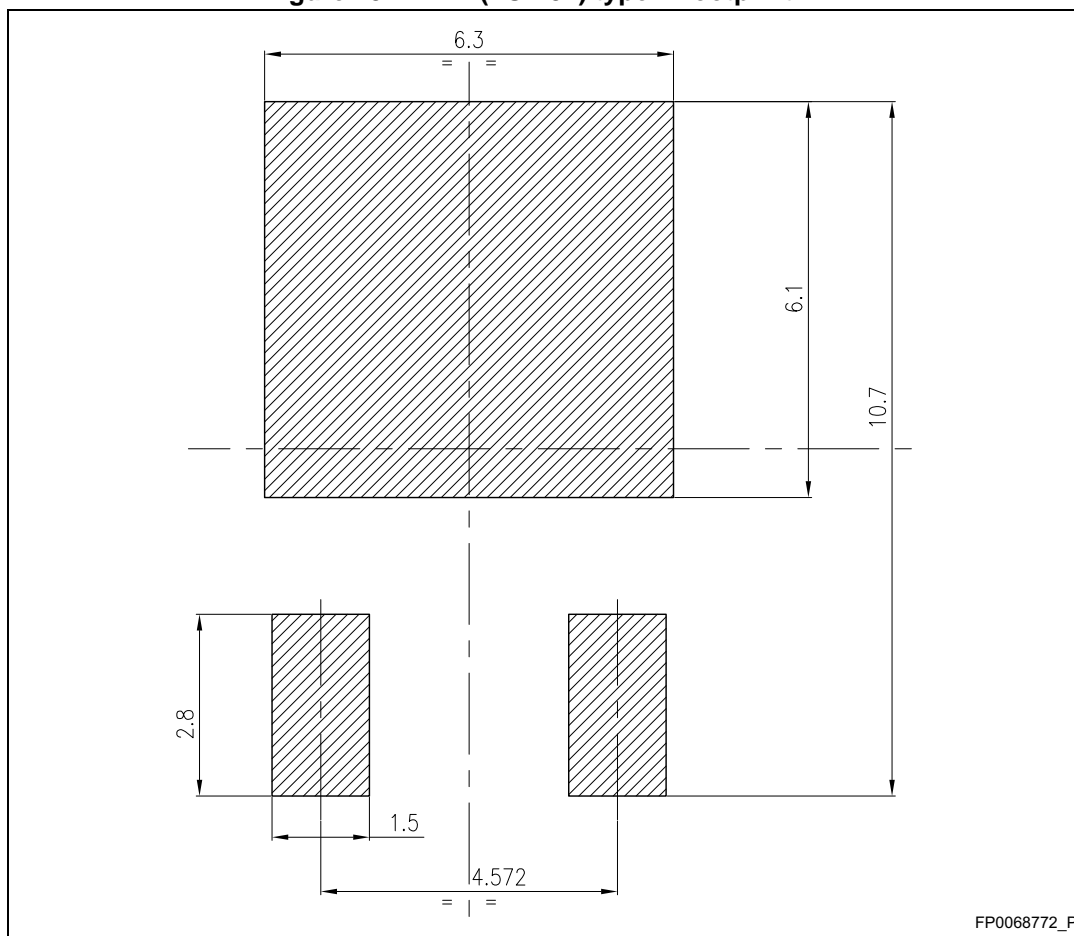


Table 9. DPAK (TO-252) type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1.00		1.50
L1		2.80	
L2		0.80	
L4	0.60		1.00
R		0.20	
V2	0°		8°

Figure 25. DPAK (TO-252) type A footprint (a)



a. All dimensions are in millimeters

4.2 TO-220FP, STF9N65M2

Figure 26. TO-220FP drawing

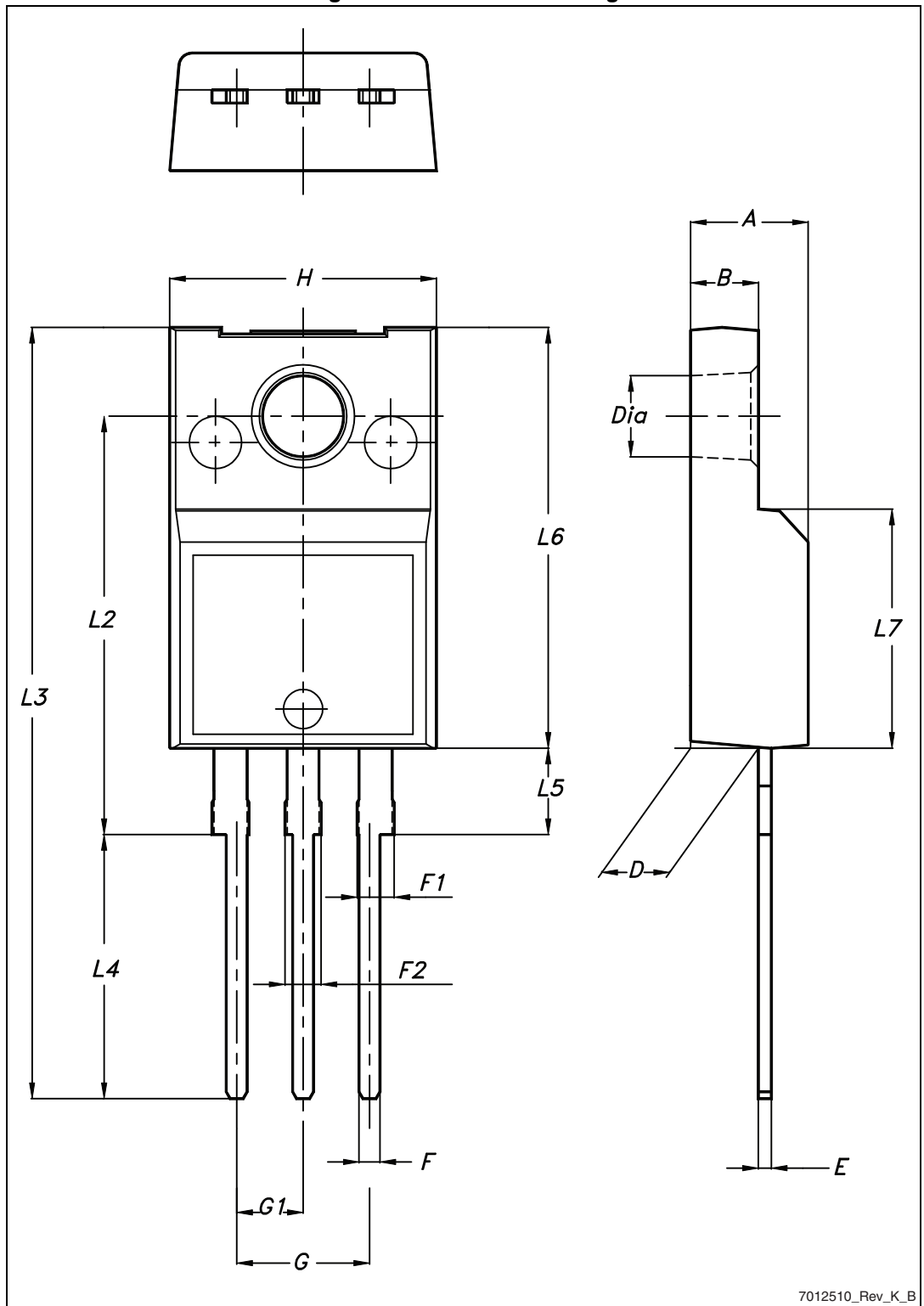


Table 10. TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Ø	3		3.2

### 4.3 TO-220, STP9N65M2

Figure 27. TO-220 type A drawing

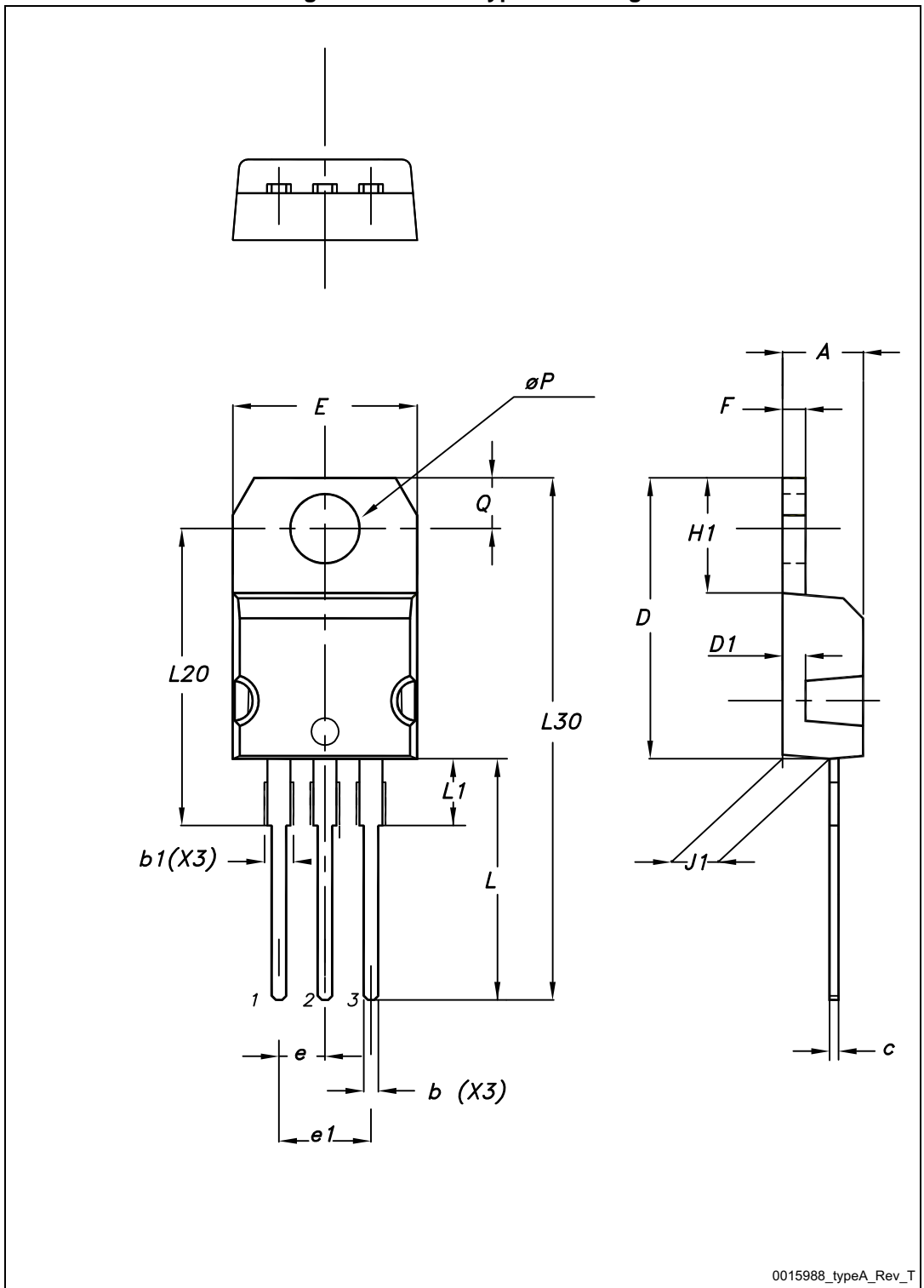




Table 11. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
ØP	3.75		3.85
Q	2.65		2.95

### 4.4 IPAK, STU9N65M2

Figure 28. IPAK (TO-251) drawing

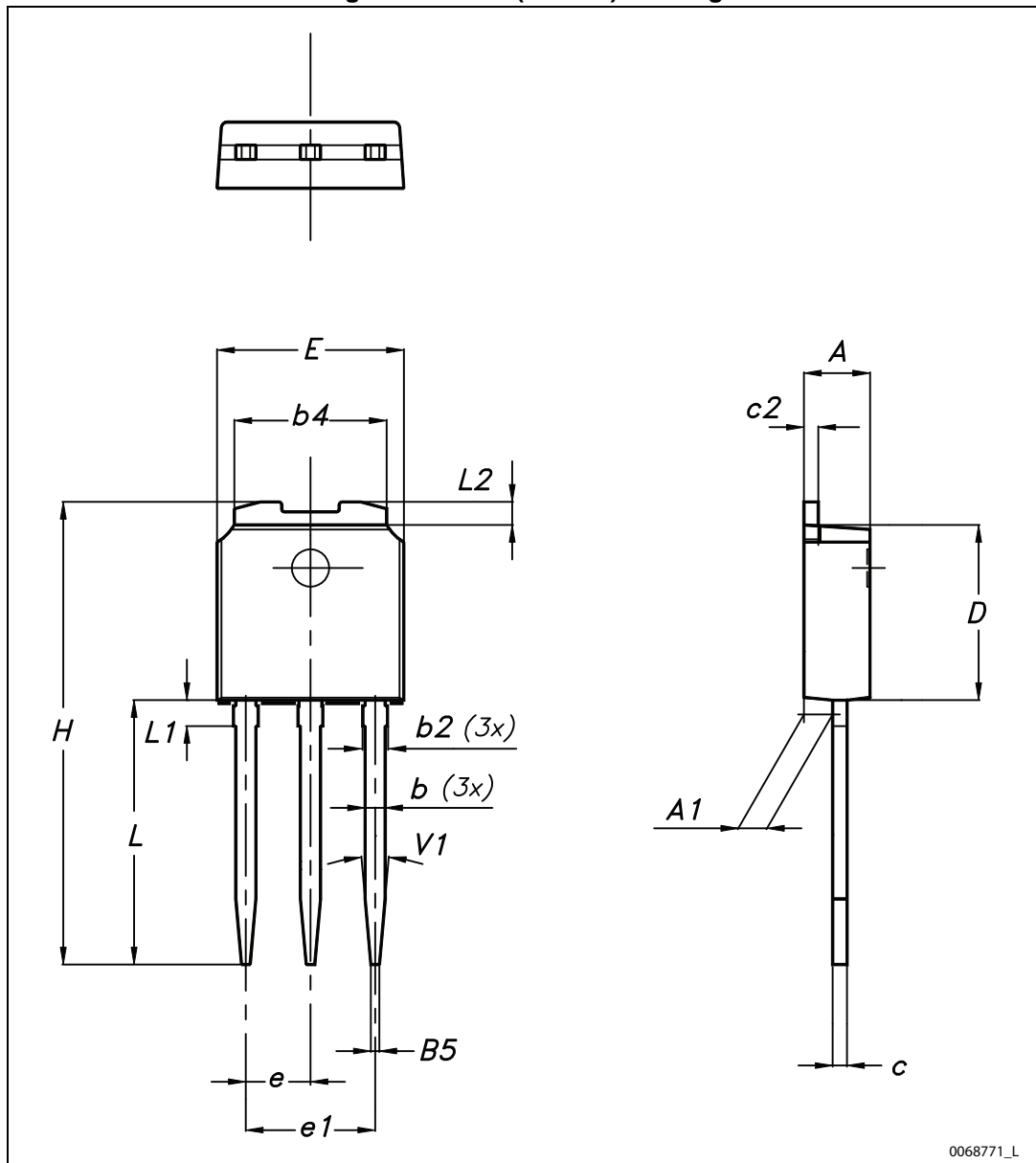


Table 12. IPAK (TO-251) mechanical data

DIM	mm.		
	min.	typ.	max.
A	2.20		2.40
A1	0.90		1.10
b	0.64		0.90
b2			0.95
b4	5.20		5.40
B5		0.30	
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
E	6.40		6.60
e		2.28	
e1	4.40		4.60
H		16.10	
L	9.00		9.40
L1	0.80		1.20
L2		0.80	1.00
V1		10°	

# 5 Packaging mechanical data

Figure 29. Tape for DPAK (TO-252)

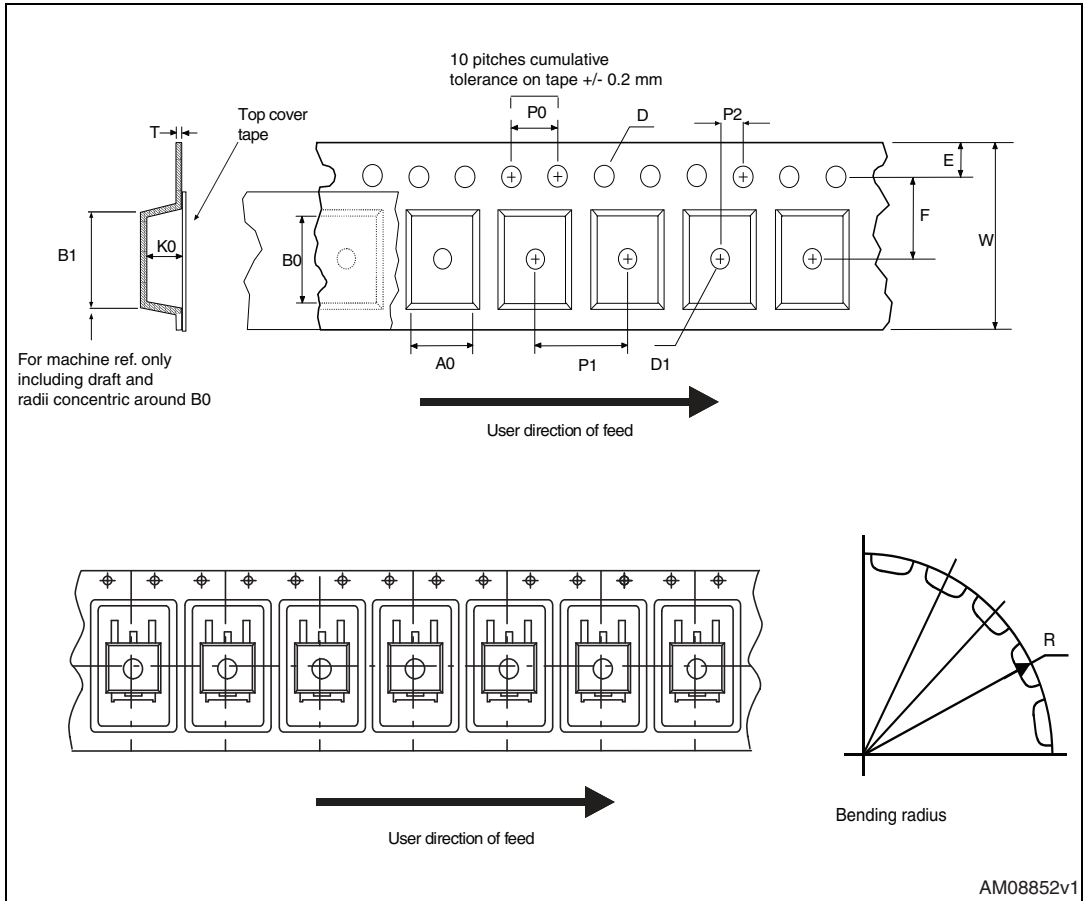


Figure 30. Reel for DPAK (TO-252)

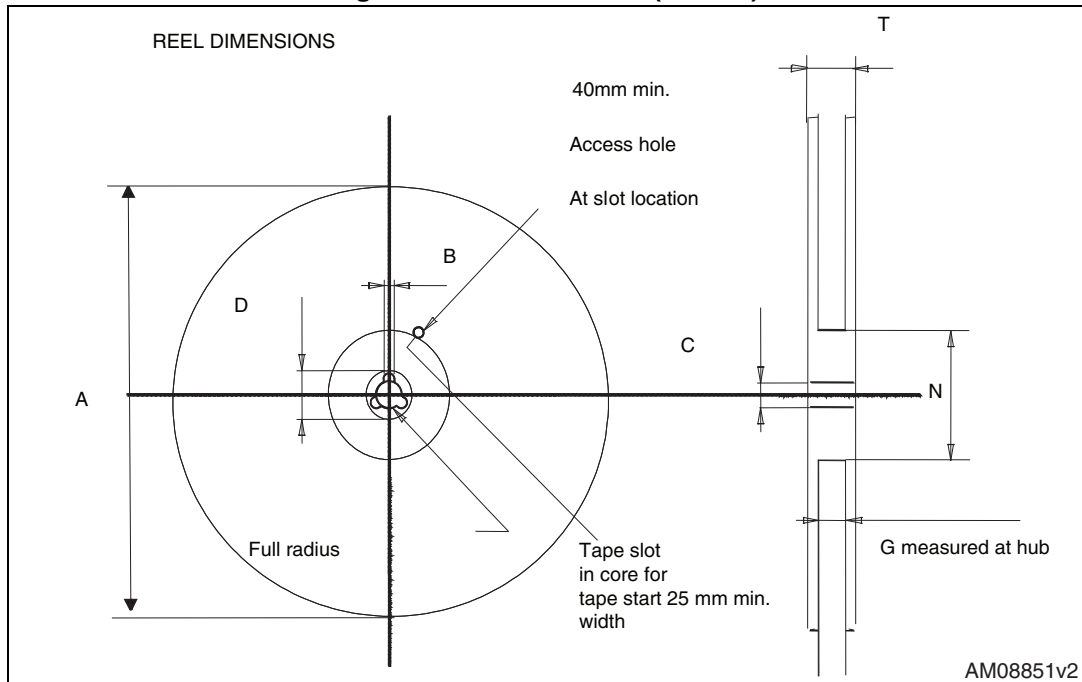


Table 13. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1		Base qty.	2500
P1	7.9	8.1		Bulk qty.	2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

## 6 Revision history

Table 14. Document revision history

Date	Revision	Changes
24-Feb-2014	1	First release.
15-Jul-2014	2	<ul style="list-style-type: none"><li>– Modified: title, <i>Features</i> and <i>Description</i></li><li>– Modified: <i>Figure 5</i> and <i>15</i></li><li>– Updated: <i>Figure 28</i> and <i>Table 12</i></li><li>– Minor text changes</li></ul>

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