

N-channel 1050 V, 2.9 Ω typ., 3 A MDmesh™ K5 Power MOSFET in a TO-220FP package

Datasheet - production data

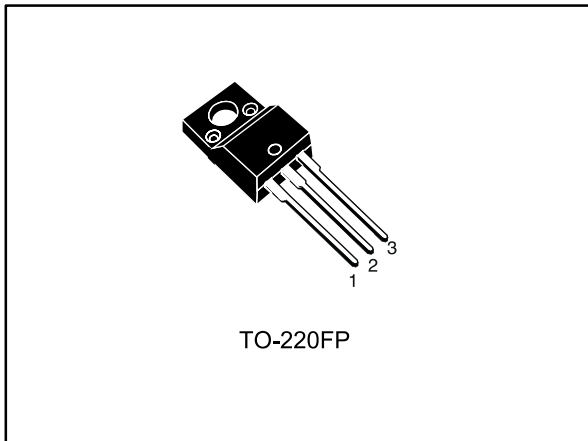
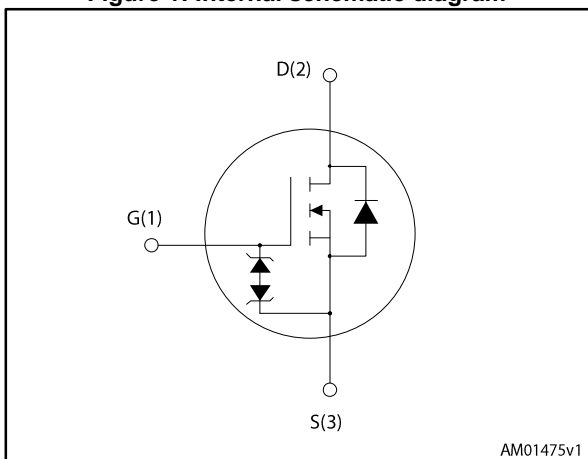


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D	P _{TOT}
STF5N105K5	1050 V	3.5 Ω	3 A	25 W

- Worldwide best FOM (figure of merit)
- Ultra low gate charge
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

This N-channel Zener-protected Power MOSFET is designed using ST's revolutionary avalanche-rugged very high voltage MDmesh™ K5 technology, based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance, and ultra-low gate charge for applications which require superior power density and high efficiency.

Table 1: Device summary

Part number	Marking	Package	Packaging
STF5N105K5	5N105K5	TO-220FP	Tube

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate- source voltage	± 30	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	3 ⁽¹⁾	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	2 ⁽¹⁾	A
I_{DM} ⁽²⁾	Drain current (pulsed)	12	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	25	W
I_{AR}	Max current during repetitive or single pulse avalanche	1	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$, $I_D = I_{AS}$, $V_{DD} = 50\text{ V}$)	85	mJ
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink ($t = 1\text{ s}$; $T_C = 25\text{ }^\circ\text{C}$)	2500	V
dv/dt ⁽³⁾	Peak diode recovery voltage slope	4.5	V/ns
dv/dt ⁽⁴⁾	MOSFET dv/dt ruggedness	50	V/ns
T_j	Operating junction temperature	- 55 to 150	$^\circ\text{C}$
T_{stg}	Storage temperature		

Notes:

⁽¹⁾Limited only by maximum junction temperature

⁽²⁾Pulse width limited by safe operating area.

⁽³⁾ $I_{SD} \leq 3\text{ A}$, $di/dt \leq 100\text{ A}/\mu\text{s}$, $V_{DS(peak)} \leq V_{(BR)DSS}$

⁽⁴⁾ $V_{DS} \leq 840\text{ V}$

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	5	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-amb max	62.5	$^\circ\text{C}/\text{W}$

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified).

Table 4: On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	V _{GS} = 0, I _D = 1 mA	1050			V
I _{DSS}	Zero gate voltage drain current	V _{GS} = 0, V _{DS} = 1050 V			1	μA
		V _{GS} = 0, V _{DS} = 1050 V, T _C = 125 °C			50	μA
I _{GSS}	Gate body leakage current	V _{DS} = 0, V _{GS} = ± 20 V			±10	μA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 100 μA	3	4	5	V
R _{DS(on)}	Static drain-source on-resistance	V _{GS} = 10 V, I _D = 1.5 A		2.9	3.5	Ω

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iSS}	Input capacitance	V _{GS} = 0, V _{DS} = 100 V, f = 1 MHz	-	210	-	pF
C _{oSS}	Output capacitance		-	16	-	pF
C _{rSS}	Reverse transfer capacitance		-	0.5	-	pF
C _{o(tr)} ⁽¹⁾	Equivalent capacitance time related	V _{GS} = 0, V _{DS} = 0 to 840 V	-	26	-	pF
C _{o(er)} ⁽²⁾	Equivalent capacitance energy related		-	10	-	pF
R _G	Intrinsic gate resistance	f = 1MHz open drain	-	9	-	Ω
Q _g	Total gate charge	V _{DD} = 840 V, I _D = 3 A	-	12.5	-	nC
Q _{gs}	Gate-source charge	V _{GS} = 10 V	-	2	-	nC
Q _{gd}	Gate-drain charge	<i>Figure 16: "Gate charge test circuit"</i>	-	9.5	-	nC

Notes:

⁽¹⁾Time related is defined as a constant equivalent capacitance giving the same charging time as C_{oSS} when V_{DS} increases from 0 to 80% V_{DSS}

⁽²⁾energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oSS} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{d(on)}	Turn-on delay time	V _{DD} = 525V, I _D = 1.5 A, R _G = 4.7 Ω, V _{GS} = 10 V <i>Figure 18: "Unclamped inductive load test circuit"</i>	-	15.5	-	ns
t _r	Rise time		-	8.5	-	ns
t _{d(off)}	Turn-off delay time		-	31	-	ns
t _f	Fall time		-	24	-	ns

Table 7: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		3	A
I_{SDM}	Source-drain current (pulsed)		-		12	A
$V_{SD}^{(1)}$	Forward on voltage	$V_{GS}=0, I_{SD}=3\text{ A}$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD}=3\text{ A}, V_{DD}=60\text{ V}$ $di/dt=100\text{ A}/\mu\text{s}$, <i>Figure 17: " Test circuit for inductive load switching and diode recovery times"</i>	-	400		ns
Q_{rr}	Reverse recovery charge		-	2.3		μC
I_{RRM}	Reverse recovery current		-	12		A
t_{rr}	Reverse recovery time	$I_{SD}=3\text{ A}, V_{DD}=60\text{ V}$ $di/dt=100\text{ A}/\mu\text{s}$, $T_j=150\text{ }^\circ\text{C}$ <i>Figure 17: " Test circuit for inductive load switching and diode recovery times"</i>	-	560		ns
Q_{rr}	Reverse recovery charge		-	3.1		μC
I_{RRM}	Reverse recovery current		-	11		A

Notes:

⁽¹⁾Pulsed: pulse duration = 300 μs , duty cycle 1.5%

Table 8: Gate-source Zener diode

Symbol	Parameter	Test conditions	Min	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1\text{ mA}, I_D=0$	30	-	-	V

The built-in back-to-back Zener diodes have specifically been designed to enhance the device's ESD capability. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

2.1 Electrical characteristics (curves)

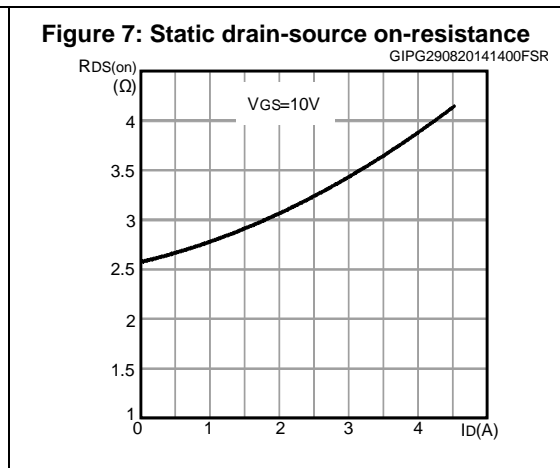
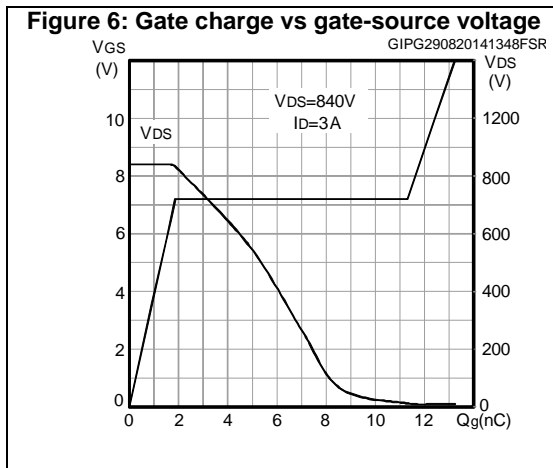
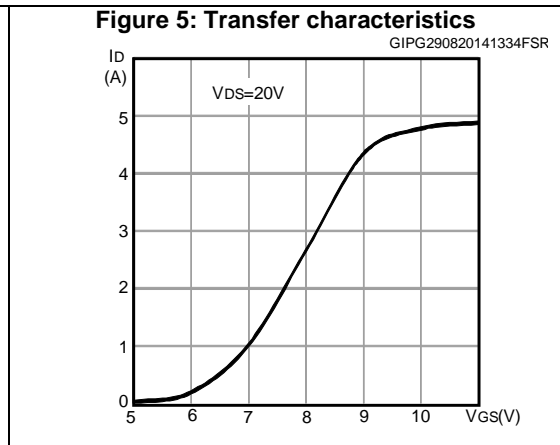
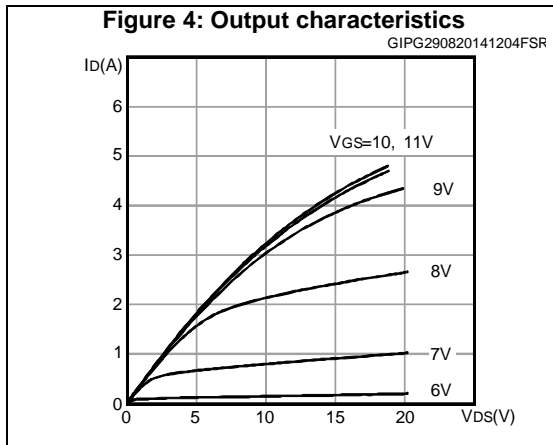
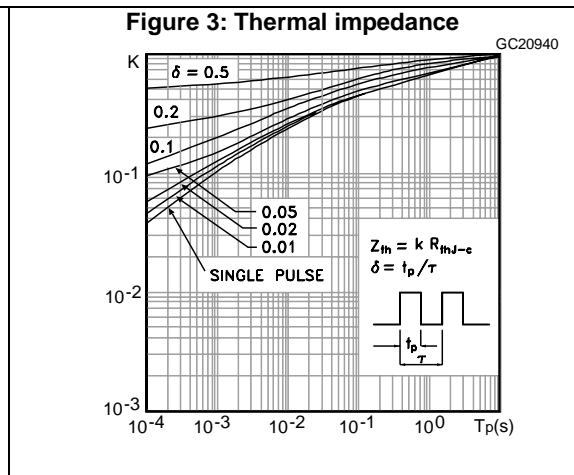
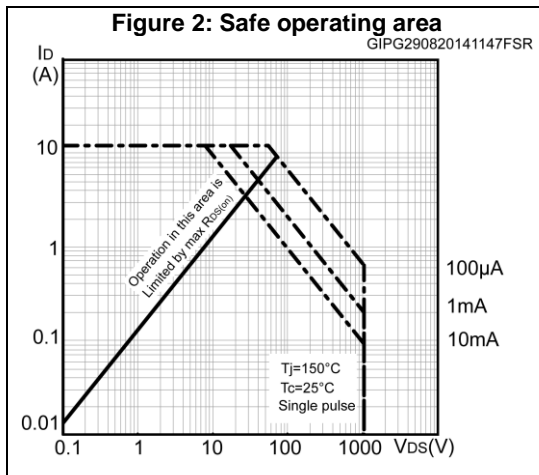


Figure 8: Capacitance variations

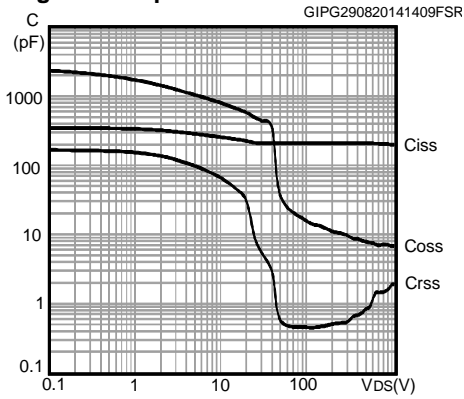


Figure 9: Maximum avalanche energy

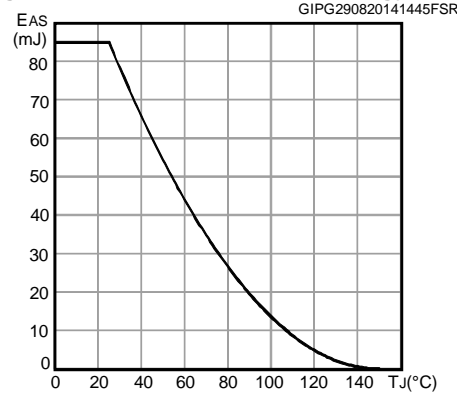


Figure 10: Normalized gate threshold voltage vs temperature

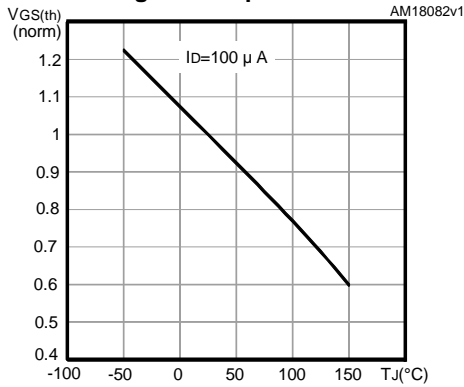


Figure 11: Normalized on-resistance vs temperature

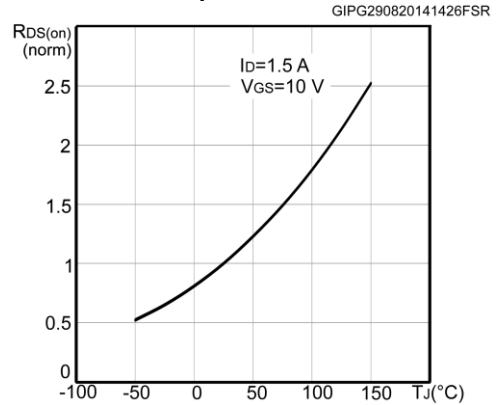


Figure 12: Normalized V(BR)DSS vs temperature

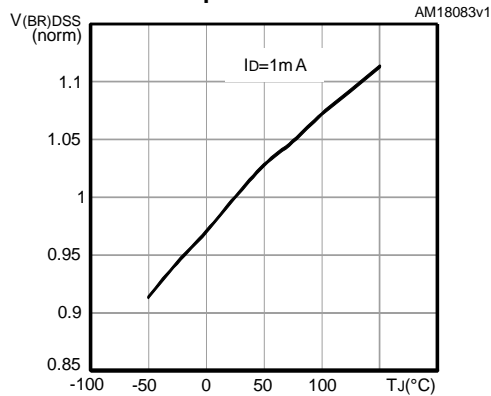


Figure 13: Source-drain diode forward characteristics

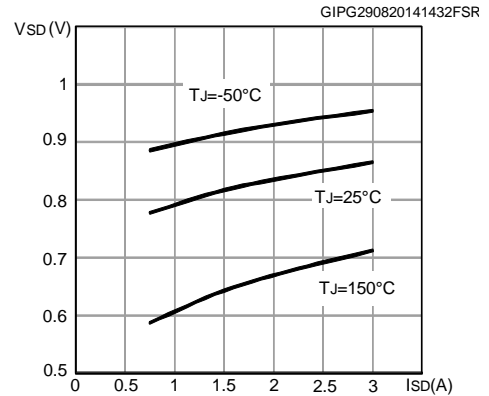
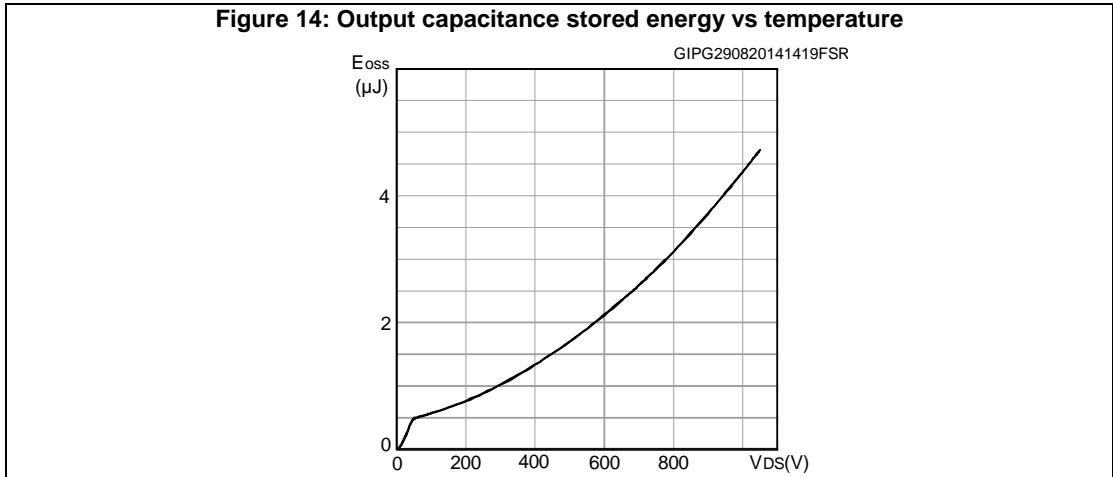
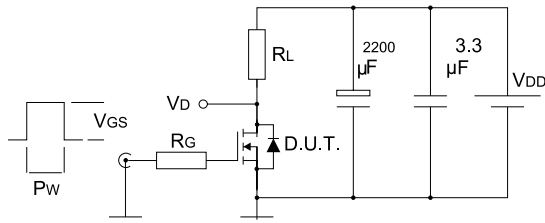


Figure 14: Output capacitance stored energy vs temperature



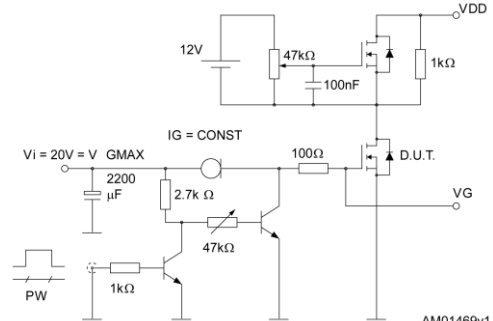
3 Test circuits

Figure 15: Switching times test circuit for resistive load



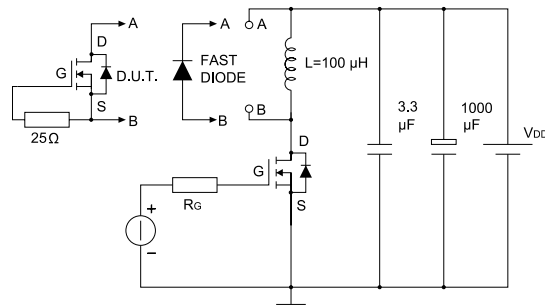
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Figure 16: Gate charge test circuit



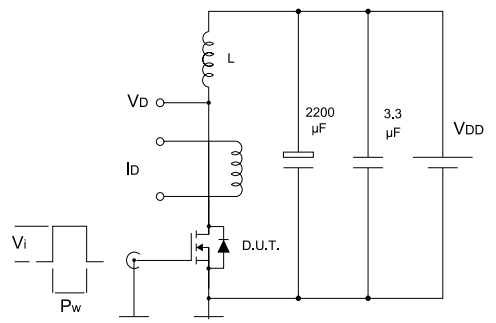
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Figure 17: Test circuit for inductive load switching and diode recovery times



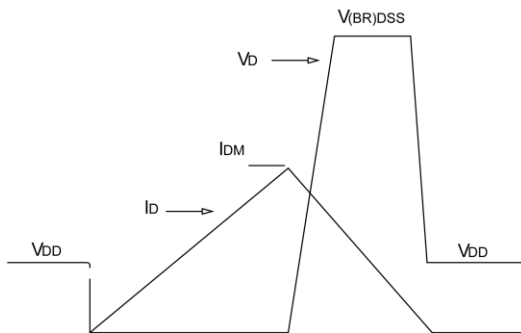
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Figure 18: Unclamped inductive load test circuit



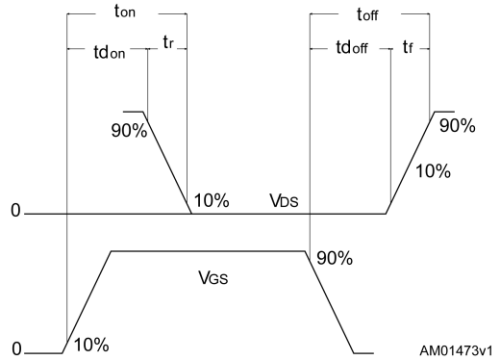
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Figure 19: Unclamped inductive waveform



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Figure 20: Switching time waveform



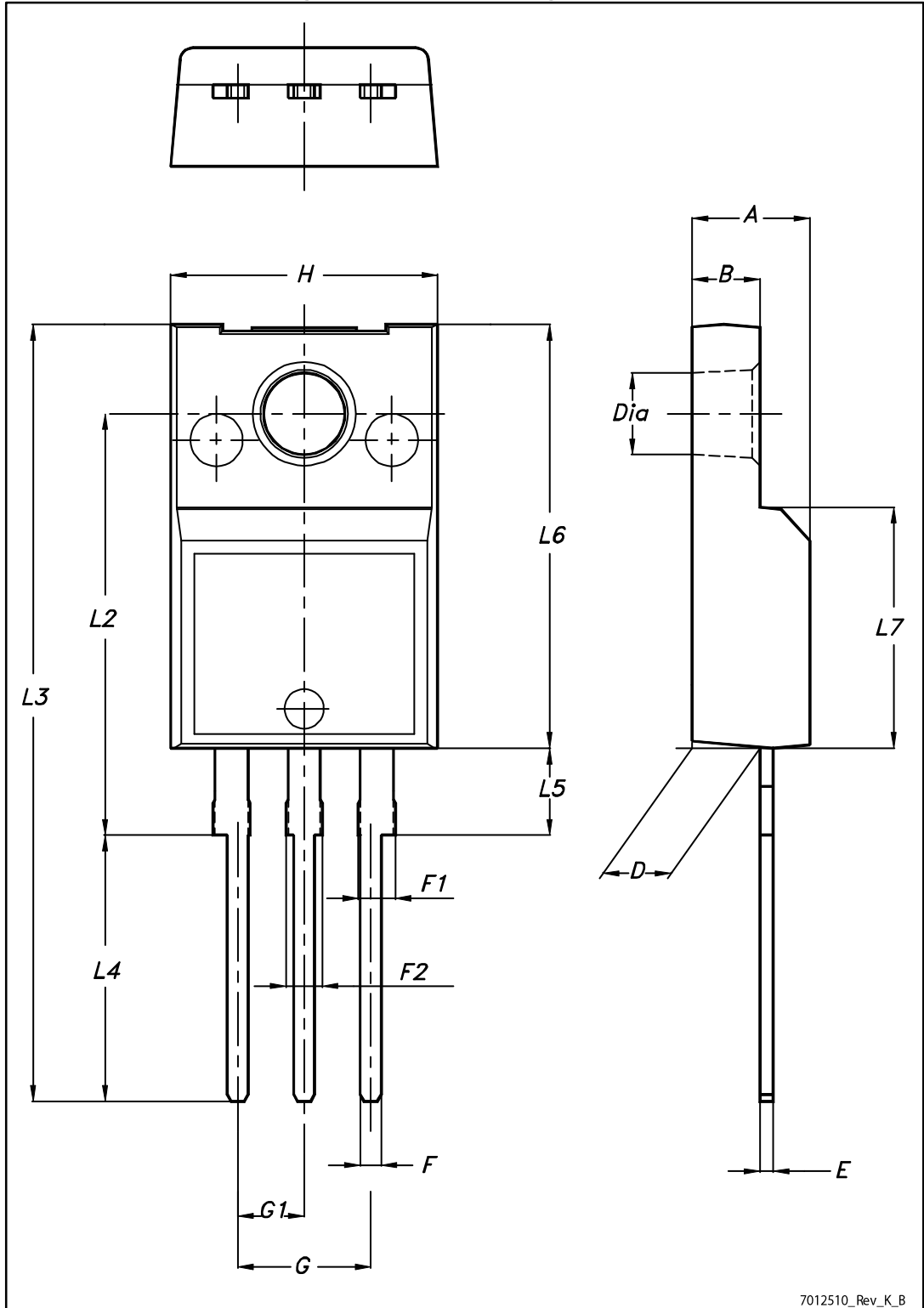
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4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 TO-220FP package mechanical data

Figure 21: TO-220FP package outline



7012510_Rev_K_B

Table 9: TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

5 Revision history

Table 10: Document revision history

Date	Revision	Changes
17-Jul-2014	1	First release.
01-Sep-2014	2	Document status promoted from preliminary to production data. Inserted Section 3.1: "Electrical characteristics (curves)" . Minor text changes.
02-Sep-2014	3	Updated title in cover page.
03-Oct-2014	4	Updated: Figure 3: "Thermal impedance" , Figure 6: "Gate charge vs gate-source voltage" and Figure 8: "Capacitance variations"
15-Oct-2014	5	Updated Table 2: "Absolute maximum ratings"

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