

Automotive-grade N-channel 80 V, 0.0017  $\Omega$  typ., 180 A, STripFET™ F7 Power MOSFETs in H<sup>2</sup>PAK-2 and H<sup>2</sup>PAK-6

Datasheet – production data

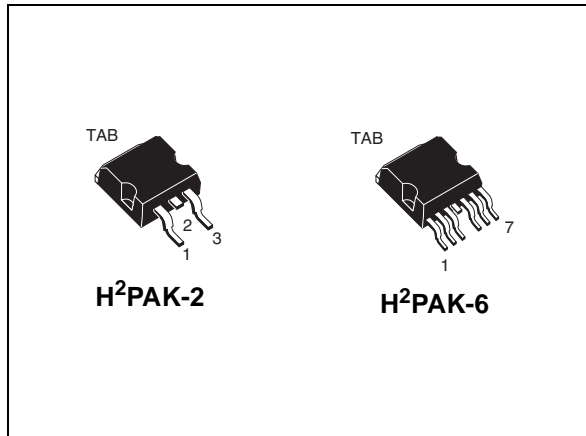
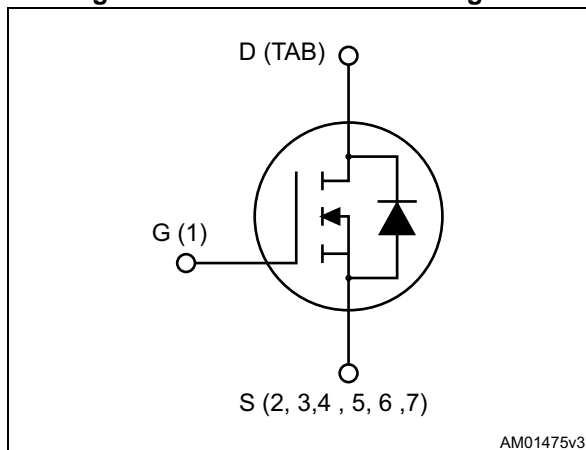


Figure 1. Internal schematic diagram



## Features

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max	I <sub>D</sub>
STH275N8F7-2AG	80 V	0.0021 $\Omega$	180 A
STH275N8F7-6AG			

- Designed for automotive applications and AEC-Q101 qualified
- Among the lowest R<sub>DS(on)</sub> on the market
- Excellent figure of merit (FoM)
- Low C<sub>rss</sub>/C<sub>iss</sub> ratio for EMI immunity
- High avalanche ruggedness

## Applications

- Switching applications

## Description

These N-channel Power MOSFETs utilize STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

Table 1. Device summary

Order code	Marking	Package	Packaging
STH275N8F7-2AG	275N8F7	H <sup>2</sup> PAK-2	Tape and reel
STH275N8F7-6AG		H <sup>2</sup> PAK-6	

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	80	V
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	180	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	180	A
$I_{DM}^{(2)}$	Drain current (pulsed)	720	A
$P_{TOT}^{(3)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	315	W
$E_{AS}^{(4)}$	Single pulse avalanche energy	1.16	J
$T_J$	Operating junction temperature range	-55 to 175	$^\circ\text{C}$
$T_{stg}$	Storage temperature range		$^\circ\text{C}$

1. Limited by package
2. Pulse width limited by safe operating area
3. This value is rated according to  $R_{thj-c}$
4. Starting  $T_j = 25\text{ }^\circ\text{C}$ ,  $I_d = 65\text{ A}$ ,  $V_{dd} = 50\text{ V}$

**Table 3. Thermal resistance**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	0.48	$^\circ\text{C/W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	35	$^\circ\text{C/W}$

1. When mounted on FR-4 board of 1 inch<sup>2</sup>, 2oz Cu

## 2 Electrical characteristics

( $T_{CASE}=25\text{ °C}$  unless otherwise specified)

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS}=0\text{ V}$ , $I_D = 1\text{ mA}$	80			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS}=0\text{ V}$ , $V_{DS}=80\text{ V}$			1	$\mu\text{A}$
		$V_{GS}=0\text{ V}$ , $V_{DS}=80\text{ V}$ , $T_C=125\text{ °C}$ <sup>(1)</sup>			100	$\mu\text{A}$
$I_{GSS}$	Gate body leakage current	$V_{DS}=0\text{ V}$ , $V_{GS}=+20\text{ V}$			100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS}=V_{GS}$ , $I_D=250\text{ }\mu\text{A}$	2.5		4.5	V
$R_{DS(on)}$	Static drain-source on- resistance	$V_{GS}=10\text{ V}$ , $I_D=90\text{ A}$		0.0017	0.0021	$\Omega$

1. Defined by design, not subject to production test.

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{GS}=0\text{ V}$ , $V_{DS}=50\text{ V}$ , $f=1\text{ MHz}$	-	13600	-	pF
$C_{oss}$	Output capacitance		-	2050	-	pF
$C_{riss}$	Reverse transfer capacitance		-	236	-	pF
$Q_g$	Total gate charge	$V_{DD}=40\text{ V}$ , $I_D=180\text{ A}$	-	193	-	nC
$Q_{gs}$	Gate-source charge	$V_{GS}=10\text{ V}$	-	96	-	nC
$Q_{gd}$	Gate-drain charge	<a href="#">Figure 14</a>	-	46	-	nC

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD}=40\text{ V}$ , $I_D=90\text{ A}$ , $R_G=4.7\text{ }\Omega$ , $V_{GS}=10\text{ V}$ <a href="#">Figure 13</a>	-	56	-	ns
$t_r$	Rise time		-	180	-	ns
$t_{d(off)}$	Turn-off delay time		-	98	-	ns
$t_f$	Fall time		-	42	-	ns

**Table 7. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		180	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		720	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS}=0\text{ V}, I_{SD} = 90\text{ A}$	-		1.2	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 180\text{ A},$ $di/dt = 100\text{ A}/\mu\text{s},$ $V_{DD}=64\text{ V}, T_j=150\text{ }^\circ\text{C}$	-	78		ns
$Q_{rr}$	Reverse recovery charge		-	182		nC
$I_{RRM}$	Reverse recovery current		-	4.7		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300μs, duty cycle 1.5%

### 3 Electrical characteristics (curves)

Figure 2. Safe operating area

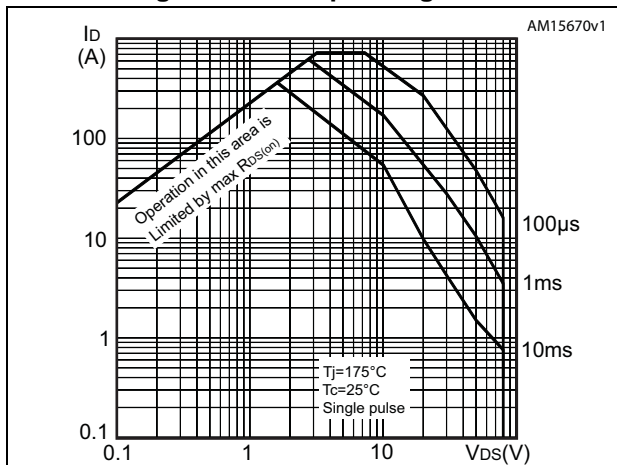


Figure 3. Thermal impedance

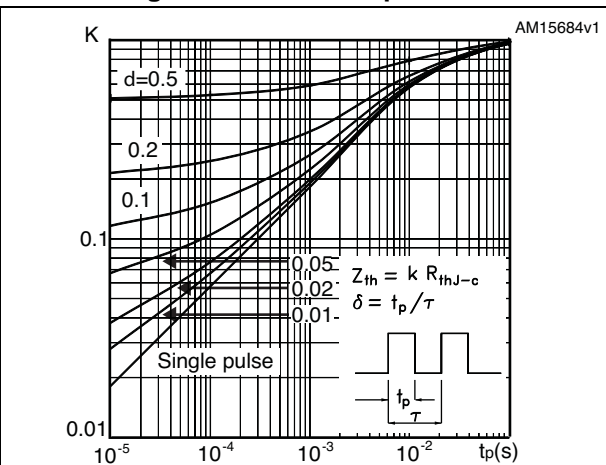


Figure 4. Gate charge vs gate-source voltage

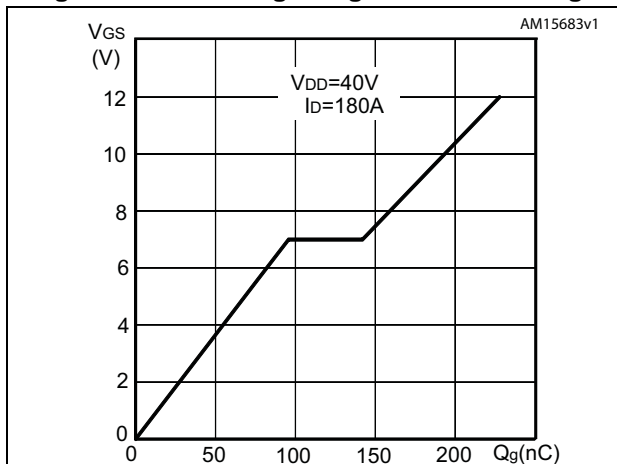


Figure 5. Output characteristics

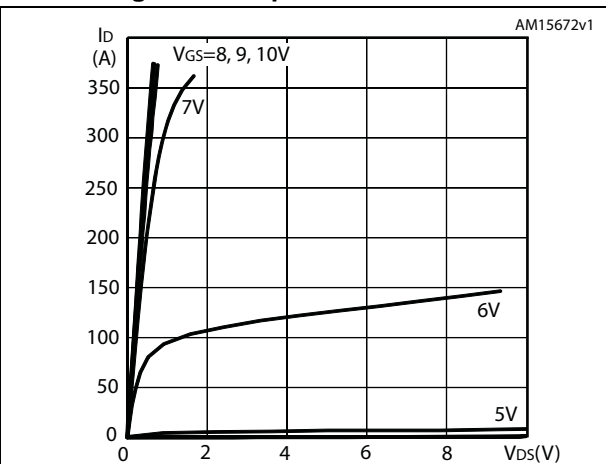


Figure 6. Transfer characteristics

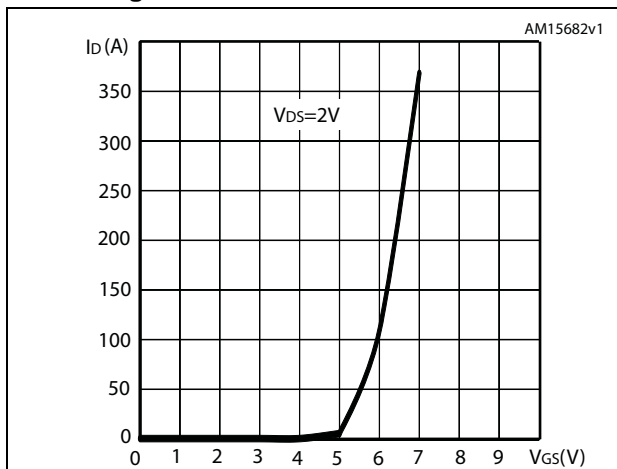


Figure 7. Normalized  $V_{(BR)DSS}$  vs temperature

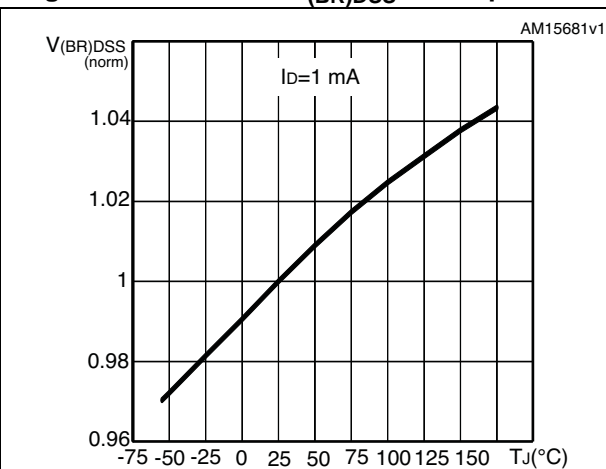


Figure 8. Static drain-source on-resistance

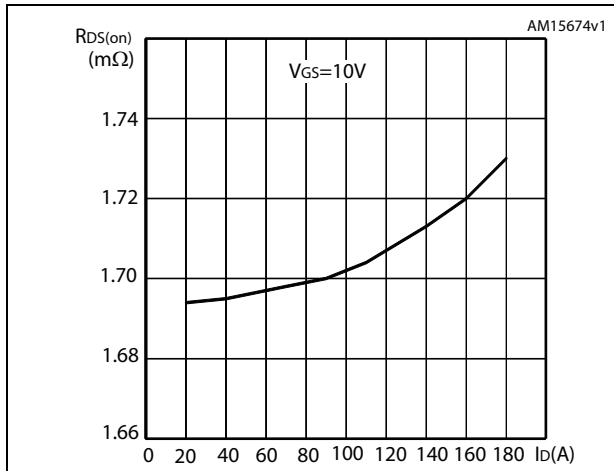


Figure 9. Capacitance variations

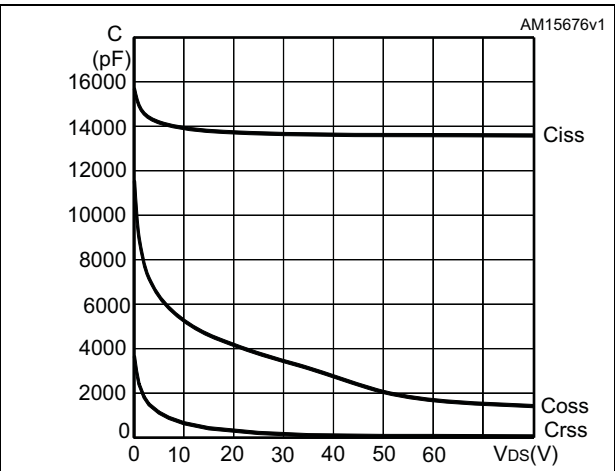


Figure 10. Source-drain diode forward characteristics

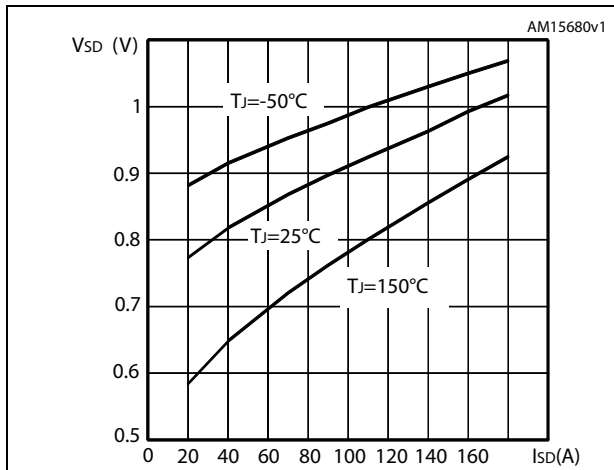


Figure 11. Normalized gate threshold voltage vs temperature

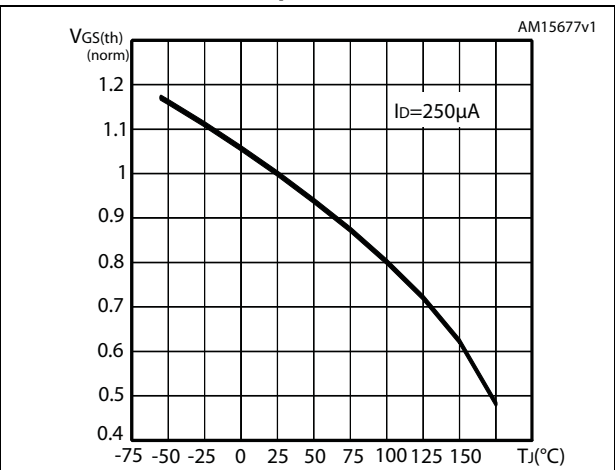
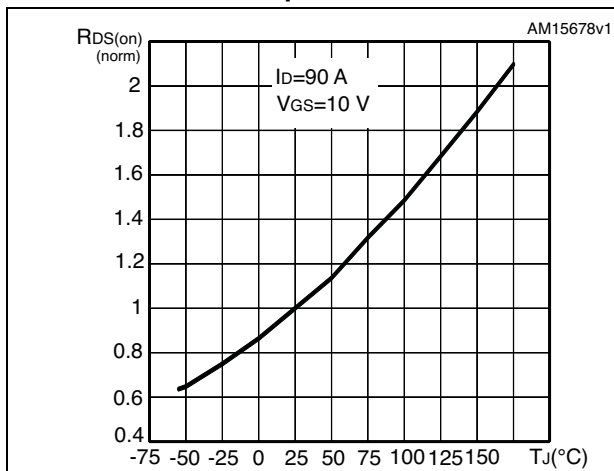


Figure 12. Normalized on-resistance vs temperature

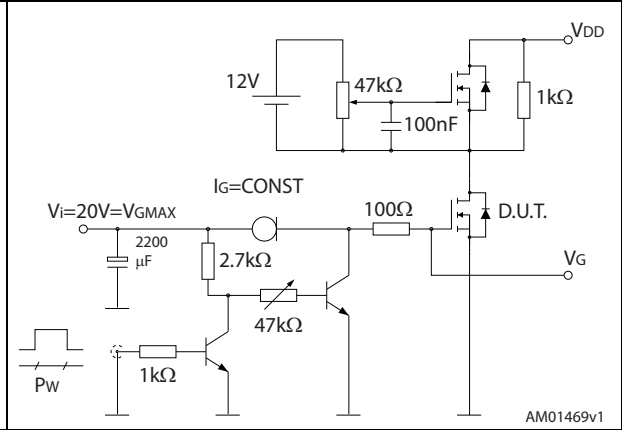


# 4 Test circuits

**Figure 13. Switching times test circuit for resistive load**



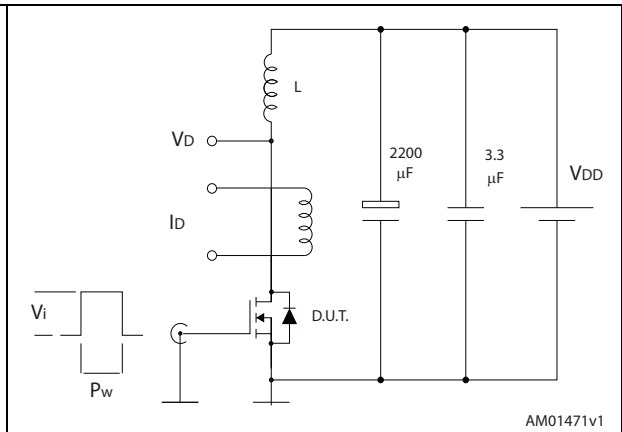
**Figure 14. Gate charge test circuit**



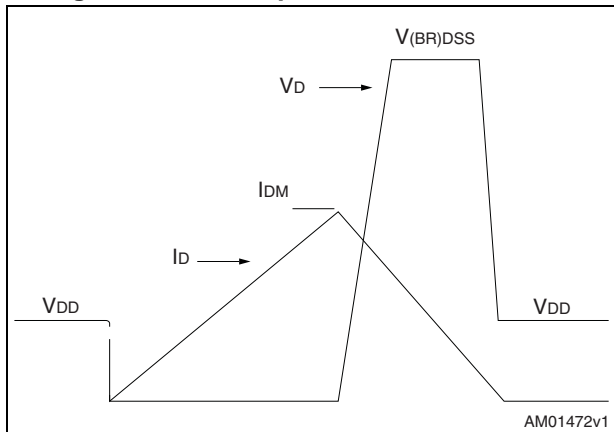
**Figure 15. Test circuit for inductive load switching and diode recovery times**



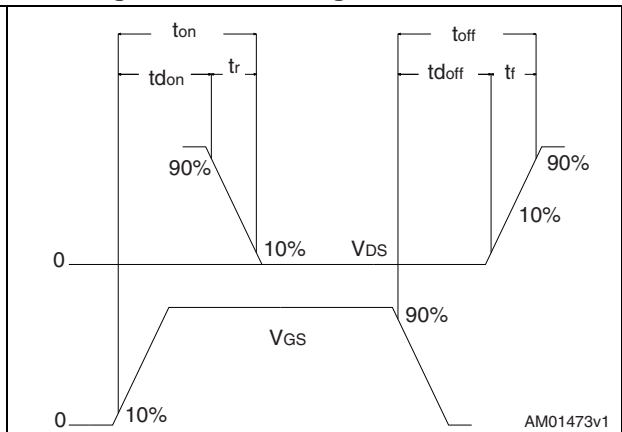
**Figure 16. Unclamped inductive load test circuit**



**Figure 17. Unclamped inductive waveform**



**Figure 18. Switching time waveform**





## 5 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

### 5.1 H<sup>2</sup>PAK-2, STH275N8F7-2AG

Figure 19. H<sup>2</sup>PAK-2 drawing

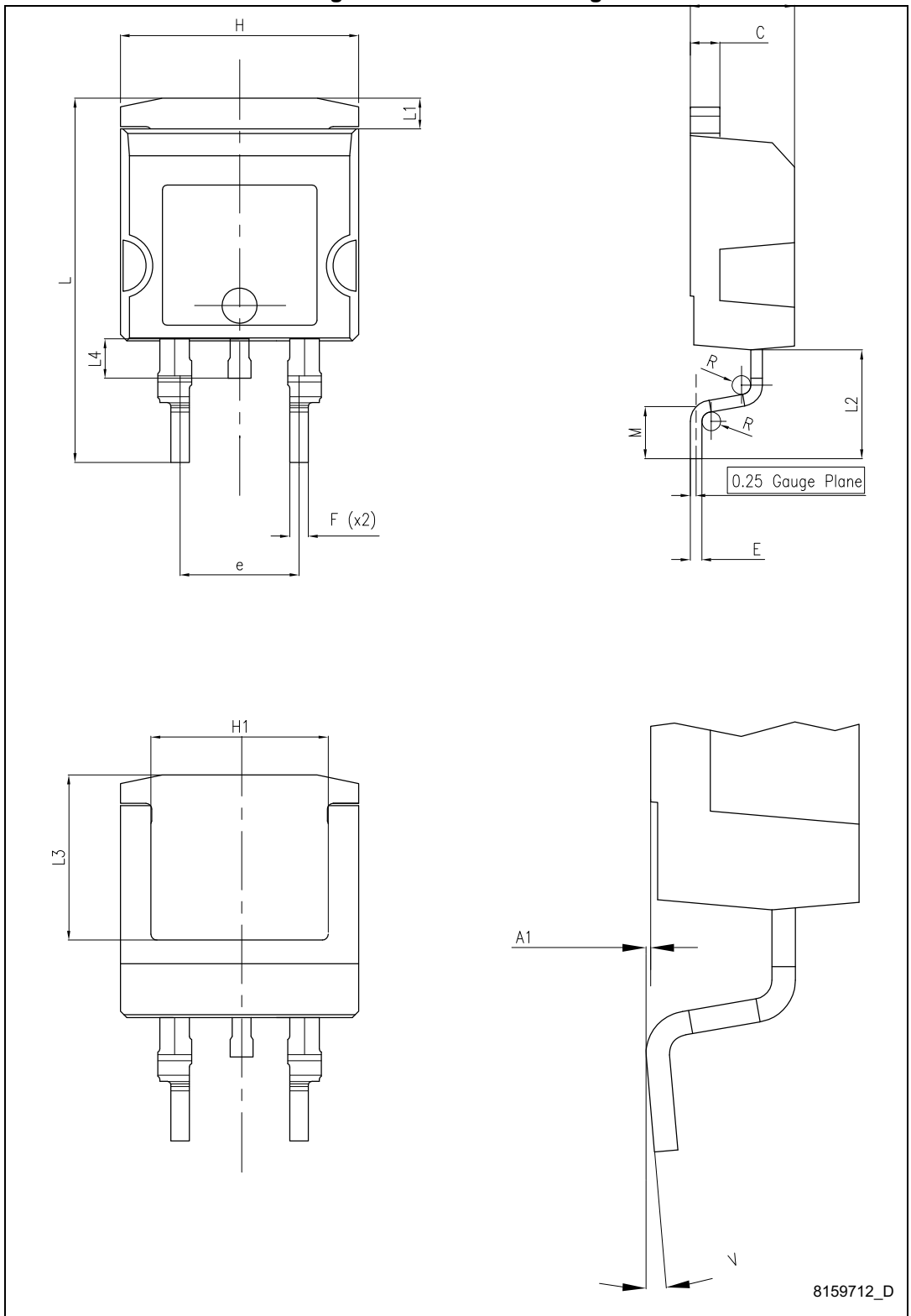
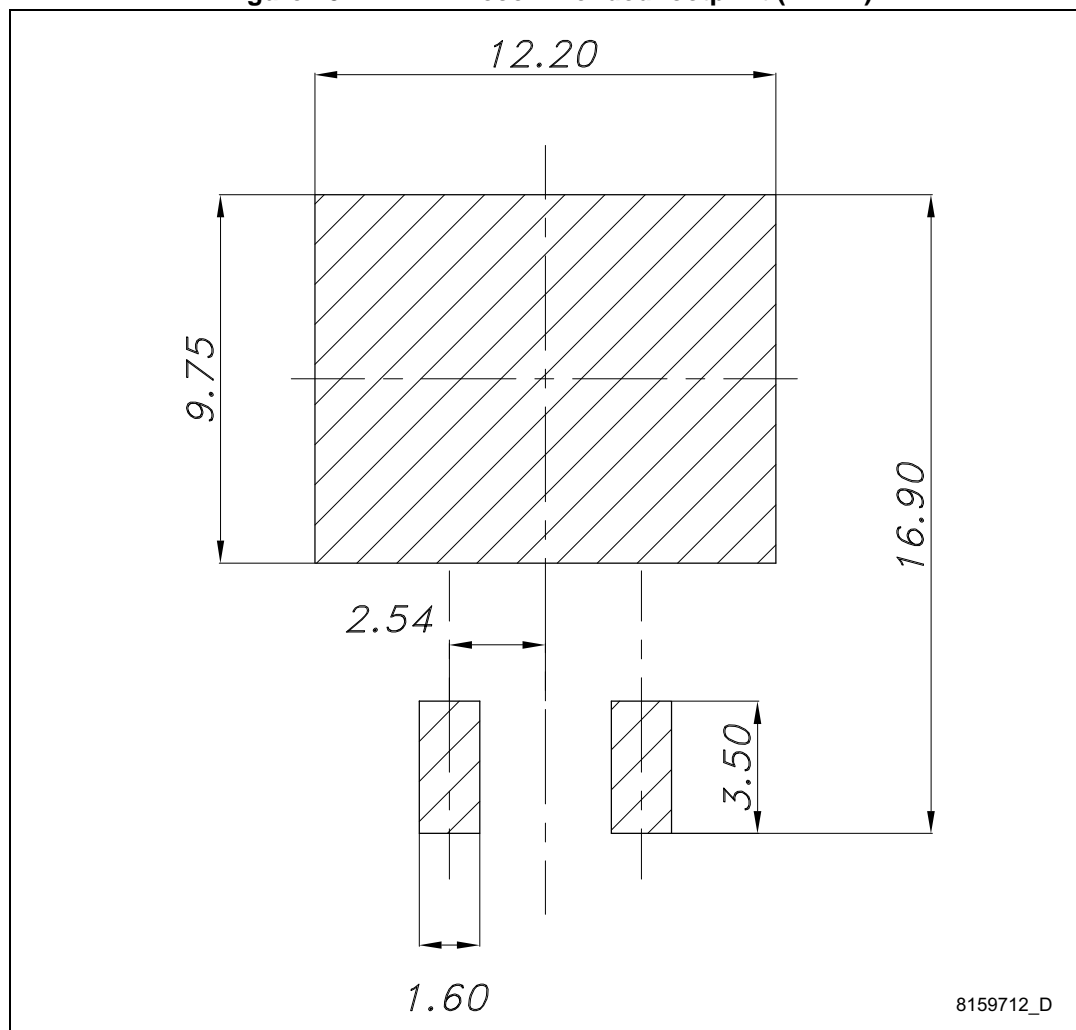


Table 8. H<sup>2</sup>PAK-2 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.30		4.80
A1	0.03		0.20
C	1.17		1.37
e	4.98		5.18
E	0.50		0.90
F	0.78		0.85
H	10.00		10.40
H1	7.40		7.80
L	15.30		15.80
L1	1.27		1.40
L2	4.93		5.23
L3	6.85		7.25
L4	1.5		1.7
M	2.6		2.9
R	0.20		0.60
V	0°		8°

Figure 20. H<sup>2</sup>PAK-2 recommended footprint (in mm)



8159712\_D

### 5.2 H<sup>2</sup>PAK-6, STH275N8F7-6AG

Figure 21. H<sup>2</sup>PAK-6 drawing

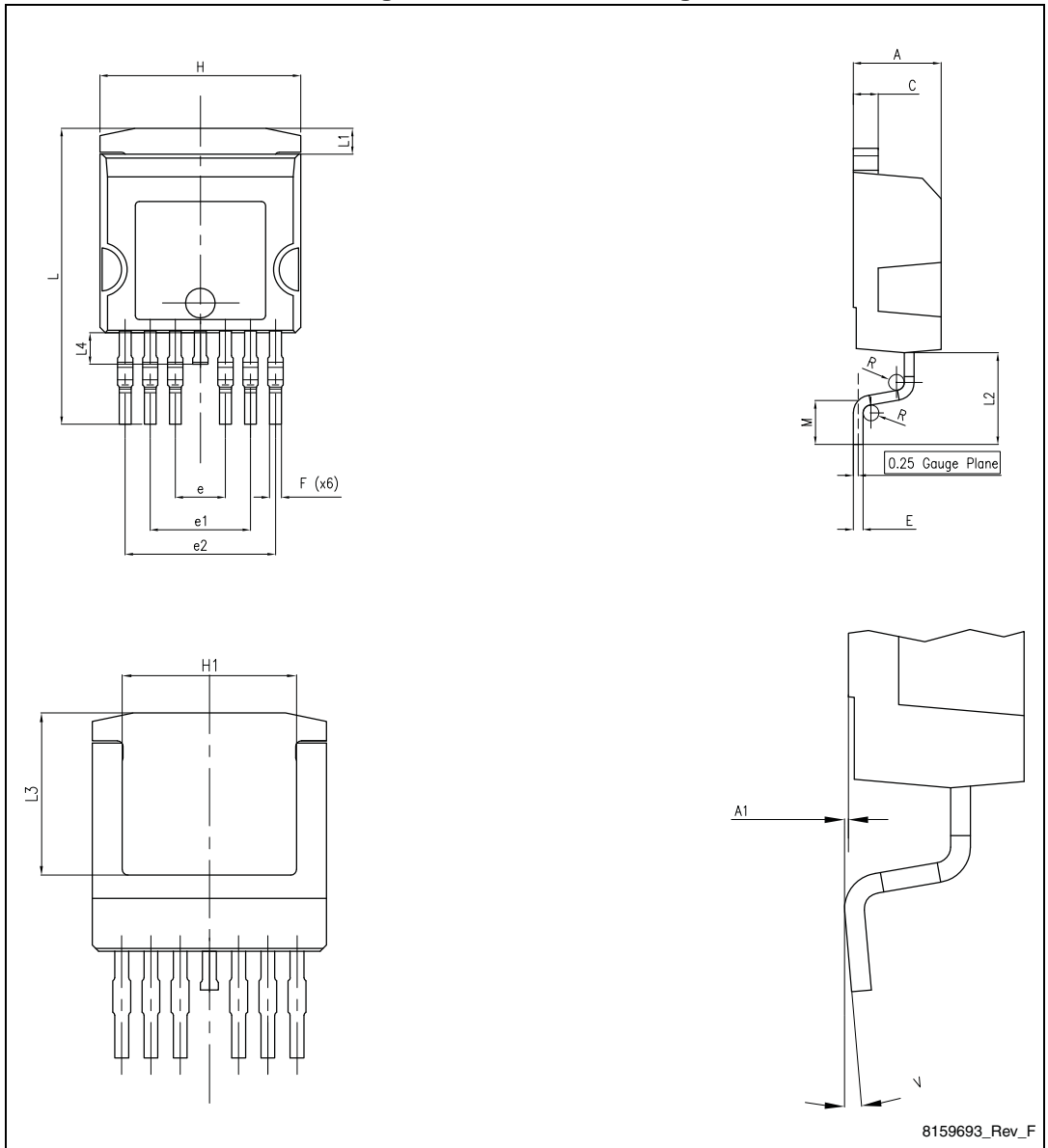
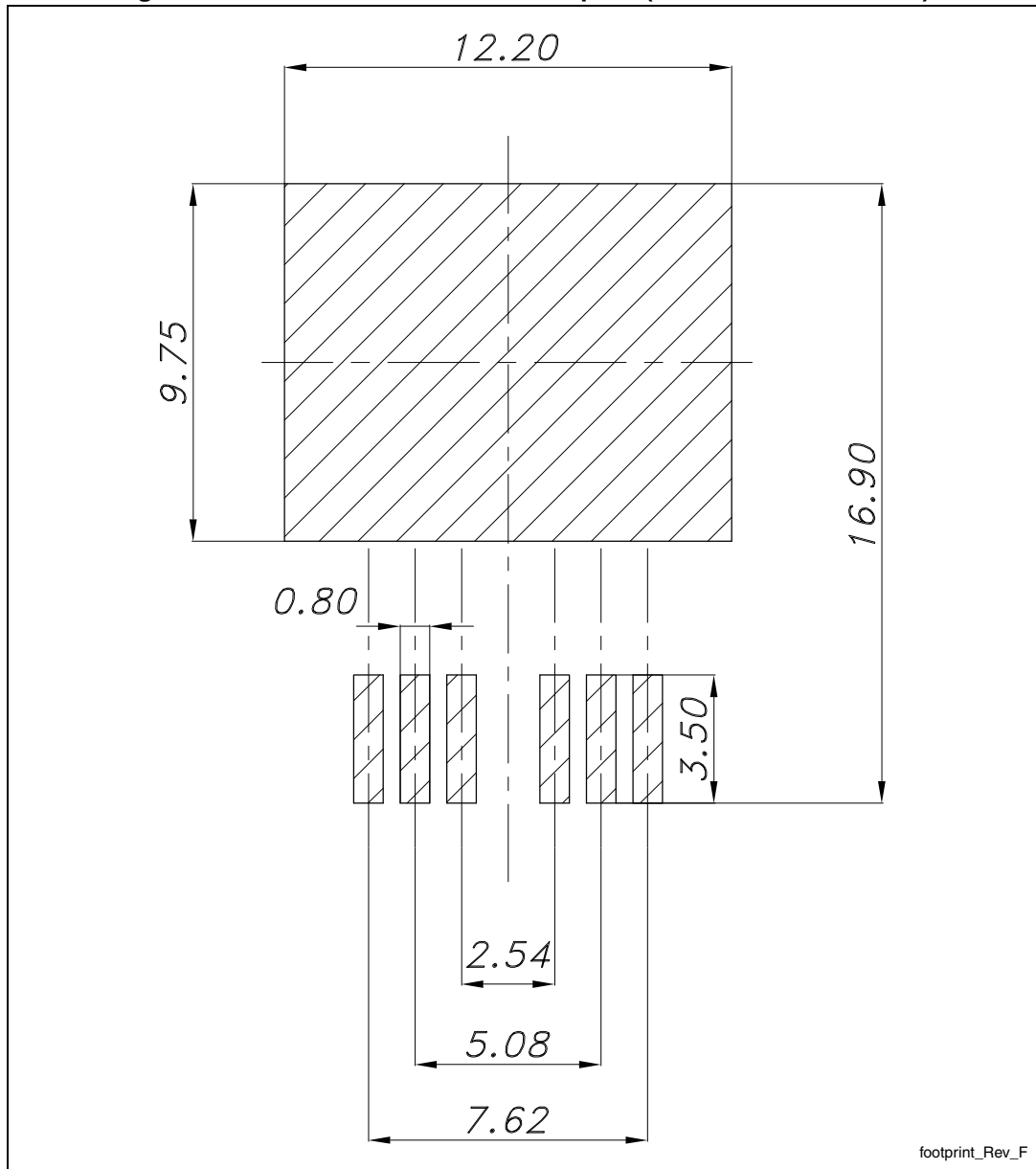


Table 9. H<sup>2</sup>PAK-6 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.30		4.80
A1	0.03		0.20
C	1.17		1.37
e	2.34		2.74
e1	4.88		5.28
e2	7.42		7.82
E	0.45		0.60
F	0.50		0.70
H	10.00		10.40
H1	7.40		7.80
L	14.75		15.25
L1	1.27		1.40
L2	4.35		4.95
L3	6.85		7.25
L4	1.5		1.75
M	1.90		2.50
R	0.20		0.60
V	0°		8°

Figure 22. H<sup>2</sup>PAK-6 recommended footprint (dimensions are in mm)



# 6 Packaging information

Figure 23. Tape

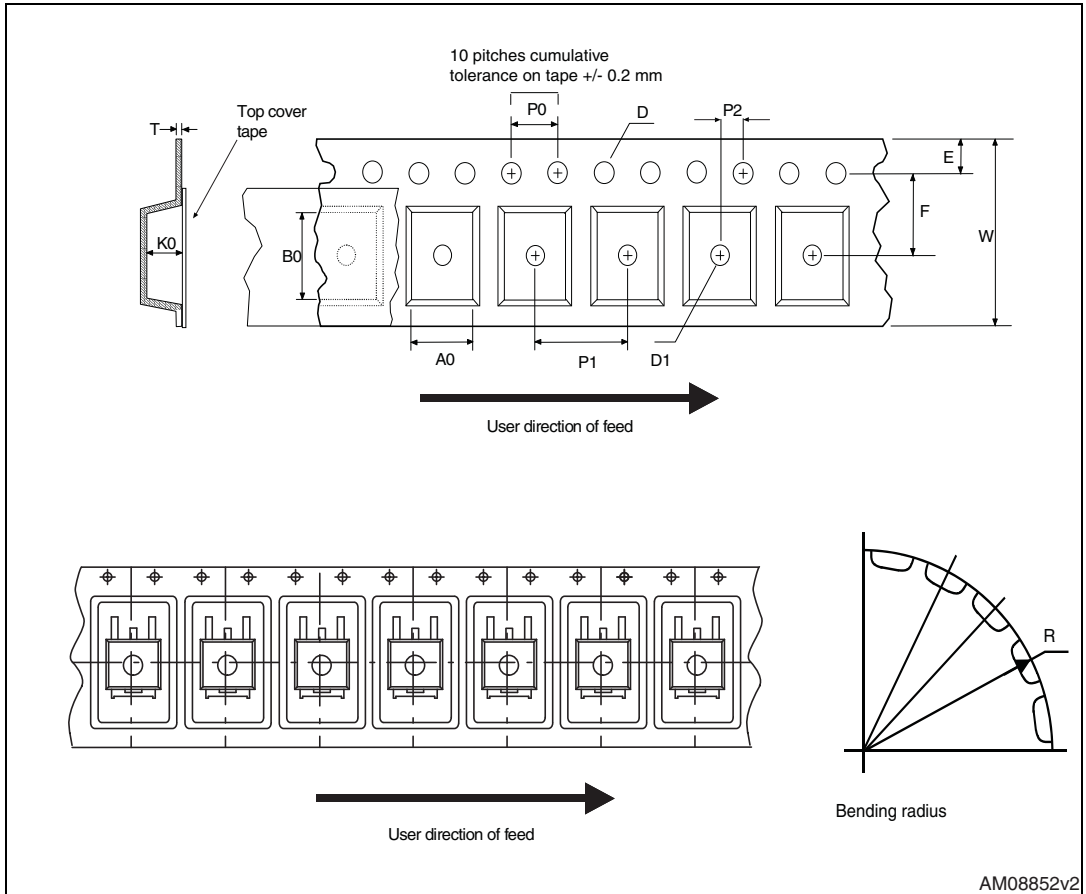
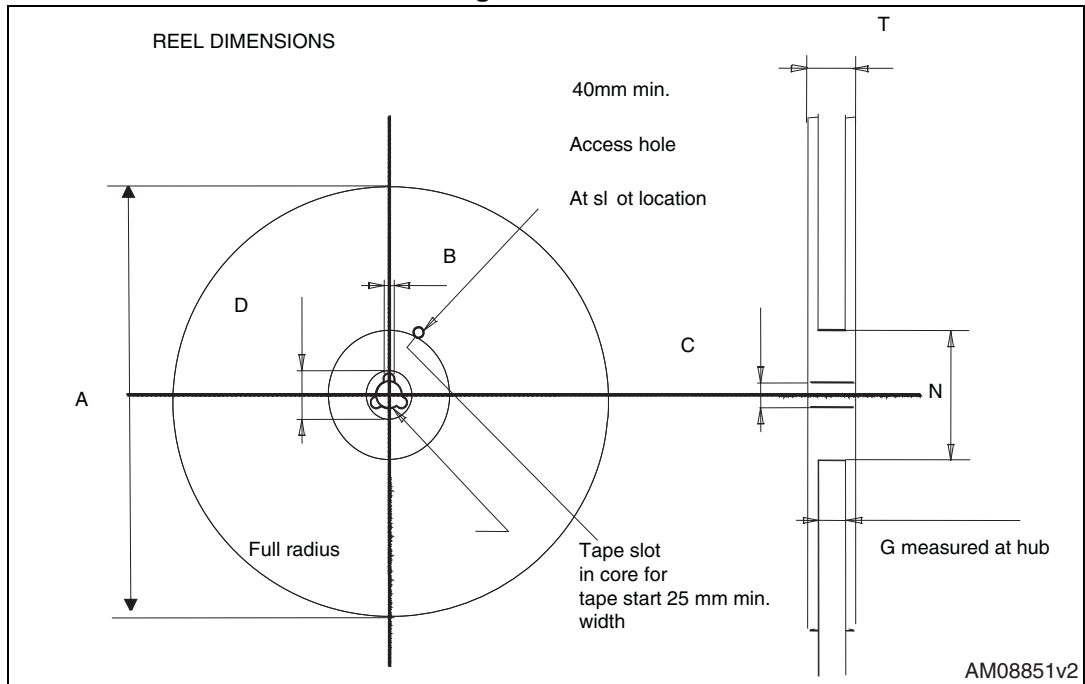




Figure 24. Reel



AM08851v2

Table 10. Tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base qty		1000
P2	1.9	2.1	Bulk qty		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

## 7 Revision history

Table 11. Document revision history

Date	Revision	Changes
27-Nov-2014	1	First release.
05-Mar-2015	2	Document status promoted from preliminary to production data. Updated title and feature in cover page.
10-Mar-2016	3	Updated <a href="#">Table 4</a> . Minor text changes.

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