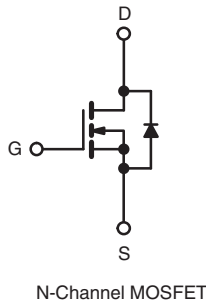
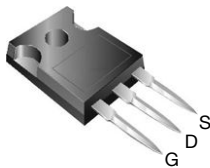


## Power MOSFET

PRODUCT SUMMARY		
$V_{DS}$ (V)	600	
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 10$ V	0.58
$Q_g$ (Max.) (nC)	70	
$Q_{gs}$ (nC)	19	
$Q_{gd}$ (nC)	28	
Configuration	Single	

TO-247AC



### FEATURES

- Low Gate Charge  $Q_g$  Results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic  $dV/dt$  Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Effective  $C_{OSS}$  Specified
- Compliant to RoHS Directive 2002/95/EC



**RoHS\***  
COMPLIANT

### APPLICATIONS

- Switch Mode Power Supply (SMPS)
- Uninterruptable Power Supply
- High Speed Power Switching

### TYPICAL SMPS TOPOLOGY

- PFC Boost

ORDERING INFORMATION	
Package	TO-247AC
Lead (Pb)-free	IRFPC50APbF SiHFPC50A-E3
SnPb	IRFPC50A SiHFPC50A


ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)					
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-Source Voltage		$V_{DS}$	600	V	
Gate-Source Voltage		$V_{GS}$	$\pm 30$		
Continuous Drain Current	$V_{GS}$ at 10 V	$I_D$	$T_C = 25$ °C	11	A
			$T_C = 100$ °C	7.0	
Pulsed Drain Current <sup>a</sup>		$I_{DM}$	44		
Linear Derating Factor			1.4	W/°C	
Single Pulse Avalanche Energy <sup>b</sup>		$E_{AS}$	920	mJ	
Repetitive Avalanche Current <sup>a</sup>		$I_{AR}$	11	A	
Repetitive Avalanche Energy <sup>a</sup>		$E_{AR}$	18	mJ	
Maximum Power Dissipation	$T_C = 25$ °C	$P_D$	180	W	
Peak Diode Recovery $dV/dt^c$		$dV/dt$	4.9	V/ns	
Operating Junction and Storage Temperature Range		$T_J, T_{stg}$	- 55 to + 150	°C	
Soldering Recommendations (Peak Temperature)	for 10 s		300 <sup>d</sup>		
Mounting Torque	6-32 or M3 screw		10		lbf · in
			1.1	N · m	

#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Starting  $T_J = 25$  °C,  $L = 15$  mH,  $R_g = 25$   $\Omega$ ,  $I_{AS} = 11$  A (see fig. 12).
- $I_{SD} \leq 11$  A,  $dI/dt \leq 126$  A/ $\mu$ s,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150$  °C.
- 1.6 mm from case.

\* Pb containing terminations are not RoHS compliant, exemptions may apply

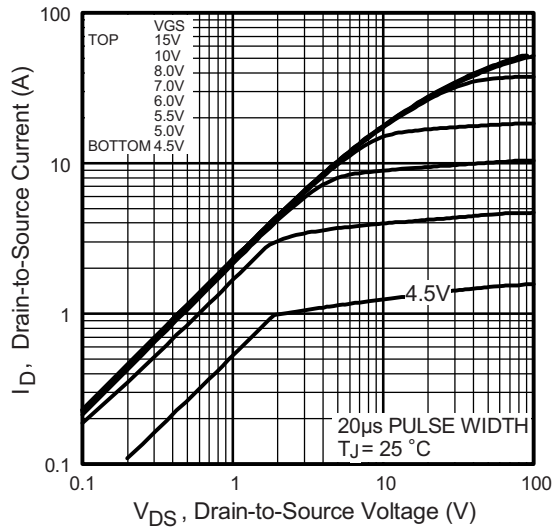
THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	40	°C/W
Case-to-Sink, Flat, Greased Surface	$R_{thCS}$	0.24	-	
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	0.65	

SPECIFICATIONS ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}$ , $I_D = 250\text{ }\mu\text{A}$	600	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$ , $I_D = 1\text{ mA}$	-	0.65	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	2.0	-	4.0	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 30\text{ V}$	-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 600\text{ V}$ , $V_{GS} = 0\text{ V}$	-	-	25	$\mu\text{A}$
		$V_{DS} = 480\text{ V}$ , $V_{GS} = 0\text{ V}$ , $T_J = 125\text{ }^\circ\text{C}$	-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$ , $I_D = 6.0\text{ A}^b$	-	-	0.58	$\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS} = 50\text{ V}$ , $I_D = 6.0\text{ A}^b$	7.7	-	-	S
<b>Dynamic</b>						
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}$ , $V_{DS} = 25\text{ V}$ , $f = 1.0\text{ MHz}$ , see fig. 5	-	2100	-	pF
Output Capacitance	$C_{oss}$		-	270	-	
Reverse Transfer Capacitance	$C_{rss}$		-	9.7	-	
Output Capacitance	$C_{oss}$	$V_{GS} = 0\text{ V}$	$V_{DS} = 1.0\text{ V}$ , $f = 1.0\text{ MHz}$	-	2830	-
			$V_{DS} = 480\text{ V}$ , $f = 1.0\text{ MHz}$	-	74	-
Effective Output Capacitance	$C_{oss\text{ eff.}}$	$V_{DS} = 0\text{ V to }480\text{ V}^c$	-	81	-	
Total Gate Charge	$Q_g$	$V_{GS} = 10\text{ V}$ , $I_D = 11\text{ A}$ , $V_{DS} = 480\text{ V}$ see fig. 6 and 13 <sup>b</sup>	-	-	70	nC
Gate-Source Charge	$Q_{gs}$		-	-	19	
Gate-Drain Charge	$Q_{gd}$		-	-	28	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 300\text{ V}$ , $I_D = 11\text{ A}$ $R_g = 6.2\text{ }\Omega$ , $R_D = 30\text{ }\Omega$ see fig. 10 <sup>b</sup>	-	15	-	ns
Rise Time	$t_r$		-	40	-	
Turn-Off Delay Time	$t_{d(off)}$		-	33	-	
Fall Time	$t_f$		-	29	-	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	11	A
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$		-	-	44	
Body Diode Voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}$ , $I_S = 11\text{ A}$ , $V_{GS} = 0\text{ V}^b$	-	-	1.4	V
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}$ , $I_F = 11\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}^b$	-	500	740	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$		-	4.0	6.0	$\mu\text{C}$
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )				

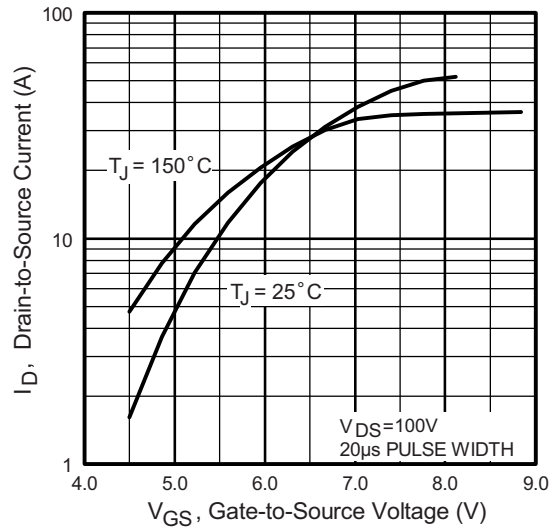
### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- $C_{oss\text{ eff.}}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DS}$ .

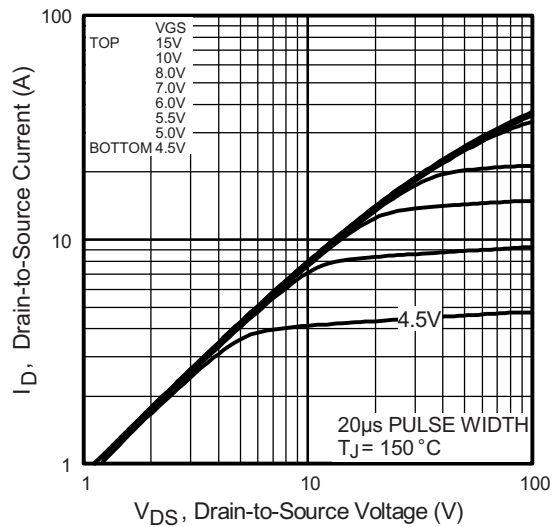
## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



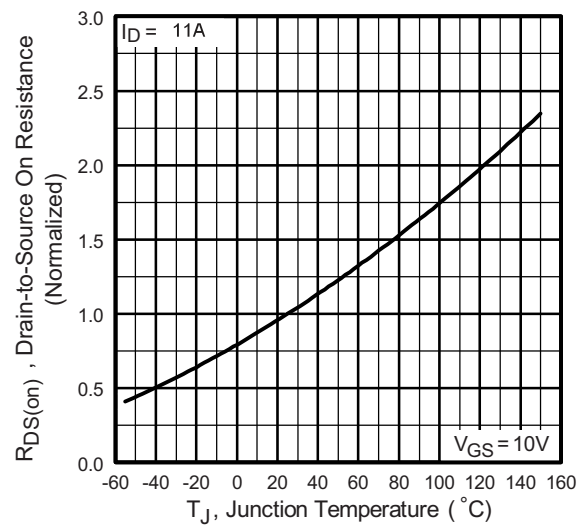
**Fig. 1 - Typical Output Characteristics**



**Fig. 3 - Typical Transfer Characteristics**



**Fig. 2 - Typical Output Characteristics**



**Fig. 4 - Normalized On-Resistance vs. Temperature**

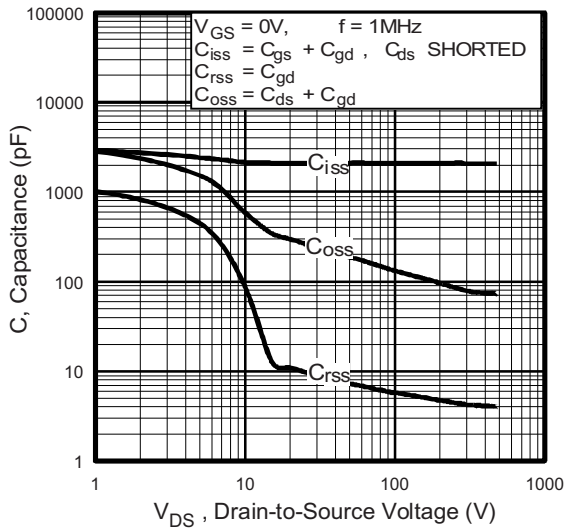


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

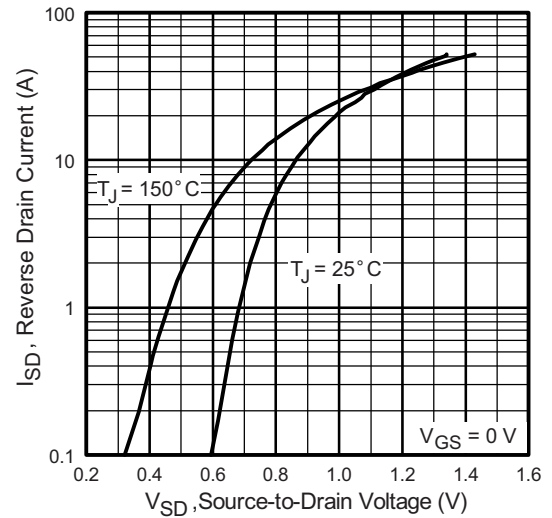


Fig. 7 - Typical Source-Drain Diode Forward Voltage

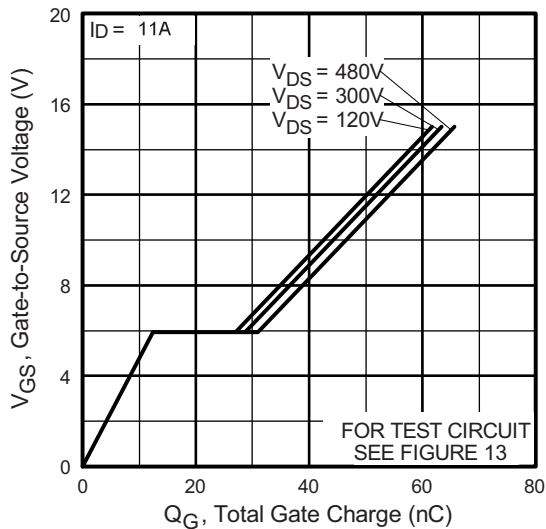


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

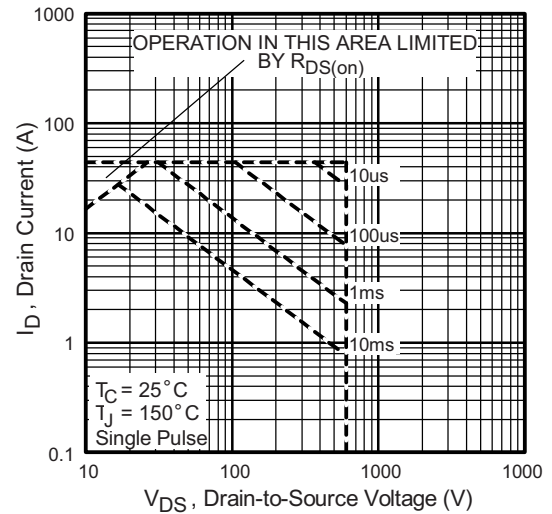


Fig. 8 - Maximum Safe Operating Area

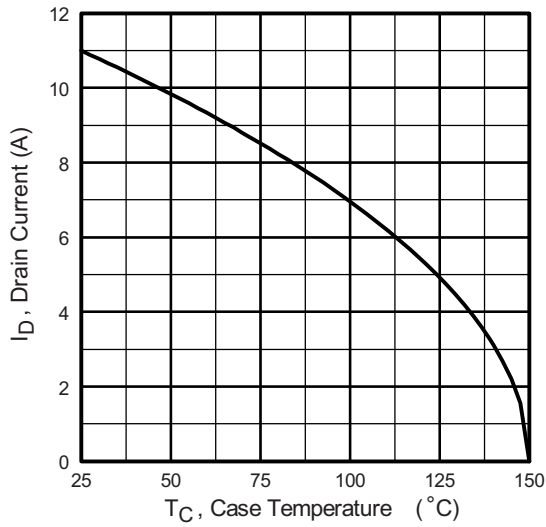


Fig. 9 - Maximum Drain Current vs. Case Temperature

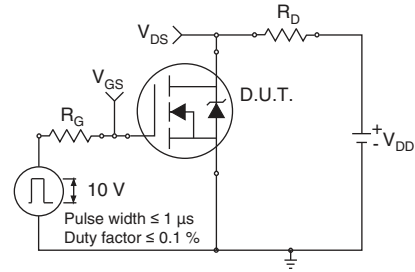


Fig. 10a - Switching Time Test Circuit

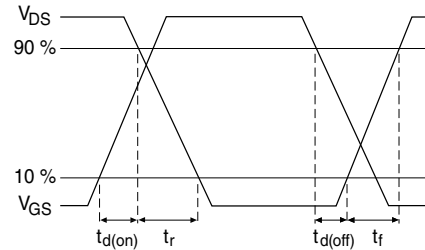


Fig. 10b - Switching Time Waveforms

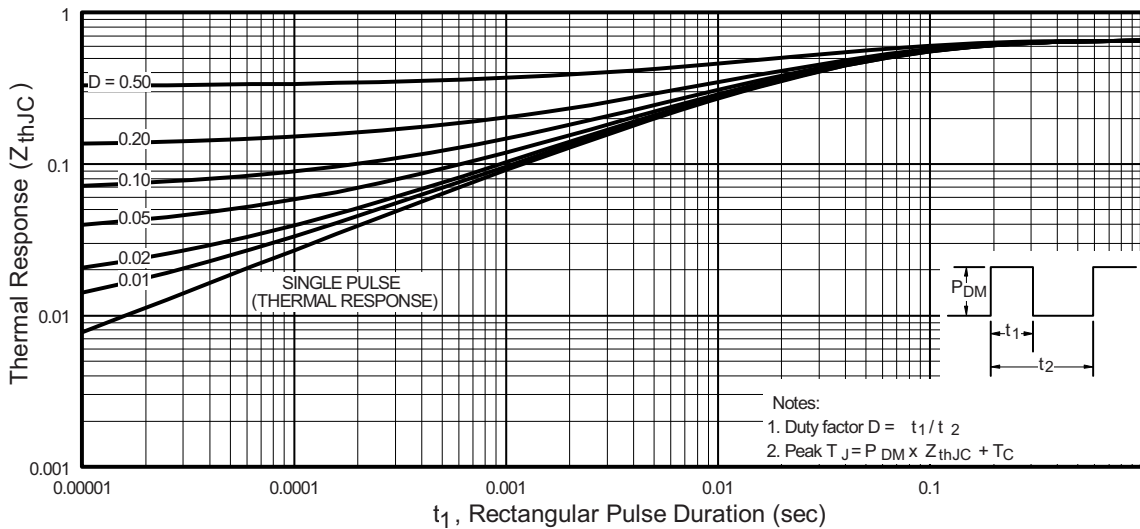


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

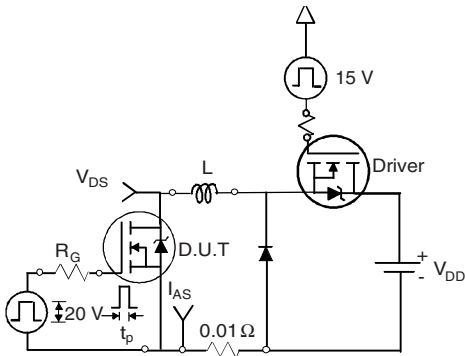


Fig. 12a - Unclamped Inductive Test Circuit

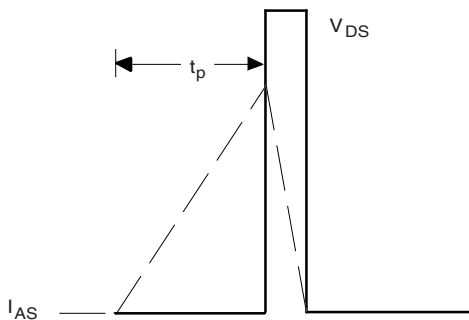


Fig. 12b - Unclamped Inductive Waveforms

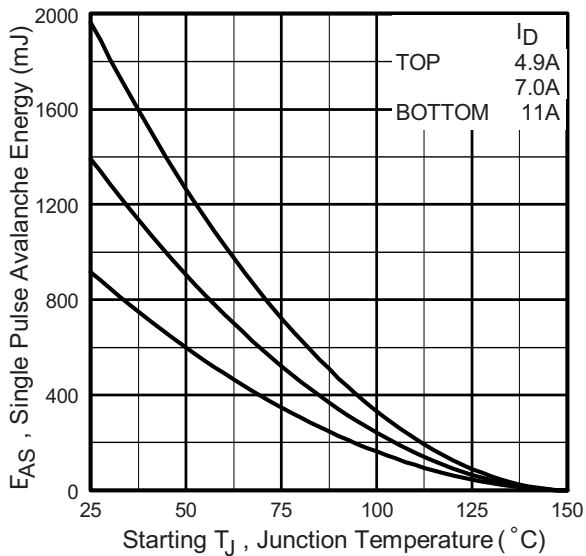


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

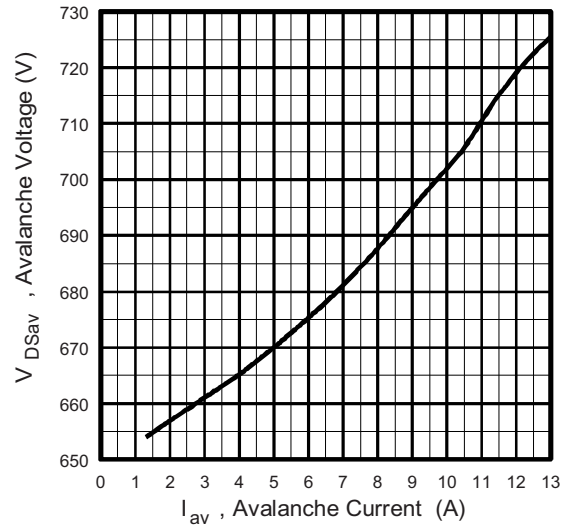


Fig. 12d - Typical Drain-to-Source Voltage vs. Avalanche Current

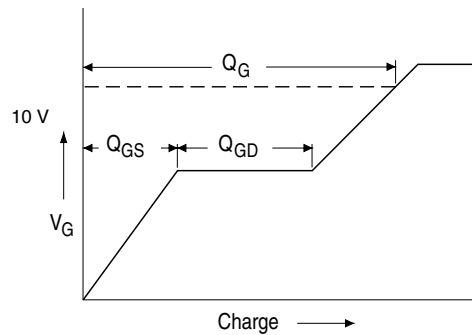


Fig. 13a - Basic Gate Charge Waveform

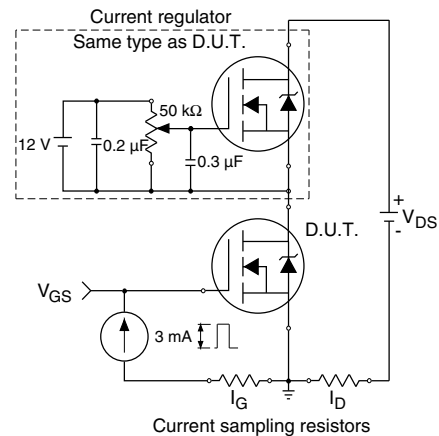
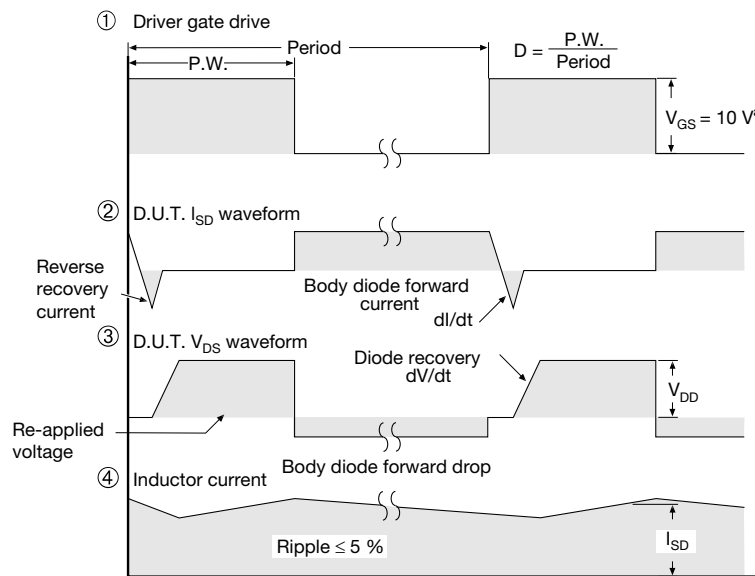
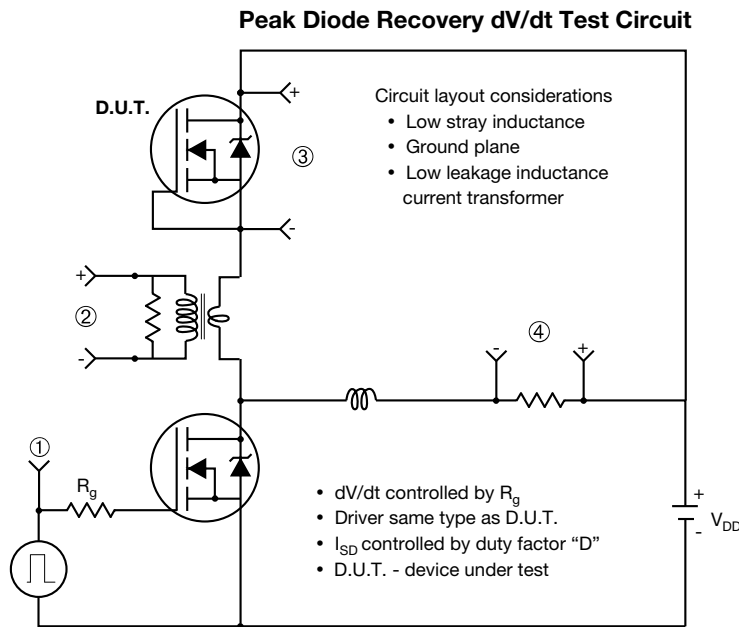


Fig. 13b - Gate Charge Test Circuit



**Note**

a.  $V_{GS} = 5 V$  for logic level devices

**Fig. 14 - For N-Channel**

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# TO-247AC (High Voltage)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.58	5.31	0.180	0.209
A1	2.21	2.59	0.087	0.102
A2	1.17	2.49	0.046	0.098
b	0.99	1.40	0.039	0.055
b1	0.99	1.35	0.039	0.053
b2	1.53	2.39	0.060	0.094
b3	1.65	2.37	0.065	0.093
b4	2.42	3.43	0.095	0.135
b5	2.59	3.38	0.102	0.133
c	0.38	0.86	0.015	0.034
c1	0.38	0.76	0.015	0.030
D	19.71	20.82	0.776	0.820
D1	13.08	-	0.515	-

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D2	0.51	1.30	0.020	0.051
E	15.29	15.87	0.602	0.625
E1	13.72	-	0.540	-
e	5.46 BSC		0.215 BSC	
Ø k	0.254		0.010	
L	14.20	16.25	0.559	0.640
L1	3.71	4.29	0.146	0.169
N	7.62 BSC		0.300 BSC	
Ø P	3.51	3.66	0.138	0.144
Ø P1	-	7.39	-	0.291
Q	5.31	5.69	0.209	0.224
R	4.52	5.49	0.178	0.216
S	5.51 BSC		0.217 BSC	

ECN: X13-0103-Rev. D, 01-Jul-13  
DWG: 5971

**Notes**

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Contour of slot optional.
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body.
4. Thermal pad contour optional with dimensions D1 and E1.
5. Lead finish uncontrolled in L1.
6. Ø P to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154").
7. Outline conforms to JEDEC outline TO-247 with exception of dimension c.
8. Xian and Mingxin actually photo.







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